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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke14f512vll16r

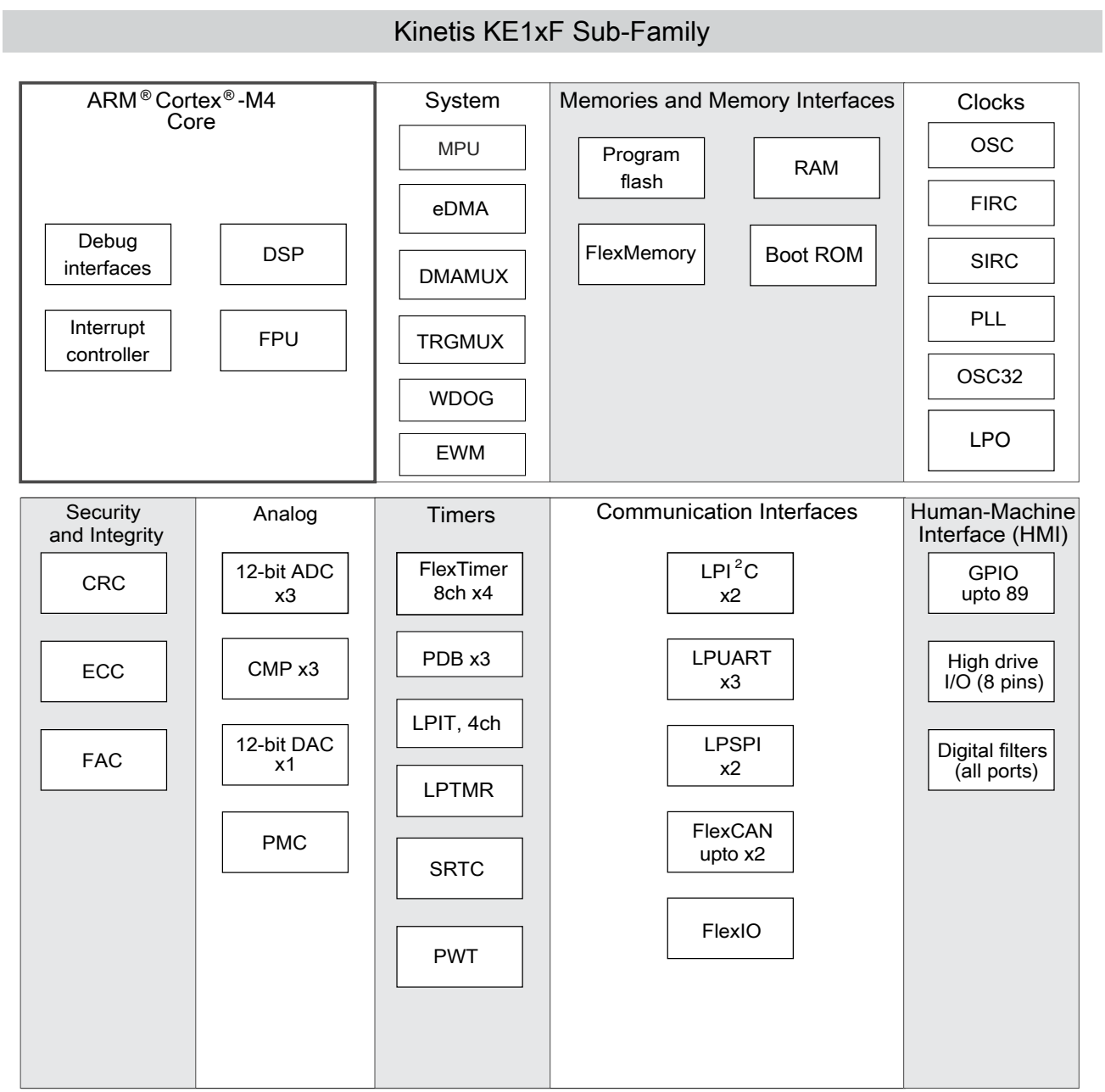


Figure 1. Functional block diagram

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory			Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels	FlexCAN
MKE18F512VLL16	MKE18F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	2
MKE18F512VLH16	MKE18F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	2
MKE18F256VLL16	MKE18F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	2
MKE18F256VLH16	MKE18F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	2
MKE16F512VLL16	MKE16F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	1
MKE16F512VLH16	MKE16F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	1
MKE16F256VLL16	MKE16F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	1
MKE16F256VLH16	MKE16F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	1
MKE14F512VLL16	MKE14F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	0
MKE14F512VLH16	MKE14F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	0
MKE14F256VLL16	MKE14F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	0
MKE14F256VLH16	MKE14F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	0

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device.

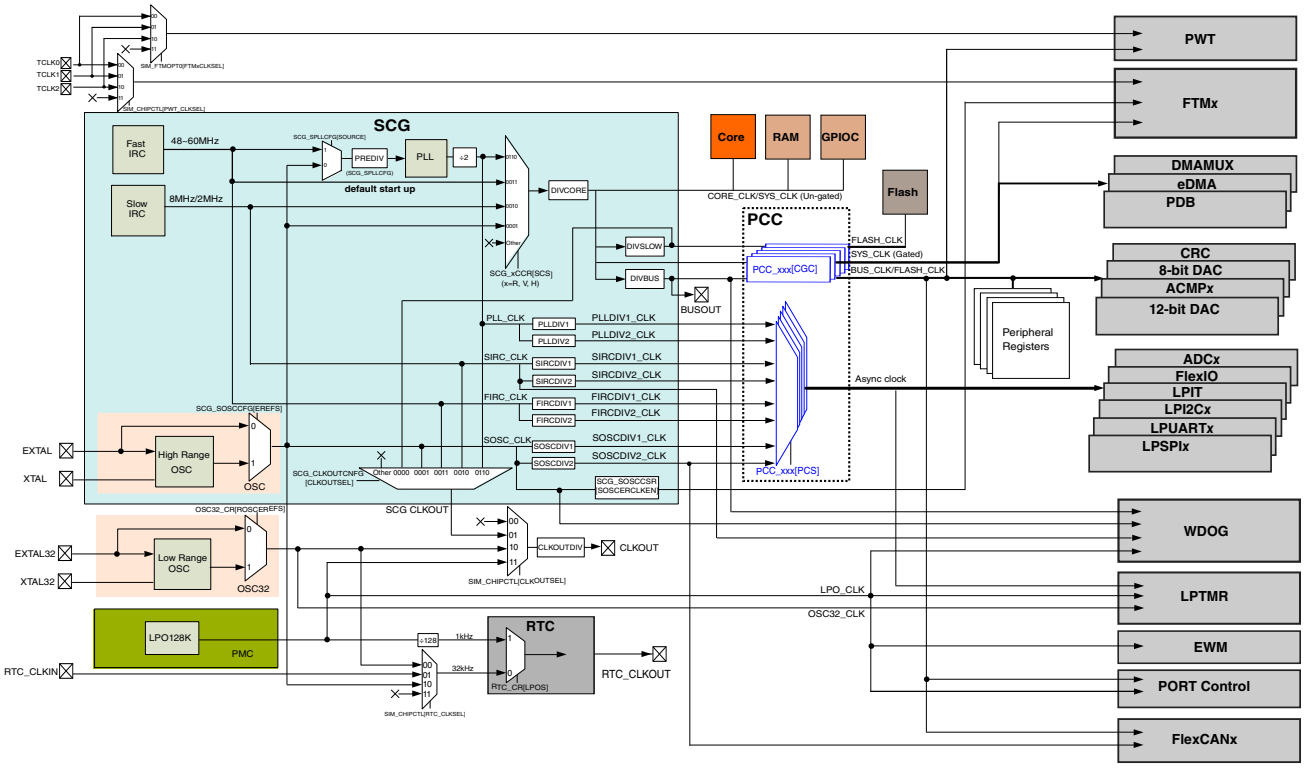


Figure 4. Clocking block diagram

2.1.7 Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD/JTAG port cannot access the memory resources of the MCU.

External interface	Security	Unsecure
SWD/JTAG port	Can't access memory source by SWD/ JTAG interface	the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command

2.1.7.1 Flash Access Control (FAC)

The FAC is a native or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×

2.2.14 LPI2C

This device contains two LPI2C modules. The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

The LPI2C modules have the following features:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- HS-mode supported in slave mode
- Multi-master support including synchronization and arbitration
- Clock stretching
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID require software support
- For master mode:
  - command/transmit FIFO of 4 words
  - receive FIFO of 4 words
- For slave mode:
  - separate I2C slave registers to minimize software overhead due to master/slave switching
  - support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
  - transmit/receive data register supporting interrupt or DMA requests

2.2.15 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer

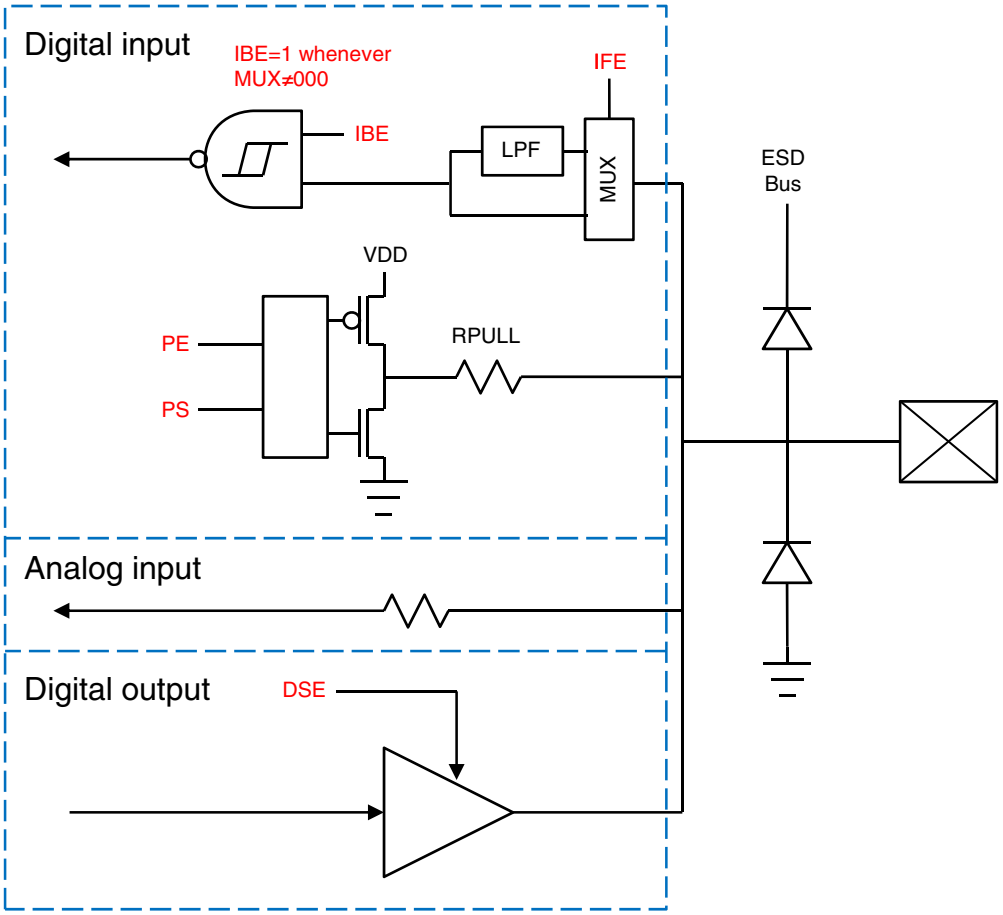


Figure 5. I/O simplified block diagram

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

4 Pinouts

4.1 KE1xF Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16			FTM2_CH7		FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15			FTM2_CH6		FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	ADC2_SE1	ADC2_SE1	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	ADC2_SE0	ADC2_SE0	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	ADC2_SE13	ADC2_SE13	PTE11	PWT_IN1	LPTMR0_ ALT1	FTM2_CH5		FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	ADC2_SE12	ADC2_SE12	PTE10	CLKOUT		FTM2_CH4		FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13			FTM2_FLT0			
8	5	PTE5	DISABLED		PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3	CAN0_TX	FXIO_D7	EWM_IN
9	6	PTE4	DISABLED		PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2	CAN0_RX	FXIO_D6	EWM_OUT_b

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	7	VDD	VDD	VDD							
11	8	VDDA	VDDA	VDDA							
12	9	VREFH	VREFH	VREFH							
13	—	VREFL	VREFL	VREFL							
14	—	VSS	VSS	VSS							
15	11	PTB7	EXTAL	EXTAL	PTB7	LPI2C0_SCL					
16	12	PTB6	XTAL	XTAL	PTB6	LPI2C0_SDA					
17	—	PTE14	ACMP2_IN3	ACMP2_IN3	PTE14	FTM0_FLT1		FTM2_FLT1			
18	13	PTE3	DISABLED		PTE3	FTM0_FLT0	LPUART2_ RTS	FTM2_FLT0		TRGMUX_IN6	ACMP2_OUT
19	—	PTE12	DISABLED		PTE12	FTM0_FLT3	LPUART2_TX				
20	—	PTD17	DISABLED		PTD17	FTM0_FLT2	LPUART2_RX				
21	14	PTD16	ACMP2_IN0	ACMP2_IN0	PTD16	FTM0_CH1					
22	15	PTD15	ACMP2_IN1	ACMP2_IN1	PTD15	FTM0_CH0					
23	16	PTE9	ACMP2_IN2/ DAC0_OUT	ACMP2_IN2/ DAC0_OUT	PTE9	FTM0_CH7	LPUART2_ CTS				
24	—	PTD14	DISABLED		PTD14	FTM2_CH5					CLKOUT
25	—	PTD13	DISABLED		PTD13	FTM2_CH4					RTC_CLKOUT
26	17	PTE8	ACMP0_IN3	ACMP0_IN3	PTE8	FTM0_CH6					
27	18	PTB5	DISABLED		PTB5	FTM0_CH5	LPSPI0_PCS1			TRGMUX_IN0	ACMP1_OUT
28	19	PTB4	ACMP1_IN2	ACMP1_IN2	PTB4	FTM0_CH4	LPSPI0_SOUT			TRGMUX_IN1	
29	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	FTM0_CH3	CAN0_TX				
30	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	FTM0_CH2	CAN0_RX				
31	22	PTD7	DISABLED		PTD7	LPUART2_TX		FTM2_FLT3			
32	23	PTD6	DISABLED		PTD6	LPUART2_RX		FTM2_FLT2			
33	24	PTD5	DISABLED		PTD5	FTM2_CH3	LPTMR0_ ALT2	FTM2_FLT1	PWT_IN2	TRGMUX_IN7	
34	—	PTD12	DISABLED		PTD12	FTM2_CH2	LPI2C1_HREQ			LPUART2_ RTS	
35	—	PTD11	DISABLED		PTD11	FTM2_CH1	FTM2_QD_ PHA			LPUART2_ CTS	
36	—	PTD10	DISABLED		PTD10	FTM2_CH0	FTM2_QD_ PHB				
37	—	VSS	VSS	VSS							
38	—	VDD	VDD	VDD							
39	25	PTC1	ADC0_SE9/ ACMP1_IN3	ADC0_SE9/ ACMP1_IN3	PTC1	FTM0_CH1				FTM1_CH7	
40	26	PTC0	ADC0_SE8/ ACMP1_IN4	ADC0_SE8/ ACMP1_IN4	PTC0	FTM0_CH0				FTM1_CH6	

Table 21. LPSPI*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPSPI*n*_SOUT	SOUT	Serial Data Out	O
LPSPI*n*_SIN	SIN	Serial Data In	I
LPSPI*n*_SCK	SCK	Serial Clock	I/O
LPSPI*n*_PCS[3:0]	PCS[3:0]	Peripheral Chip Select 0-3	I/O

Table 22. LPI2C*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPI2C*n*_SCL	SCL	Bidirectional serial clock line of the I2C system.	I/O
LPI2C*n*_SDA	SDA	Bidirectional serial data line of the I2C system.	I/O
LPI2C*n*_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C*n*_SCLS	SCLS	Secondary I2C clock line.	I/O
LPI2C*n*_SDAS	SDAS	Secondary I2C data line.	I/O

Table 23. LPUART*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART*n*_TX	LPUART_TX	Transmit data	O
LPUART*n*_RX	LPUART_RX	Receive data	I
LPUART*n*_CTS	LPUART_CTS	Clear to send	I
LPUART*n*_RTS	LPUART_RTS	Request to send	O

Table 24. FlexIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FXIO_D[7:0]	FXIO_D[7:0]	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

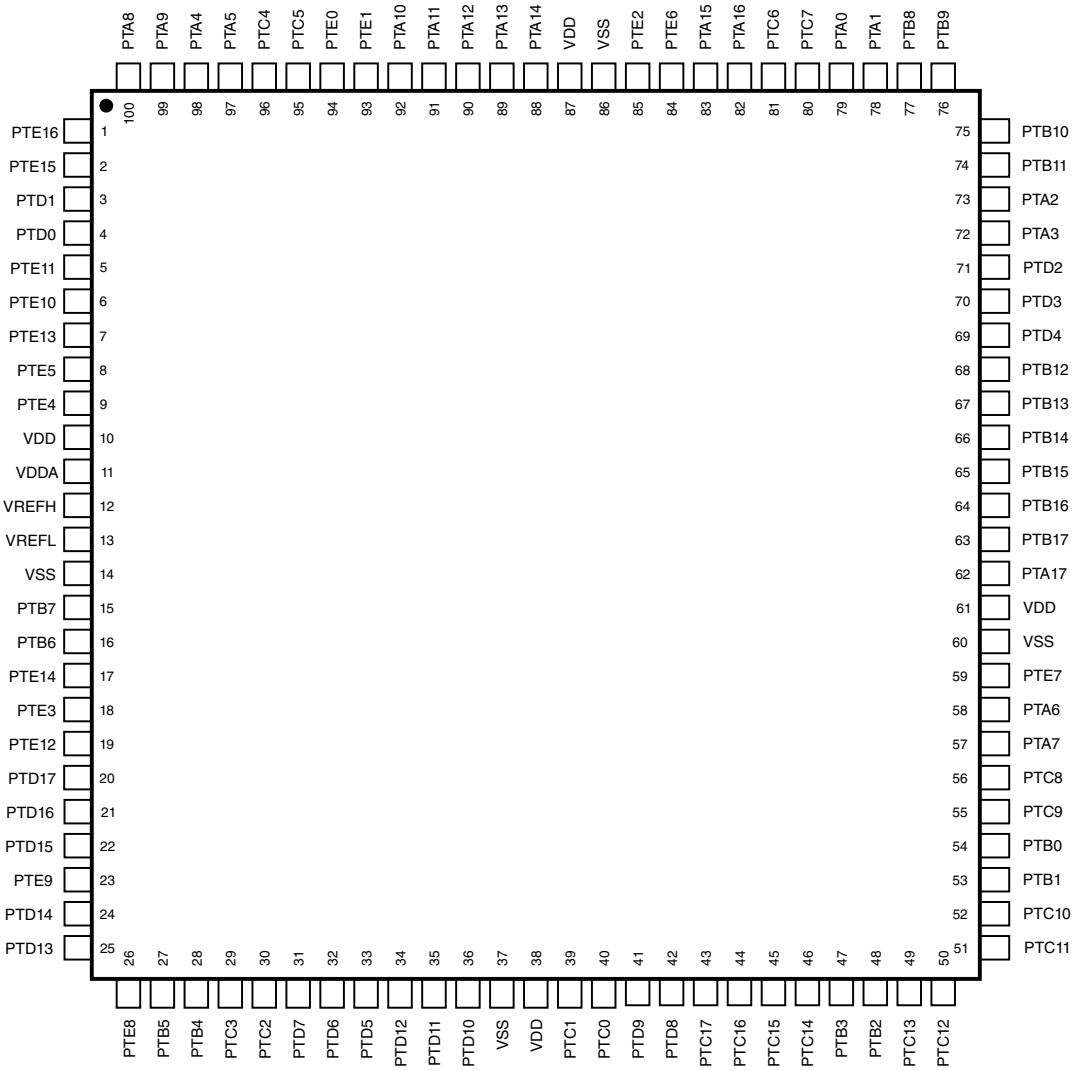


Figure 7. 100 LQFP Pinout Diagram

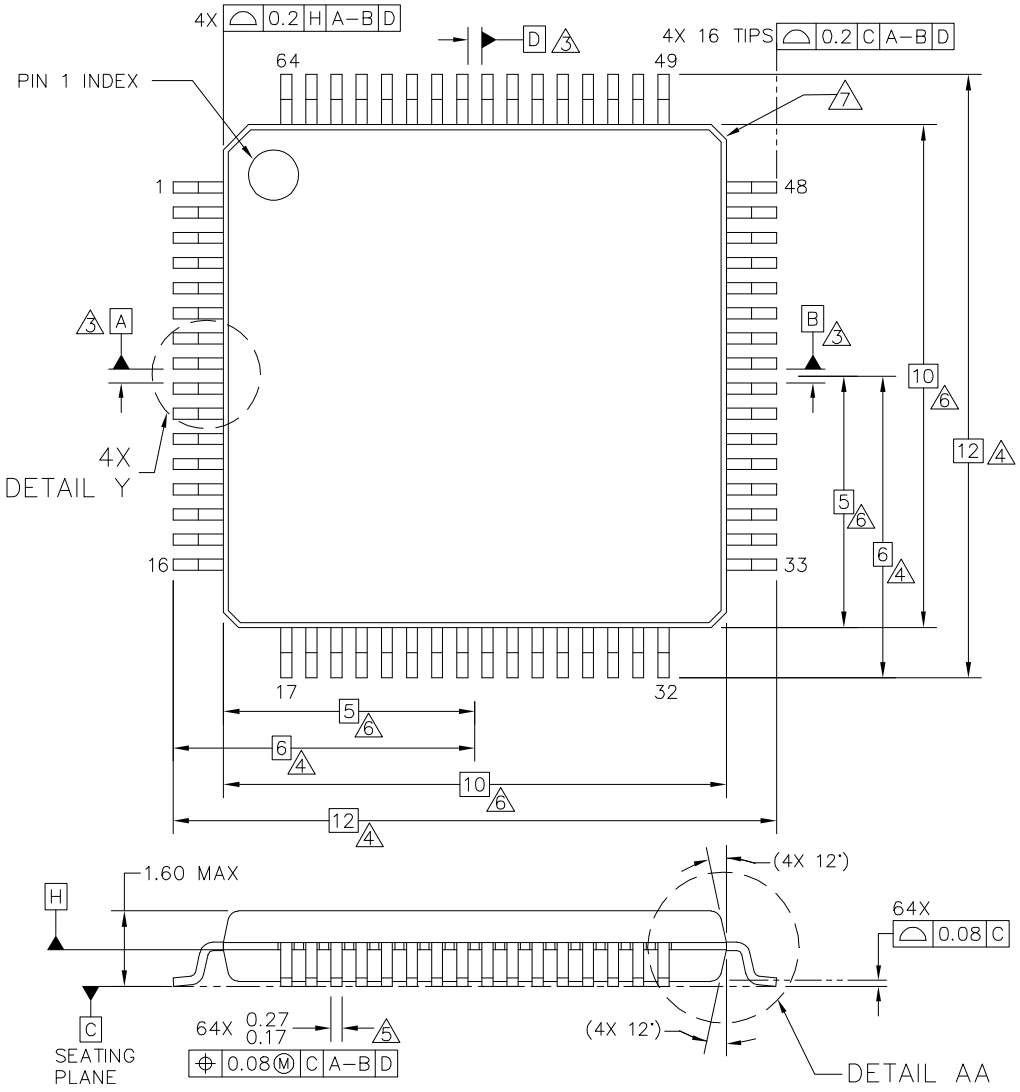


Figure 11. 64-pin LQFP package dimensions 1

Table 28. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{il}	Input Buffer Low Voltage @ V_{DD} = 3.3 V	V_{SS} – 0.3	—	0.3 × V_{DD}	V	
	@ V_{DD} = 5.0 V	V_{SS} – 0.3	—	0.35 × V_{DD}	V	
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_5	Normal drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V) @ V_{DD} = 3.3 V	2.8	—	—	mA	
	@ V_{DD} = 5.0 V	4.8	—	—	mA	
Iol_5	Normal drive I/O current sink capability measured when pad = 0.8 V @ V_{DD} = 3.3 V	2.4	—	—	mA	
	@ V_{DD} = 5.0 V	4.4	—	—	mA	
Ioh_20	High drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V)[2] @ V_{DD} = 3.3 V	10.8	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
Iol_20	High drive I/O current sink capability measured when pad = 0.8 V[4] @ V_{DD} = 3.3 V	10.1	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
I_leak	Hi-Z (Off state) leakage current (per pin)	—	—	300	nA	5, 6
V_{OH}	Output high voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	V_{DD} – 0.8	—	—	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	V_{DD} – 0.8	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	—	—	0.8	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	—	—	0.8	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	—	—	0.8	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	—	—	0.8	V	

Table continues on the next page...

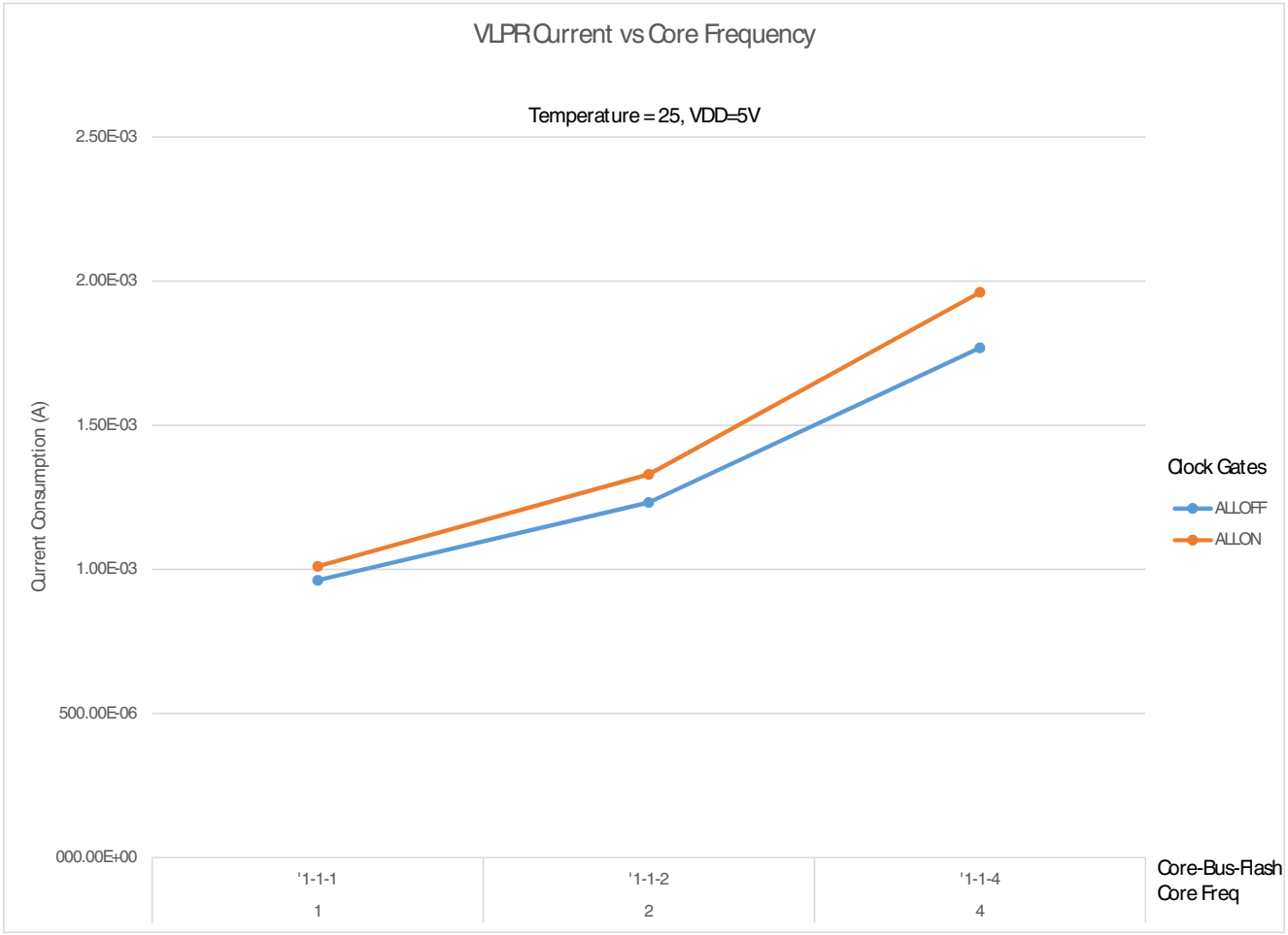


Figure 15. VLPR mode supply current vs. core frequency

5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 33. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 34. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus clock	—	84	MHz	

Table continues on the next page...

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 39. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	60	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	42	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	24	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	12	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 40. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	57	°C/W

Table continues on the next page...

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

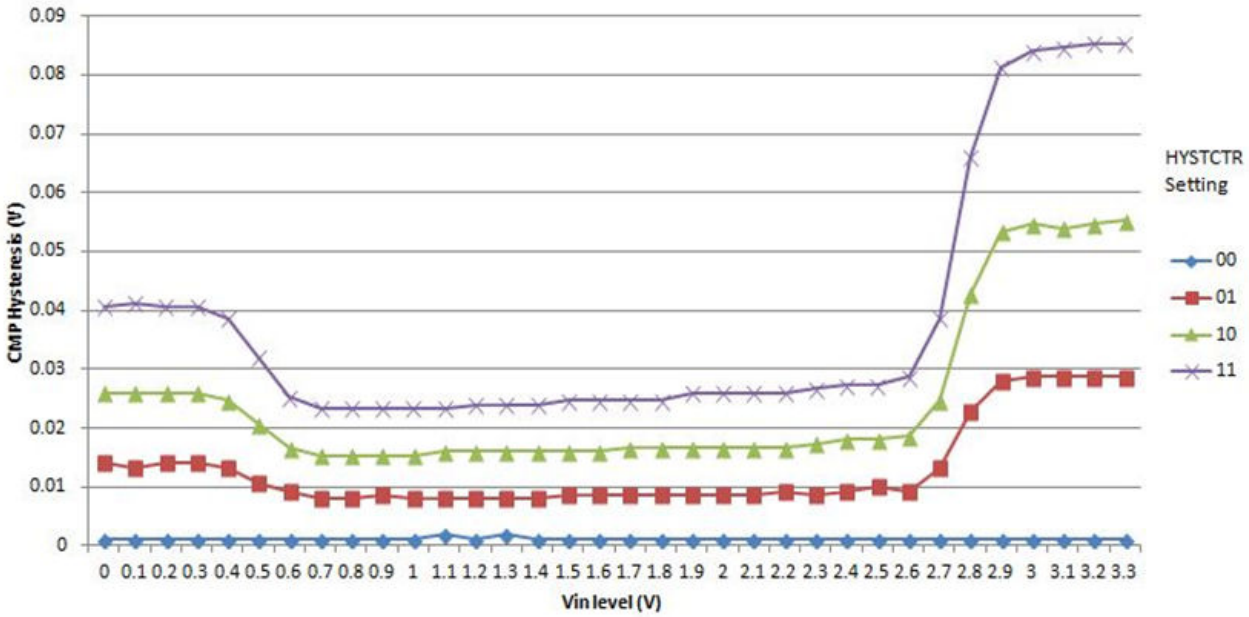
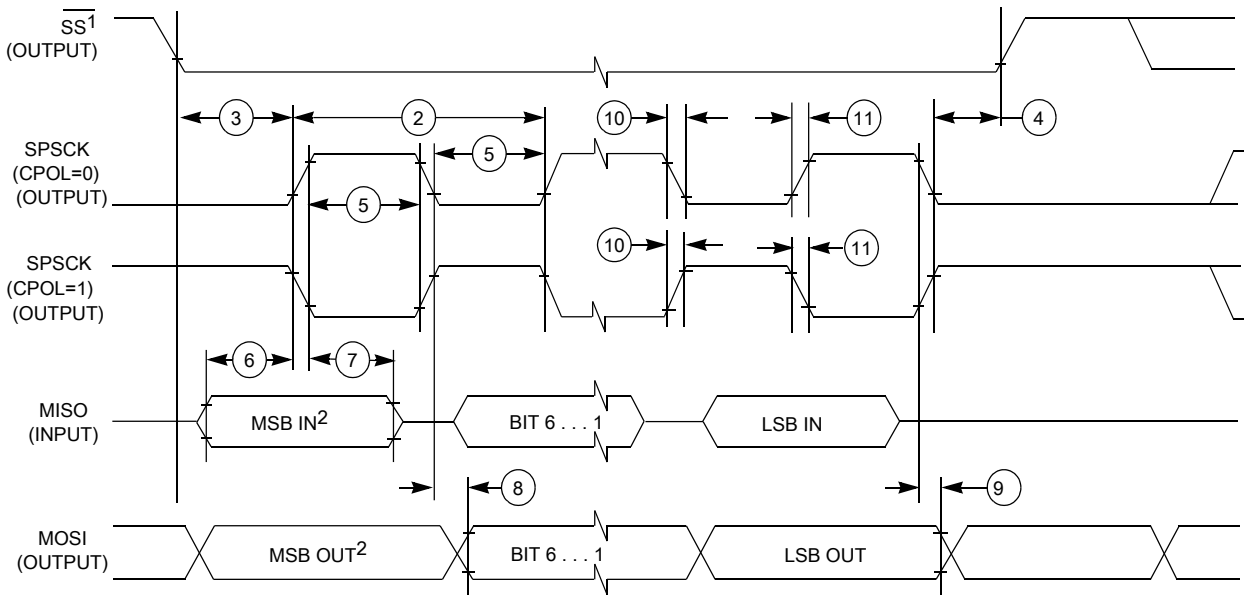
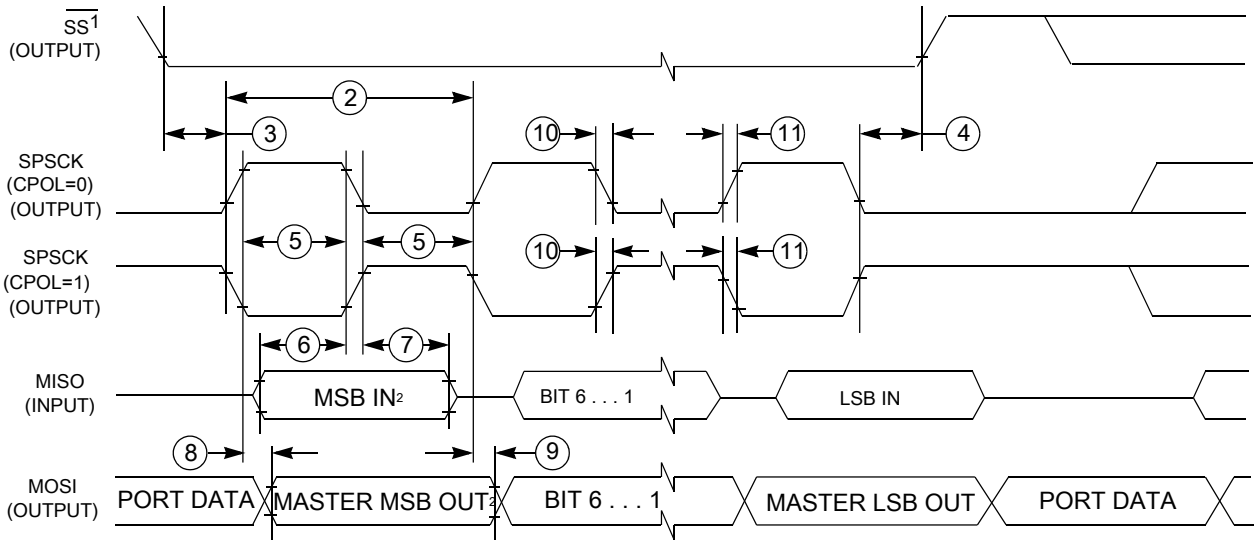


Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 25. LPSPI master mode timing (CPHA = 1)

Table 59. LPSPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—

Table continues on the next page...

Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

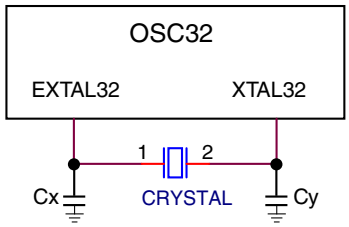


Figure 40. RTC Oscillator (OSC32) module connection – Diagram 1

Table 64. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

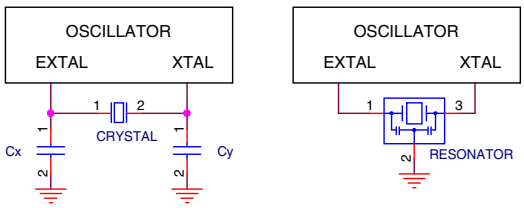


Figure 41. Crystal connection – Diagram 2

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 65. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE18, KE16, KE14
A	Key attribute	• D = Cortex-M4 with DSP • F = Cortex-M4 with DSP and FPU
FFF	Program flash memory size	• 512 = 512 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 16 = 168 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE18F512VLL16

8 Revision history

The following table provides a revision history for this document.

Table 66. Revision history

Rev. No.	Date	Substantial Changes
2	09/2016	Initial public release.