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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke16f256vll16

- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.16 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

4 Pinouts

4.1 KE1xF Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16			FTM2_CH7		FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15			FTM2_CH6		FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	ADC2_SE1	ADC2_SE1	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	ADC2_SE0	ADC2_SE0	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	ADC2_SE13	ADC2_SE13	PTE11	PWT_IN1	LPTMR0_ ALT1	FTM2_CH5		FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	ADC2_SE12	ADC2_SE12	PTE10	CLKOUT		FTM2_CH4		FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13			FTM2_FLT0			
8	5	PTE5	DISABLED		PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3	CAN0_TX	FXIO_D7	EWM_IN
9	6	PTE4	DISABLED		PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2	CAN0_RX	FXIO_D6	EWM_OUT_b

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	7	VDD	VDD	VDD							
11	8	VDDA	VDDA	VDDA							
12	9	VREFH	VREFH	VREFH							
13	—	VREFL	VREFL	VREFL							
14	—	VSS	VSS	VSS							
15	11	PTB7	EXTAL	EXTAL	PTB7	LPI2C0_SCL					
16	12	PTB6	XTAL	XTAL	PTB6	LPI2C0_SDA					
17	—	PTE14	ACMP2_IN3	ACMP2_IN3	PTE14	FTM0_FLT1		FTM2_FLT1			
18	13	PTE3	DISABLED		PTE3	FTM0_FLT0	LPUART2_ RTS	FTM2_FLT0		TRGMUX_IN6	ACMP2_OUT
19	—	PTE12	DISABLED		PTE12	FTM0_FLT3	LPUART2_TX				
20	—	PTD17	DISABLED		PTD17	FTM0_FLT2	LPUART2_RX				
21	14	PTD16	ACMP2_IN0	ACMP2_IN0	PTD16	FTM0_CH1					
22	15	PTD15	ACMP2_IN1	ACMP2_IN1	PTD15	FTM0_CH0					
23	16	PTE9	ACMP2_IN2/ DAC0_OUT	ACMP2_IN2/ DAC0_OUT	PTE9	FTM0_CH7	LPUART2_ CTS				
24	—	PTD14	DISABLED		PTD14	FTM2_CH5					CLKOUT
25	—	PTD13	DISABLED		PTD13	FTM2_CH4					RTC_CLKOUT
26	17	PTE8	ACMP0_IN3	ACMP0_IN3	PTE8	FTM0_CH6					
27	18	PTB5	DISABLED		PTB5	FTM0_CH5	LPSPI0_PCS1			TRGMUX_IN0	ACMP1_OUT
28	19	PTB4	ACMP1_IN2	ACMP1_IN2	PTB4	FTM0_CH4	LPSPI0_SOUT			TRGMUX_IN1	
29	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	FTM0_CH3	CAN0_TX				
30	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	FTM0_CH2	CAN0_RX				
31	22	PTD7	DISABLED		PTD7	LPUART2_TX		FTM2_FLT3			
32	23	PTD6	DISABLED		PTD6	LPUART2_RX		FTM2_FLT2			
33	24	PTD5	DISABLED		PTD5	FTM2_CH3	LPTMR0_ ALT2	FTM2_FLT1	PWT_IN2	TRGMUX_IN7	
34	—	PTD12	DISABLED		PTD12	FTM2_CH2	LPI2C1_HREQ			LPUART2_ RTS	
35	—	PTD11	DISABLED		PTD11	FTM2_CH1	FTM2_QD_ PHA			LPUART2_ CTS	
36	—	PTD10	DISABLED		PTD10	FTM2_CH0	FTM2_QD_ PHB				
37	—	VSS	VSS	VSS							
38	—	VDD	VDD	VDD							
39	25	PTC1	ADC0_SE9/ ACMP1_IN3	ADC0_SE9/ ACMP1_IN3	PTC1	FTM0_CH1				FTM1_CH7	
40	26	PTC0	ADC0_SE8/ ACMP1_IN4	ADC0_SE8/ ACMP1_IN4	PTC0	FTM0_CH0				FTM1_CH6	

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3		FTM1_CH5	
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2		FTM1_CH4	
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13/ ACMP2_IN4	ADC0_SE13/ ACMP2_IN4	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12/ ACMP2_IN5	ADC0_SE12/ ACMP2_IN5	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7	ADC0_SE7	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6	ADC0_SE6	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13	FTM3_CH7	FTM2_CH7				
50	—	PTC12	DISABLED		PTC12	FTM3_CH6	FTM2_CH6				
51	—	PTC11	DISABLED		PTC11	FTM3_CH5					
52	—	PTC10	DISABLED		PTC10	FTM3_CH4					
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	ADC2_SE15	ADC2_SE15	PTC9	LPUART1_TX	FTM1_FLT1			LPUART0_ RTS	
56	36	PTC8	ADC2_SE14	ADC2_SE14	PTC8	LPUART1_RX	FTM1_FLT0			LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	ADC2_SE2/ ACMP2_IN6	ADC2_SE2/ ACMP2_IN6	PTE7	FTM0_CH7	FTM3_FLT0				
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6	FTM3_FLT0	EWM_OUT_b			
63	—	PTB17	ADC2_SE3	ADC2_SE3	PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	ADC1_SE15	ADC1_SE15	PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	ADC1_SE14	ADC1_SE14	PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1	FTM3_FLT1				
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0	FTM3_FLT2				
69	44	PTD4	ADC1_SE6/ ACMP1_IN6	ADC1_SE6/ ACMP1_IN6	PTD4	FTM0_FLT3	FTM3_FLT3				
70	45	PTD3	NMI_b	ADC1_SE3	PTD3	FTM3_CH5	LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2	FTM3_CH4	LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3	FTM3_CH1	LPI2C0_SCL	EWM_IN		LPUART0_TX	

5 Electrical characteristics

5.1 Terminology and guidelines

5.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

5.3.1 Nonswitching electrical specifications

5.3.1.1 Voltage and current operating requirements

Table 27. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	
I_{ICIO}	Analog DC injection current — single pin				
	$V_{IN} < V_{SS}$ - 0.3 V (Negative current injection)	– 5	—	mA	1, 2
	$V_{IN} > V_{DD}$ + 0.3 V (Positive current injection)	—	+ 5	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	– 25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
2. Max voltage levels that I/O pins can withstand while keeping the injection current (maximum) at 5mA:
   - Max supply V_{DD} = 6.0 V for 60 s lifetime (with no switching restrictions) or for 10 hours (if device is in reset or no switching state)
   - Max I/O pin voltage = 6.5 V (at injection current ≤ 5 mA) or 7.0 V (at injection current > 5 mA)
3. Open drain outputs must be pulled to V_{DD}.

5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

Table 28. DC electrical specifications

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{DD}	I/O Supply Voltage [1] @ V_{DD} = 3.3 V	2.7	3.3	4	V	
	@ V_{DD} = 5.0 V	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage @ V_{DD} = 3.3 V	0.7 × V_{DD}	—	V_{DD} + 0.3	V	
	@ V_{DD} = 5.0 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V	

Table continues on the next page...

5.3.1.3 Voltage regulator electrical characteristics

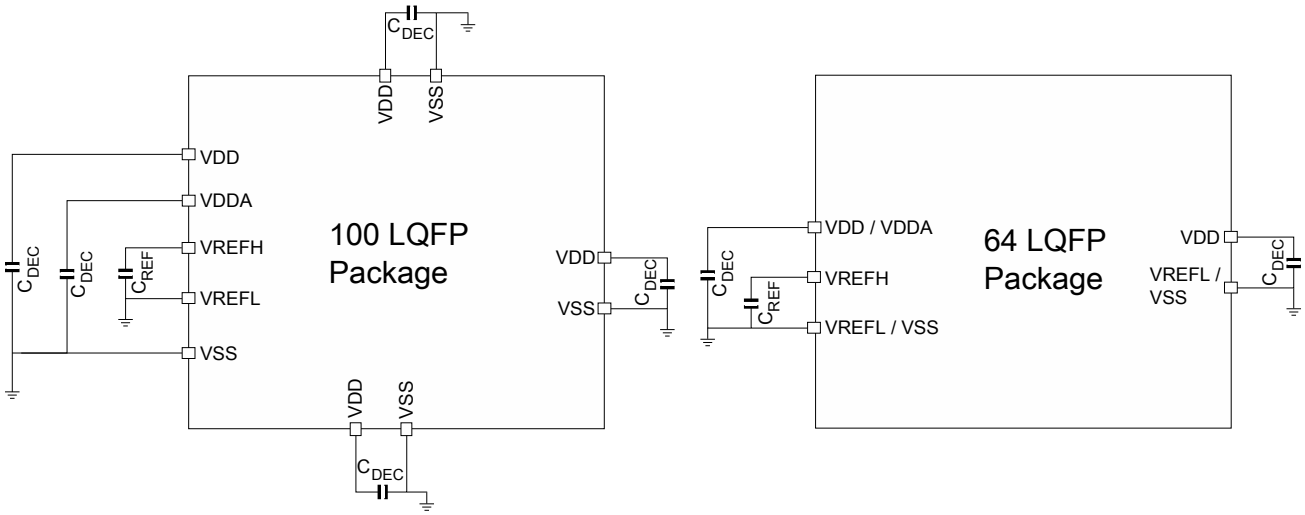

Figure 13. Pinout decoupling

Table 29. Voltage regulator electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF} [1, 2]	ADC reference high decoupling capacitance	—	100	—	nF
C_{DEC} [2, 3]	Recommended decoupling capacitance	—	100	—	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding V_{DD}/V_{SS} pins.
3. The requirement and value of of C_{DEC} will be decided by the device application requirement.

NOTE

For 64 LQFP, the external decoupling capacitor C_{DEC} must be added, and the minimum value is 100 nF.

5.3.1.4 LVR, LVD and POR operating requirements

Table 30. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and Falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVRX}	LVRX falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVRX_HYST}	LVRX hysteresis	—	45	—	mV	1
V_{LVRX_LP}	LVRX falling threshold (VLPS/VLPR modes)	1.97	2.12	2.44	V	
$V_{LVRX\_LP\_HYST}$	LVRX hysteresis (VLPS/VLPR modes)	—	40	—	mV	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.88	3	V	

Table continues on the next page...

Table 32. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 ℃	—	39.87	40.50	
				105 ℃	—	46.03	51.64	
		IRC48M	Running CoreMark in Flash in **Compute Operation** mode. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	14.02	14.65	
				105 ℃	—	19.76	25.37	
		IRC48M	Running CoreMark in Flash all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	16.83	17.46	
				105 ℃	—	22.64	28.25	
		IRC48M	Running CoreMark in Flash, all peripheral clock enabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	19.70	20.33	
				105 ℃	—	25.59	31.20	
		IRC48M	Running While(1) loop in Flash, all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	17.22	17.85	
				105 ℃	—	23.23	28.84	
VLPR	I_{DD_VLPR}	IRC8M	Very Low Power Run Core Mark in Flash in **Compute Operation** mode. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.52	1.63	mA
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.73	1.84	
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.95	2.06	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.77	1.88	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.96	2.07	
		IRC2M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled.	25 ℃	—	1.19	1.30	

Table continues on the next page...

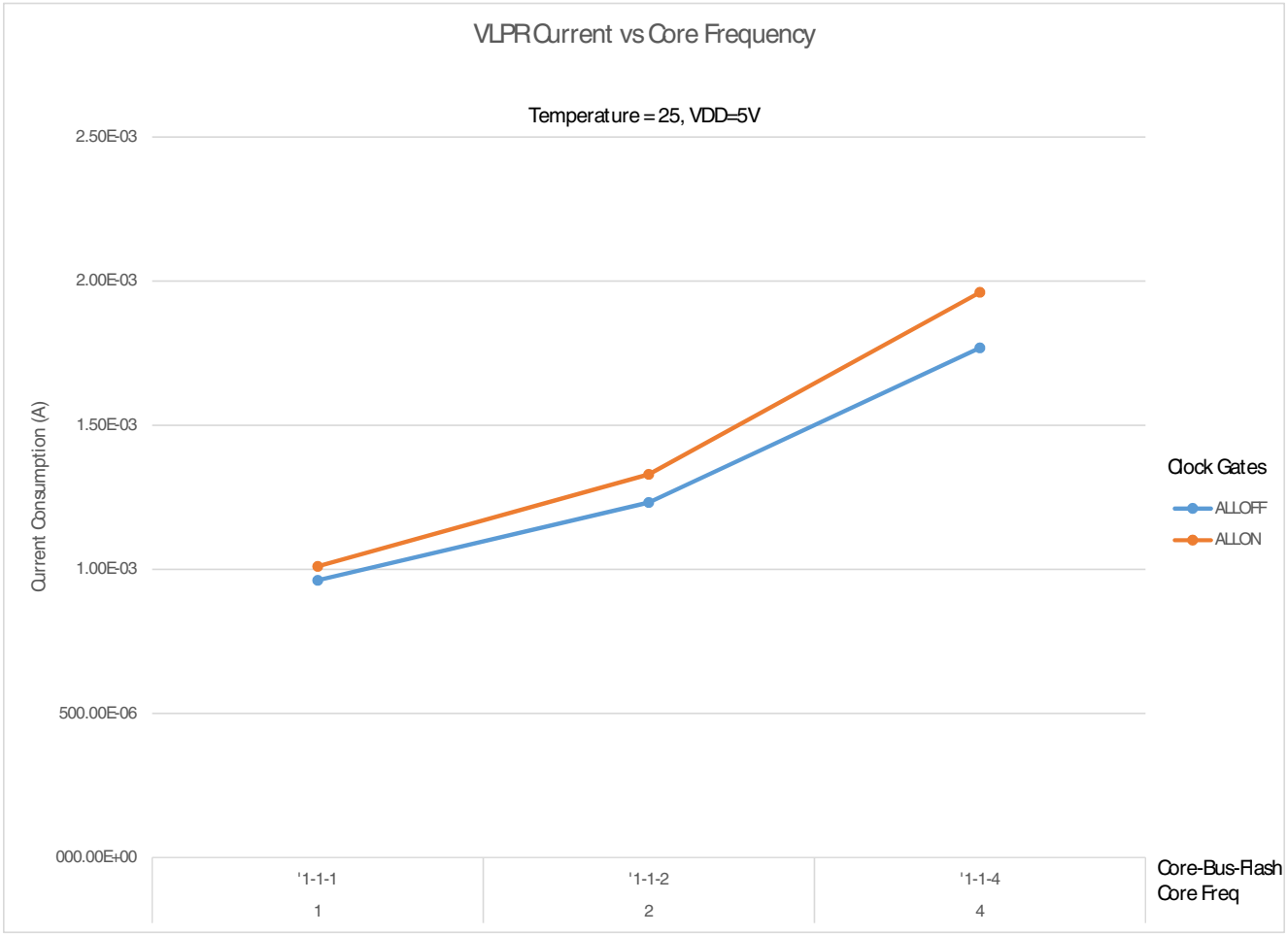

Figure 15. VLPR mode supply current vs. core frequency

5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 39. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	60	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	42	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	24	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	12	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 40. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	57	°C/W

Table continues on the next page...

Table 41. External Oscillator electrical specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL32 pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL32 pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL32 load capacitance	—	—	—		2
C_2	XTAL32 load capacitance	—	—	—		2
R_F	Feedback resistor	—	—	—	MΩ	
R_S	Series resistor	—	—	—	MΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)	—	0.6	—	V	3

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 42. External Oscillator electrical specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current — low-gain mode (low-power mode) (HGO=0)					1
	4 MHz	—	200	—	µA	
	8 MHz	—	300	—	µA	
	16 MHz	—	1.2	—	mA	
	24 MHz	—	1.6	—	mA	
	32 MHz	—	2	—	mA	
	40 MHz	—	2.6	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	4 MHz	—	1	—	mA	
	8 MHz	—	1.2	—	mA	
	16 MHz	—	3.5	—	mA	
	24 MHz	—	5	—	mA	
	32 MHz	—	5.5	—	mA	
	40 MHz	—	6	—	mA	
g_{mXOSC}	Fast external crystal oscillator transconductance					
	32 kHz, Low Frequency Range, High Gain (32 kHz)	15	—	45	µA / V	
	High Frequency Range 1 (4-8 MHz)	2.2	—	9.7	mA / V	
	High Frequency Range 2 (8-40 MHz)	16		37	mA / V	
V_{EXTAL}	EXTAL input voltage — external clock mode	0	—	V_{DD}	V	

Table continues on the next page...

Table 44. External Oscillator frequency specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode	32	—	40	kHz	
f_{osc_me}	Oscillator crystal or resonator frequency — Medium Frequency	1	—	8	MHz	
f_{osc_hi}	Oscillator crystal or resonator frequency — High Frequency	8	—	32		
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz Low Frequency, High-Gain Mode	—	500	—	ms	1
	Crystal startup time — 8 MHz High Frequency, Low-Power Mode	—	1.5	—		
	Crystal startup time — 8 MHz High Frequency, High-Gain Mode	—	2.5	—		
	Crystal startup time — 40 MHz High Frequency, Low-Power Mode	—	2	—		
	Crystal startup time — 40 MHz High Frequency, High-Gain Mode	—	2.5	—		

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

5.4.2.2 System Clock Generation (SCG) specifications

5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 45. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	Fast internal reference frequency Trim range = 00 range = 01 (Note: 52/56 MHz are not trimmed) range = 10 (Note: 52/56 MHz are not trimmed) Trim range = 11	—	48 52 56 60	—	MHz
I_{VDD}	Supply current	—	400	500	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	F_{IRC}× (1-0.3)	—	F_{IRC}× (1+0.3)	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	±0.5	±1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		—	3	µs[2]
T_{JIT}	Period jitter (RMS)	—	35	150	ps

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.1.2 Flash timing specifications — commands

Table 50. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk64k}$	• 64 KB data flash	—	—	0.5	ms	
$t_{rd1blk512k}$	• 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk64k}$	• 64 KB data flash	—	55	475	ms	
$t_{ersblk512k}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	500	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	500	4200	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
$t_{pgmpart64k}$	• 64 KB EEPROM backup	—	71	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	µs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram48k}$	• 48 KB EEPROM backup	—	1.0	1.5	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr8b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
	16-bit write to FlexRAM execution time:					

Table continues on the next page...

Table 50. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr16b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	
$t_{eewr32b48k}$	• 48 KB EEPROM backup	—	720	2125	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 51. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.1.4 Reliability specifications

Table 52. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2

Table continues on the next page...

Table 52. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree2k}$	• EEPROM backup to FlexRAM ratio = 2,048	20 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

5.4.5.1.1 12-bit ADC operating conditions

Table 53. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	3
V_{REFL}	ADC reference voltage low		– 100	0	100	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance		—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	

Table continues on the next page...

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

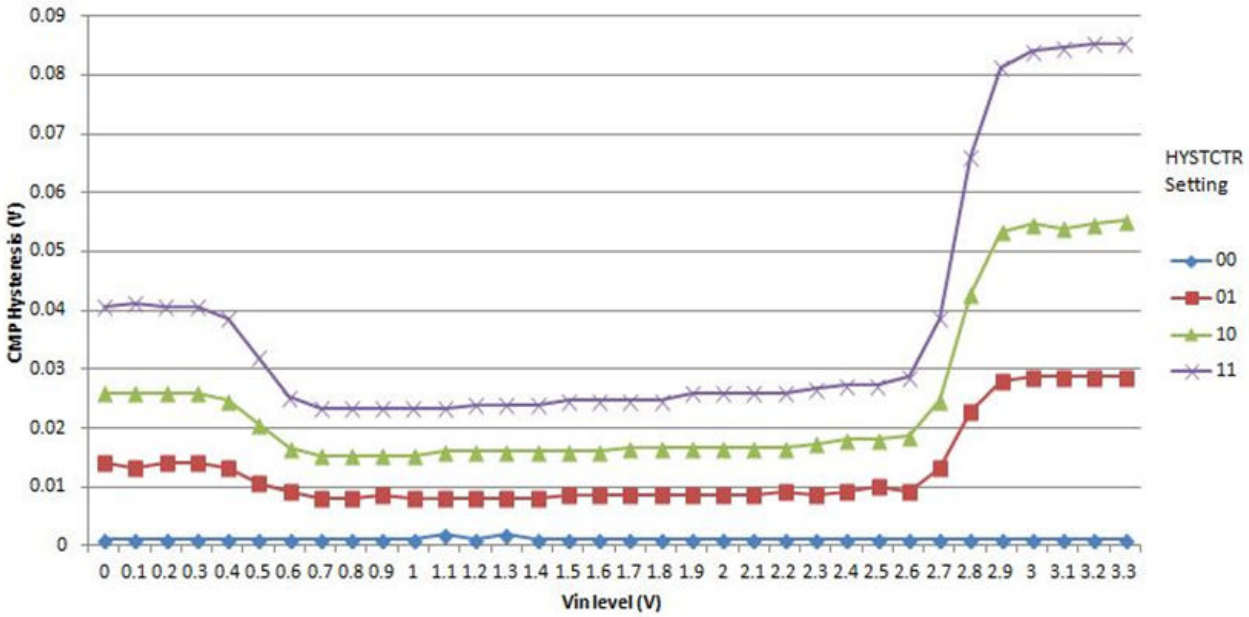

Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

Table 57. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode	—	—	5	µs	1
$t_{CCDACHP}$	Code-to-code settling time (0xBF8 to 0xC08) — high-power mode	—	0.7	—	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-power mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-power mode, no load, DAC set to 0xFFF	V_{DACR} – 100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high-power mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio					
	High-power mode, code set to 3FF or BFF		68		dB	5
	Low-power mode, code set to 3FF or BFF		60			
T_{CO}	Temperature coefficient offset voltage	—	5	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	1 0.05	1.5 0.12	— —	V/µs	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
4. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV
5. DAC reference to VREFH (DACREF_1)
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

5.4.6 Communication interfaces

5.4.6.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

NOTE

High drive pin should be used for fast bit rate.

Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

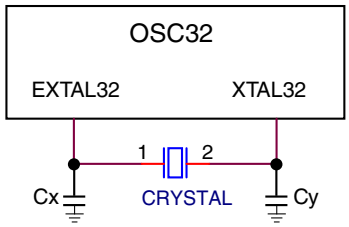

Figure 40. RTC Oscillator (OSC32) module connection – Diagram 1

Table 64. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

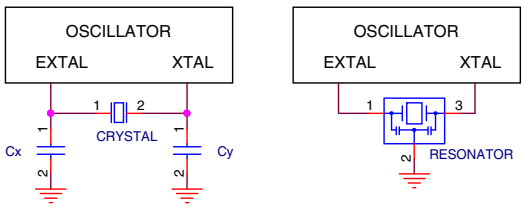

Figure 41. Crystal connection – Diagram 2