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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	89
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke16f512vll16

- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.16 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

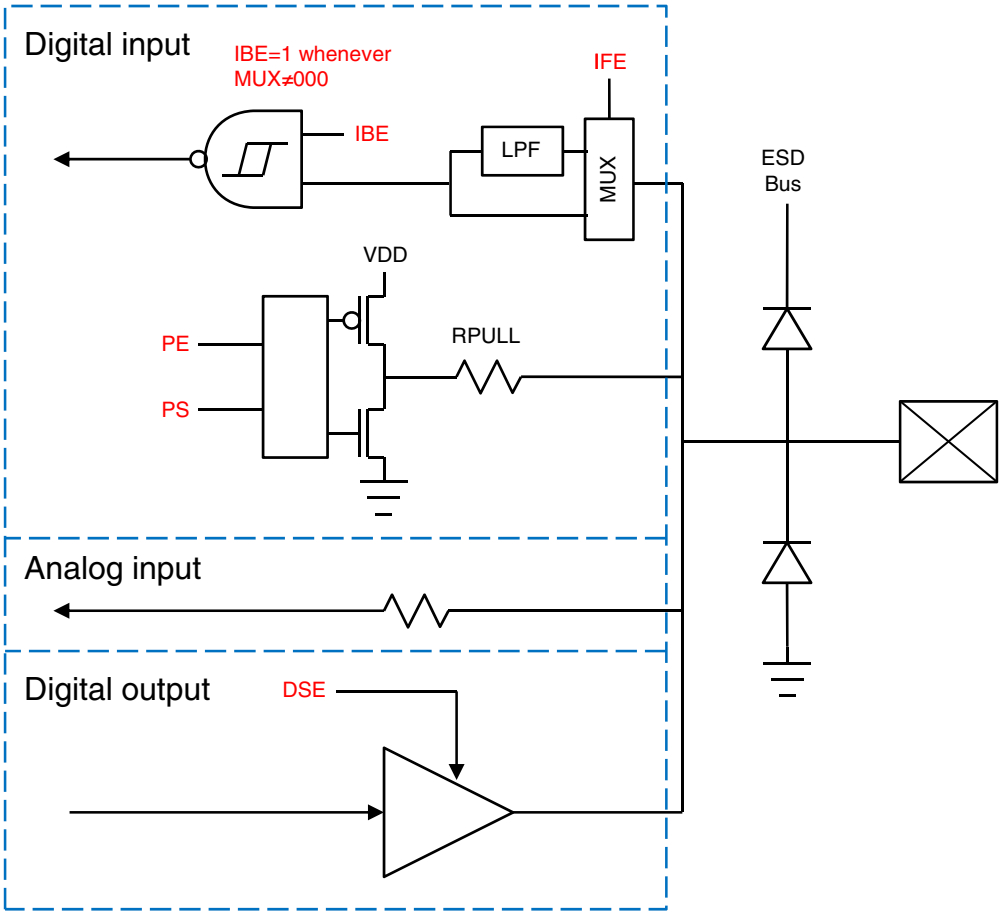


Figure 5. I/O simplified block diagram

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

4.2 Port control and interrupt summary

The following table provides more information regarding the Port Control and Interrupt configurations.

Table 6. Ports summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull select control	Yes	Yes	Yes	Yes	Yes
Pull select at reset	PTA4/PTA5=Pull up, Others=No	No	PTC5=Pull up, Others=No	PTD3=Pull up, Others=No	No
Pull enable control	Yes	Yes	Yes	Yes	Yes
Pull enable at reset	PTA4/ PTA5=Enabled; Others=Disabled	Disabled	PTC4/ PTC5=Enabled; Others=Disabled	PTD3=Enabled; Others=Disabled	Disabled
Passive filter enable control	PTA5=Yes; Others=No	No	No	PTD3=Yes; Others=No	No
Passive filter enable at reset	PTA5=Enabled; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable control	Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive strength enable control	No	PTB4/PTB5 only	No	PTD0/PTD1/ PTD15/PTD16 only	PTE0/PTE1 only
Drive strength enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Pin mux control	Yes	Yes	Yes	Yes	Yes
Pin mux at reset	PTA4/PTA5/ PTA10=ALT7; Others=ALT0	ALT0	PTC4/PTC5=ALT7; Others=ALT0	PTD3=ALT7; Others=ALT0	ALT0
Lock bit	Yes	Yes	Yes	Yes	Yes
Interrupt and DMA request	Yes	Yes	Yes	Yes	Yes
Digital glitch filter	Yes	Yes	Yes	Yes	Yes

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

Table 16. ACMP*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*n*_IN[6:0]	IN[6:0]	Analog voltage inputs	I
ACMP*n*_OUT	CMPO	Comparator output	O

4.3.5 Timer Modules

Table 17. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALT*n*	Pulse Counter Input pin	I

Table 18. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or 32 kHz clock	O

Table 19. FTM*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*n*_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM*n*_FLT[3:0]	FAULTj	Fault input (j), where j can be 3-0	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

4.3.6 Communication Interfaces

Table 20. CAN*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CAN*n*_RX	CAN Rx	CAN Receive Pin	I
CAN*n*_TX	CAN Tx	CAN Transmit Pin	O

NOTE

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 32. Power consumption operating behaviors

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
HSRUN	I_{DD_HSRUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	44.50	46.36	mA
				105 °C	—	51.88	59.46	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	50.49	52.35	
				105 °C	—	58.31	65.89	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	60.51	62.37	
				105 °C	—	68.62	76.20	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	52.74	54.60	
				105 °C	—	60.76	68.34	
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	62.48	64.34	
				105 °C	—	70.75	78.33	
RUN	I_{DD_RUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	29.04	29.67	mA
				105 °C	—	34.82	40.43	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	33.29	33.92	
				105 °C	—	39.08	44.69	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	41.00	41.63	
				105 °C	—	47.00	52.61	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	34.59	35.22	
				105 °C	—	40.68	46.29	

Table continues on the next page...

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

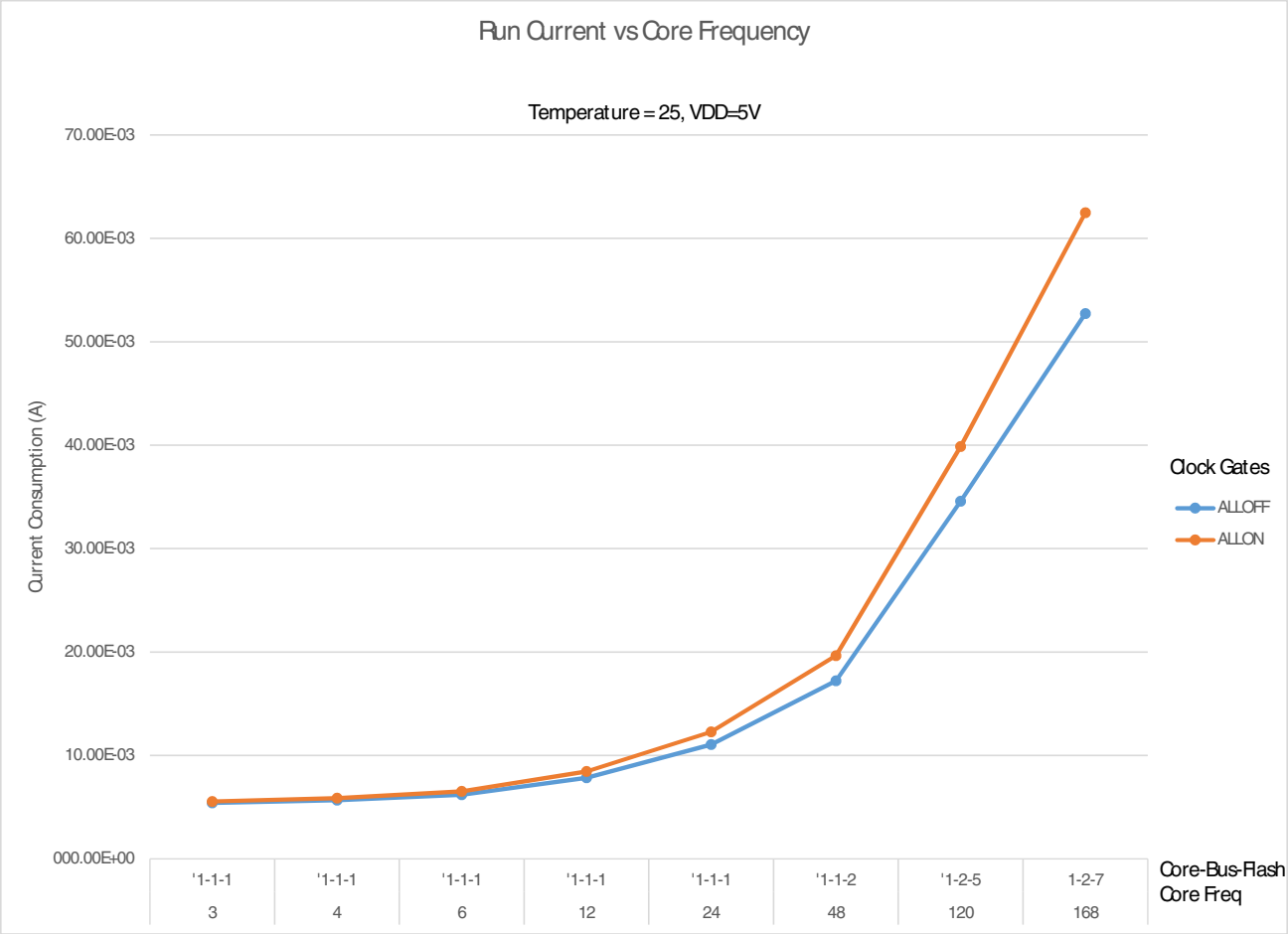


Figure 14. Run mode supply current vs. core frequency

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 33. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

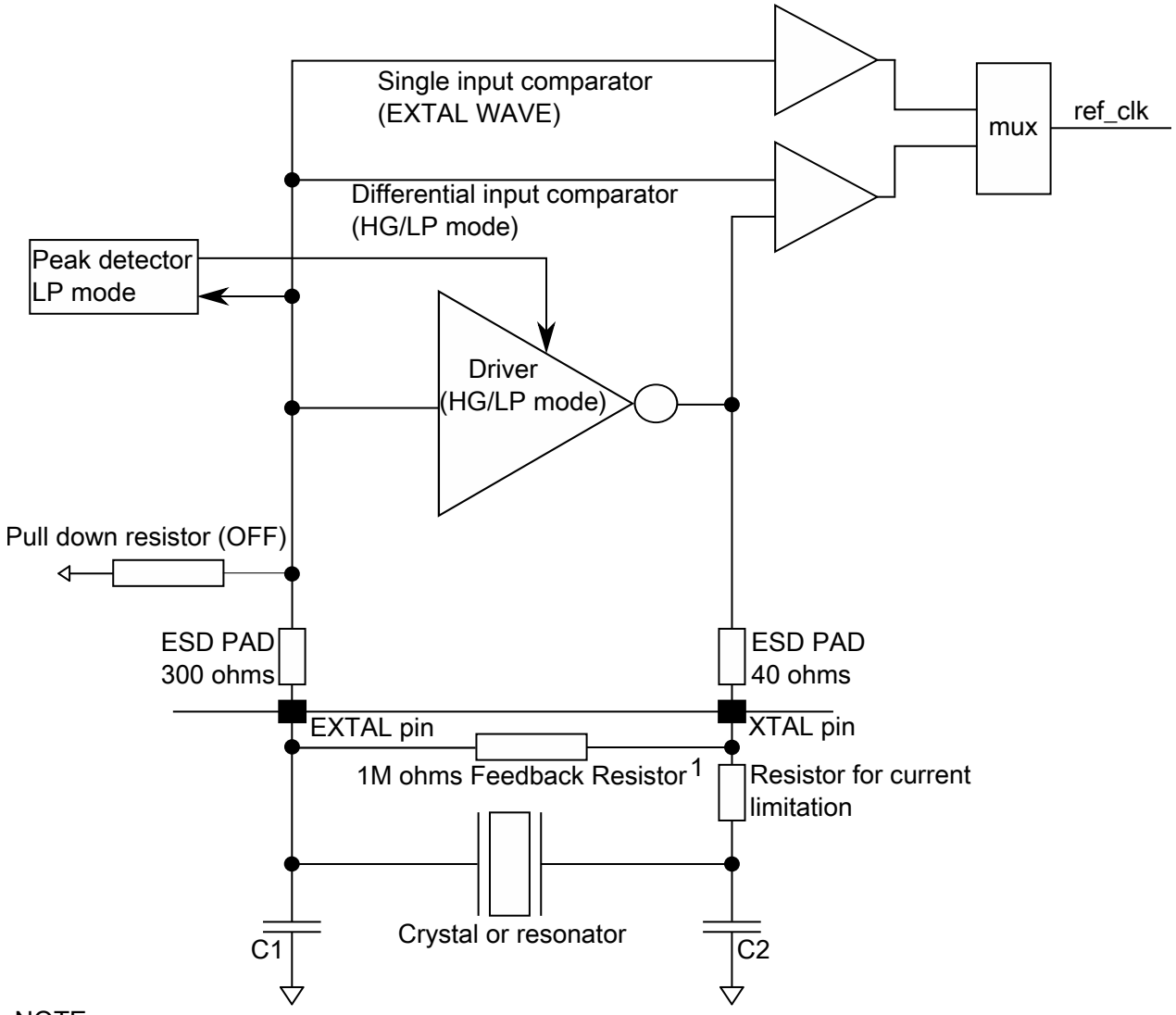
5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 34. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus clock	—	84	MHz	

Table continues on the next page...



NOTE:

1. 1M Feedback resistor is needed only for HG mode.

Figure 18. Oscillator connections scheme (OSC)

NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

Table 41. External Oscillator electrical specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current	—	25	—	µA	1
g_{mXOSC}	Oscillator transconductance	6	—	9	µA/V	
V_{EXTAL}	EXTAL32 input voltage — external clock mode	0	—	3.6	V	

Table continues on the next page...

Table 48. PLL electrical specifications (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	VCO @ 150 MHz (F_{pll_ref} = 12 MHz, VDIV multiplier = 25, PRDIV divide = 2)	—	2.8	—	mA
	VCO @ 300 MHz (F_{pll_ref} = 12 MHz, VDIV multiplier = 50, PRDIV divide = 2)	—	3.6	—	mA
J_{cyc_pll}	PLL Period Jitter (RMS)[2]				
	at F_{vco} 180 MHz	—	120	—	ps
	at F_{vco} 360 MHz	—	75	—	ps
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)[2]				
	at F_{vco} 180 MHz	—	1350	—	ps
	at F_{vco} 360 MHz	—	600	—	ps
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{pll_lock}	Lock detector detection time[3]	—	—	100×10^{-6} + 1075(1/F_{pll_ref})	s

1. Excludes any oscillator currents that are also consuming power while PLL is in operation.
2. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
3. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, thisspecification assumes it is already running.

5.4.3 Memories and memory interfaces

5.4.3.1 Flash memory module (FTFE) electrical specifications

This section describes the electrical characteristics of the flash memory module (FTFE).

5.4.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 49. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk64k}$	Erase Flash Block high-voltage time for 64 KB	—	52	452	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

Table 53. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
R_{AS}	Analog source resistance (external)		—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency		2	40	50	MHz	5, 6
C_{rate}	ADC conversion rate	No ADC hardware averaging[7] Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	8

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. Clock and compare cycle need to be set according the guidelines in the block guide.
6. ADC conversion will become less reliable above maximum frequency.
7. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
8. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

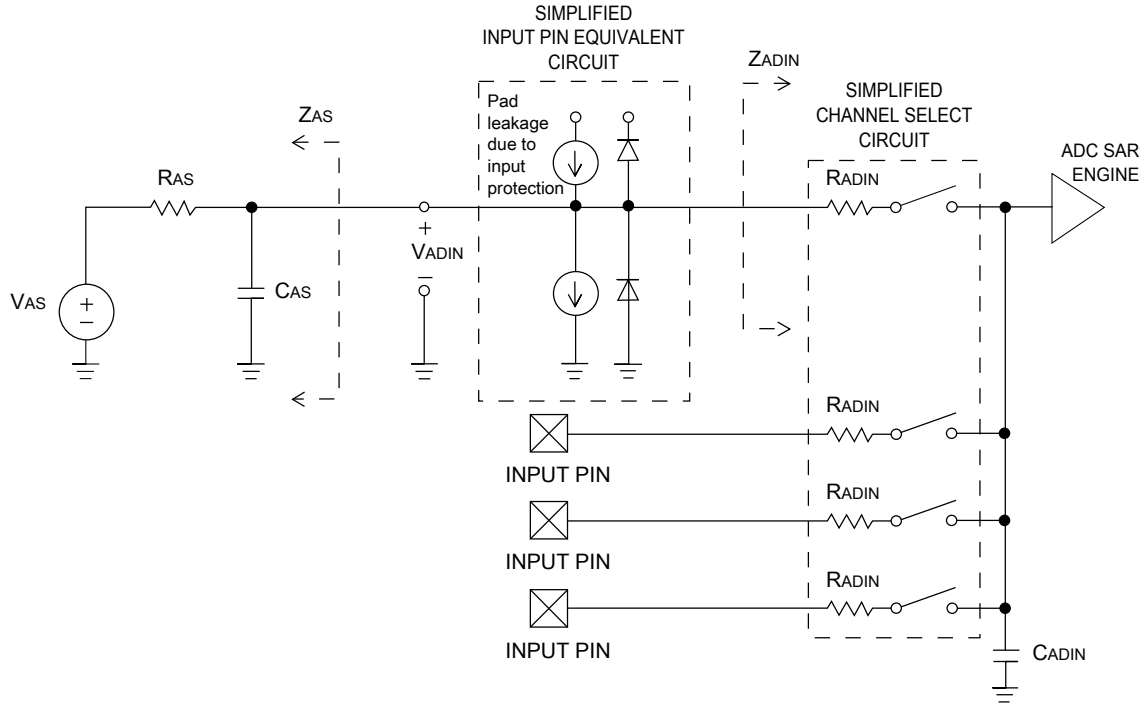


Figure 19. ADC input impedance equivalency diagram

5.4.5.1.2 12-bit ADC electrical characteristics

NOTE

All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

For ADC signals adjacent to VDD/VSS or the XTAL pins some degradation in the ADC performance may be observed.

NOTE

All values guarantee the performance of the ADC for the multiple ADC input channel pins. When using the ADC to monitor the internal analogue parameters, please assume minor degradation.

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
I_{DDA_ADC}	Supply current at 2.7 to 5.5 V		621	658 µA @ 5 V	696	mA	4

Table continues on the next page...

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.56	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.95	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.40	LSB[5]	V_{ADIN} = V_{DDA}[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.14	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temperature sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temperatue sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

5.4.5.2 CMP with 8-bit DAC electrical specifications

Table 55. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit
V_{DD}	Supply voltage	2.7	—	5.5	V
I_{DDHS}	Supply current, High-speed mode[2]				µA
	within ambient temperature range	—	145	200	
I_{DDLS}	Supply current, Low-speed mode[2]				µA
	within ambient temperature range	—	5	10	
V_{AIN}	Analog input voltage	0	0 - V_{DDX}	V_{DDX}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	within ambient temperature range	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	within ambient temperature range	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[3]				ns
	within ambient temperature range	—	30	200	
t_{DLSB}	Propagation delay, Low-speed mode[3]				µs
	within ambient temperature range	—	0.5	2	
t_{DHSS}	Propagation delay, High-speed mode[4]				ns
	within ambient temperature range	—	70	400	
t_{DLSS}	Propagation delay, Low-speed mode[4]				µs
	within ambient temperature range	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode [3]				µs
	within ambient temperature range	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[3]				µs
	within ambient temperature range	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0 (V_{AIO})				mV
	within ambient temperature range	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	within ambient temperature range	—	16	53	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	within ambient temperature range	—	11	30	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	within ambient temperature range	—	32	90	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	within ambient temperature range	—	22	53	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV

Table continues on the next page...

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

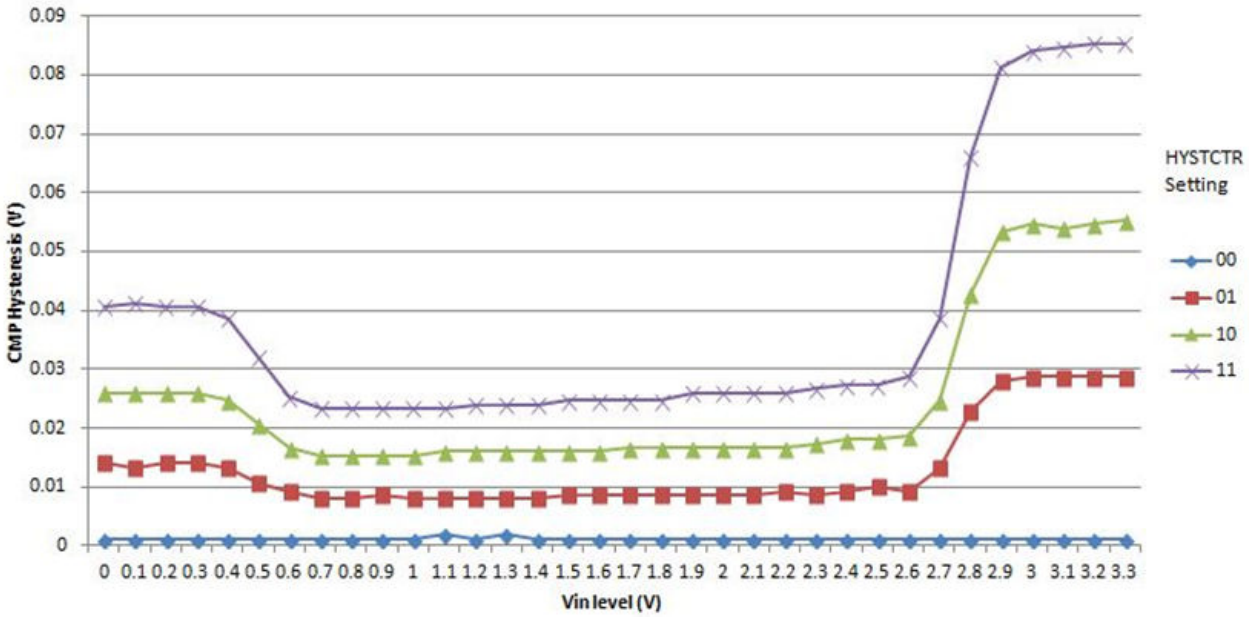


Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

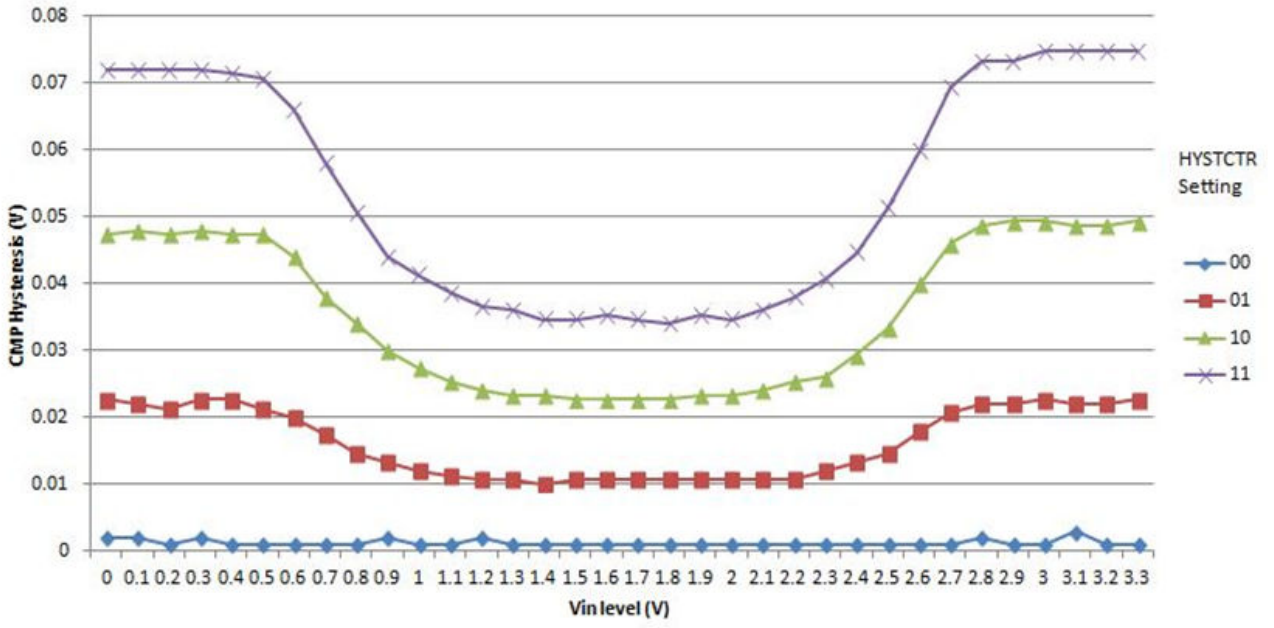


Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

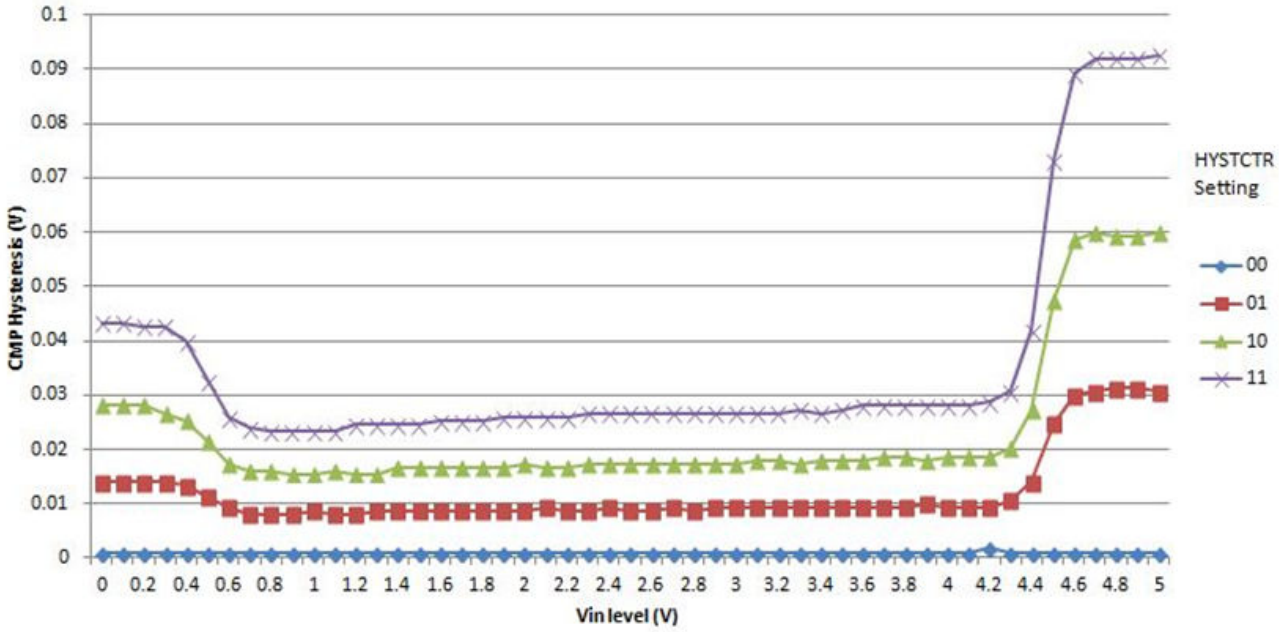


Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

NOTE

High drive pin should be used for fast bit rate.

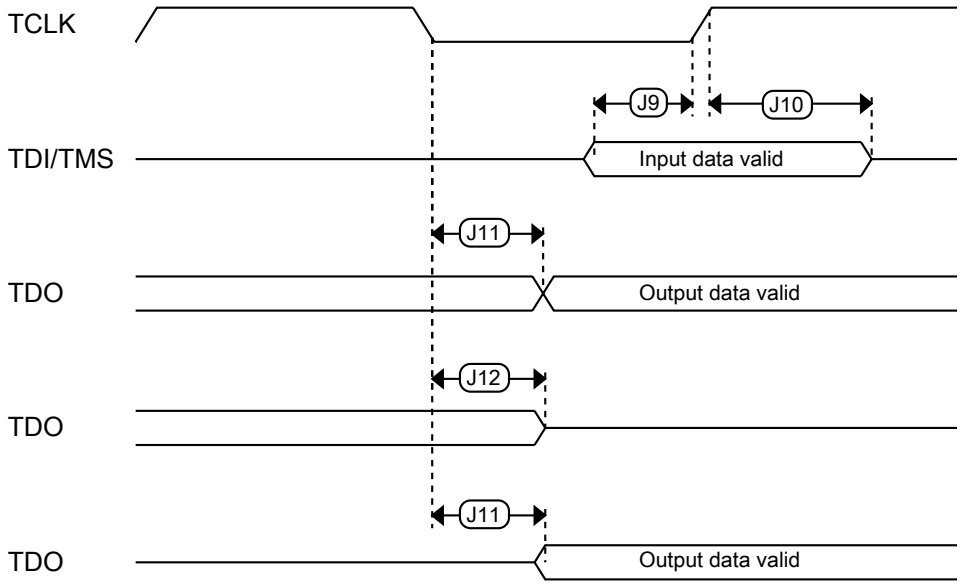


Figure 32. Test Access Port timing

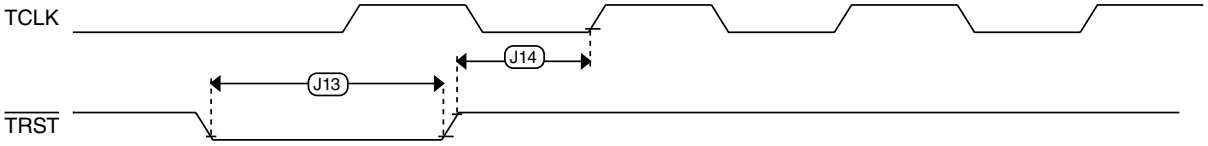


Figure 33. $\overline{\text{TRST}}$ timing

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

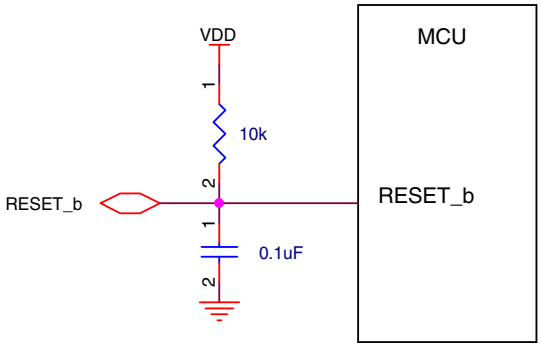


Figure 36. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

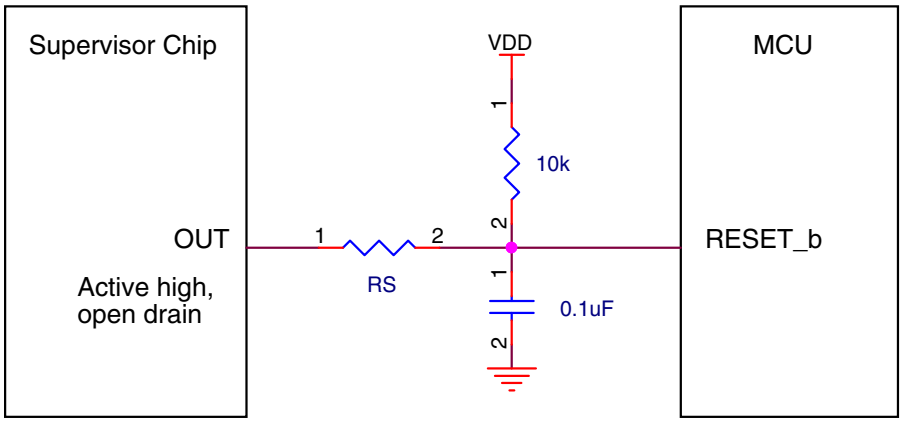


Figure 37. Reset signal connection to external reset chip

- NMI pin

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 65. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE18, KE16, KE14
A	Key attribute	• D = Cortex-M4 with DSP • F = Cortex-M4 with DSP and FPU
FFF	Program flash memory size	• 512 = 512 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 16 = 168 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE18F512VLL16

8 Revision history

The following table provides a revision history for this document.

Table 66. Revision history

Rev. No.	Date	Substantial Changes
2	09/2016	Initial public release.