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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, FlexIO, I²C, SPI, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	58
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	68K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke18f256vlh16

Clock interfaces

- 3 - 40 MHz fast external oscillator (OSC)
- 32 kHz slow external oscillator (OSC32)
- 48 - 60 MHz high-accuracy (up to 1%) fast internal reference clock (FIRC) for high-speed run
- 8 MHz / 2 MHz high-accuracy (up to 3%) slow internal reference clock (SIRC) for low-speed run
- 128 kHz low power oscillator (LPO)
- Phased lock loop (PLL)
- Up to 60 MHz DC external square wave input clock
- System clock generator (SCG)
- Real time counter (RTC)

Power management

- Low-power ARM Cortex-M4 core with excellent energy efficiency
- Power management controller (PMC) with multiple power modes: HSRun, Run, Wait, Stop, VLPR, VLPW and VLPS
- Supports clock gating for unused modules, and specific peripherals remain working in low power modes
- POR, LVD/LVR

Operating Characteristics

- Voltage range: 2.7 to 5.5 V
- Ambient temperature range: –40 to 105 °C

Connectivity and communications interfaces

- TriggerMUX: for module inter-connectivity
- 3× low-power universal asynchronous receiver/ transmitter (LPUART) modules with DMA support and working at Stop mode
- 2 low-power serial peripheral interface (LPSPI) modules with DMA support and working at Stop mode
- 2× low-power inter-integrated circuit (LPI2C) modules with DMA support and working at Stop mode
- Up to 2 ×FlexCAN modules, with flexible message buffers and mailboxes
- FlexIO module for flexible and high performance serial interfaces emulation

Debug functionality

- Serial Wire JTAG Debug Port (SWJ-DP) combines
- Debug Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Test Port Interface Unit (TPIU)
- Flash Patch and Breakpoints (FPB)

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KE1xF512PB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KE1xFP100M168SF0RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KE1xFP100M168SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_E_0N79P [1]
Package drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W 64-LQFP: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory			Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels	FlexCAN
MKE18F512VLL16	MKE18F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	2
MKE18F512VLH16	MKE18F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	2
MKE18F256VLL16	MKE18F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	2
MKE18F256VLH16	MKE18F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	2
MKE16F512VLL16	MKE16F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	1
MKE16F512VLH16	MKE16F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	1
MKE16F256VLL16	MKE16F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	1
MKE16F256VLH16	MKE16F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	1
MKE14F512VLL16	MKE14F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	0
MKE14F512VLH16	MKE14F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	0
MKE14F256VLL16	MKE14F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	0
MKE14F256VLH16	MKE14F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	0

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device.

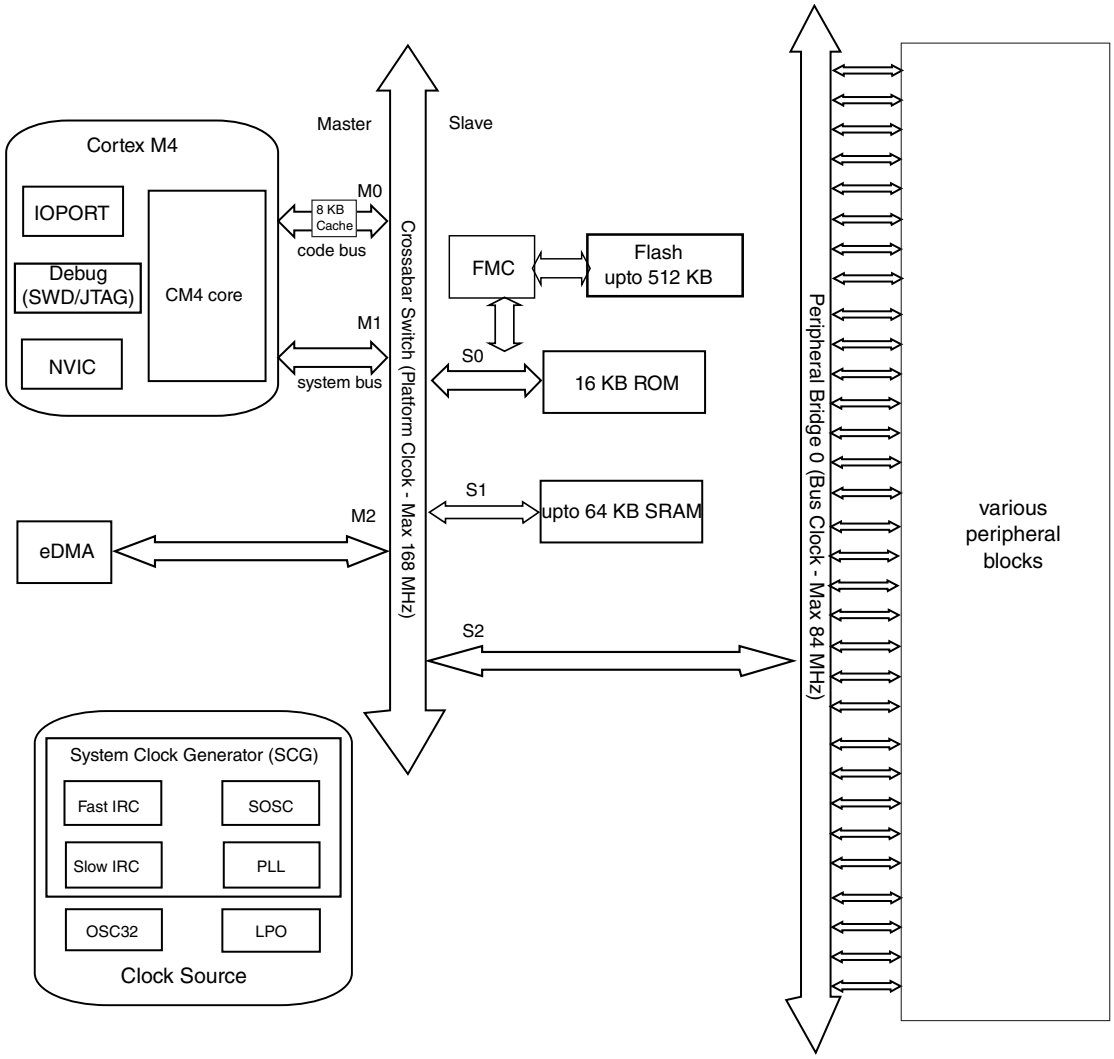

Figure 2. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

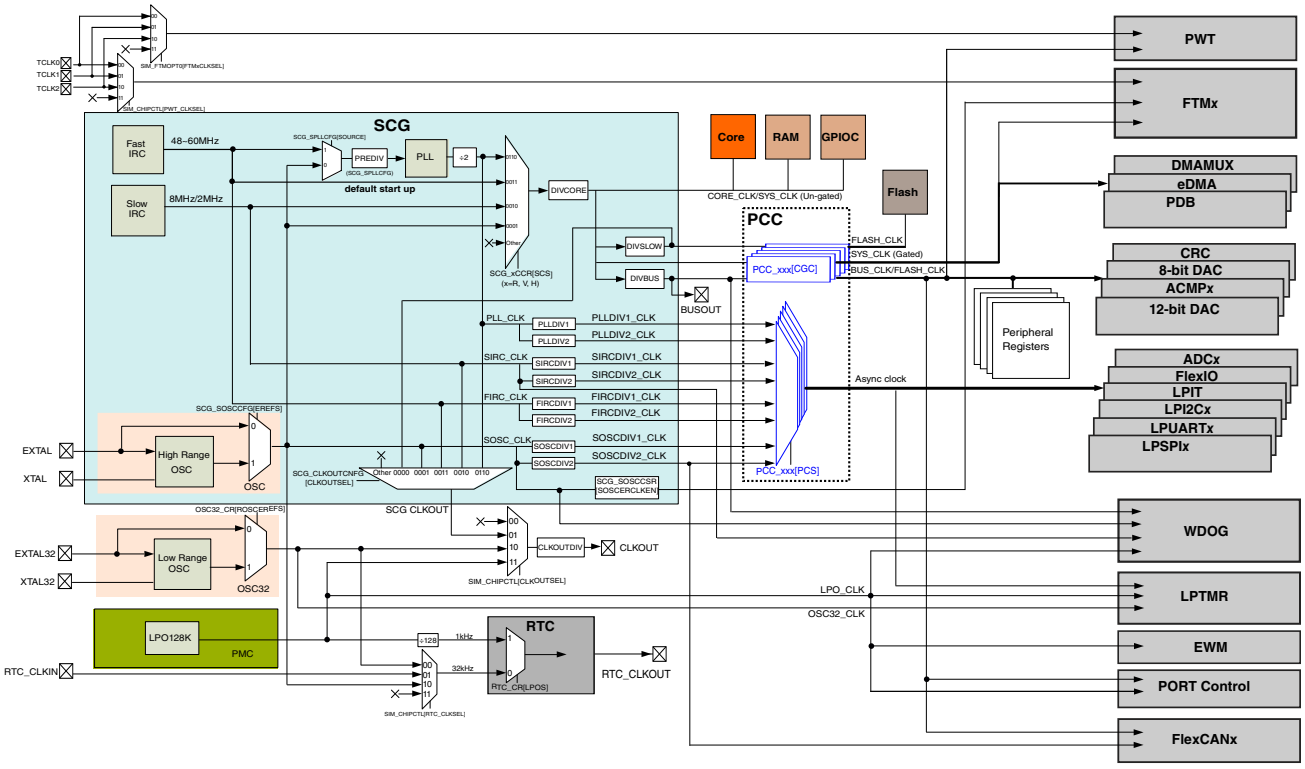

Figure 4. Clocking block diagram

2.1.7 Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD/JTAG port cannot access the memory resources of the MCU.

External interface	Security	Unsecure
SWD/JTAG port	Can't access memory source by SWD/ JTAG interface	the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command

2.1.7.1 Flash Access Control (FAC)

The FAC is a native or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these

2.2.3 ADC

This device contains three 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 16 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 Vin to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources

Each FlexCAN module contains 16 message buffers. Each message buffer is 16 bytes.

The FlexCAN module has the following features:

- Flexible mailboxes of zero to eight bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Remote request frames may be handled automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability

4.3.1 Core Modules

Table 7. JTAG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	JTAG_TMS/ SWD_DIO	JTAG Test Mode Selection	I/O
JTAG_TCLK	JTAG_TCLK/ SWD_CLK	JTAG Test Clock	I
JTAG_TDI	JTAG_TDI	JTAG Test Data Input	I
JTAG_TDO	JTAG_TDO/ TRACE_SWO	JTAG Test Data Output	O
JTAG_TRST_b	JTAG_TRST_b	JTAG Reset	I

Table 8. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_CLK	JTAG_TCLK/ SWD_CLK	Serial Wire Clock	I
SWD_DIO	JTAG_TMS/ SWD_DIO	Serial Wire Data	I/O

Table 9. TPIU Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_SWO	JTAG_TDO/ TRACE_SWO	Trace output data from the ARM CoreSight debug block over a single pin	O

4.3.2 System Modules

Table 10. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	I
RESET_b	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

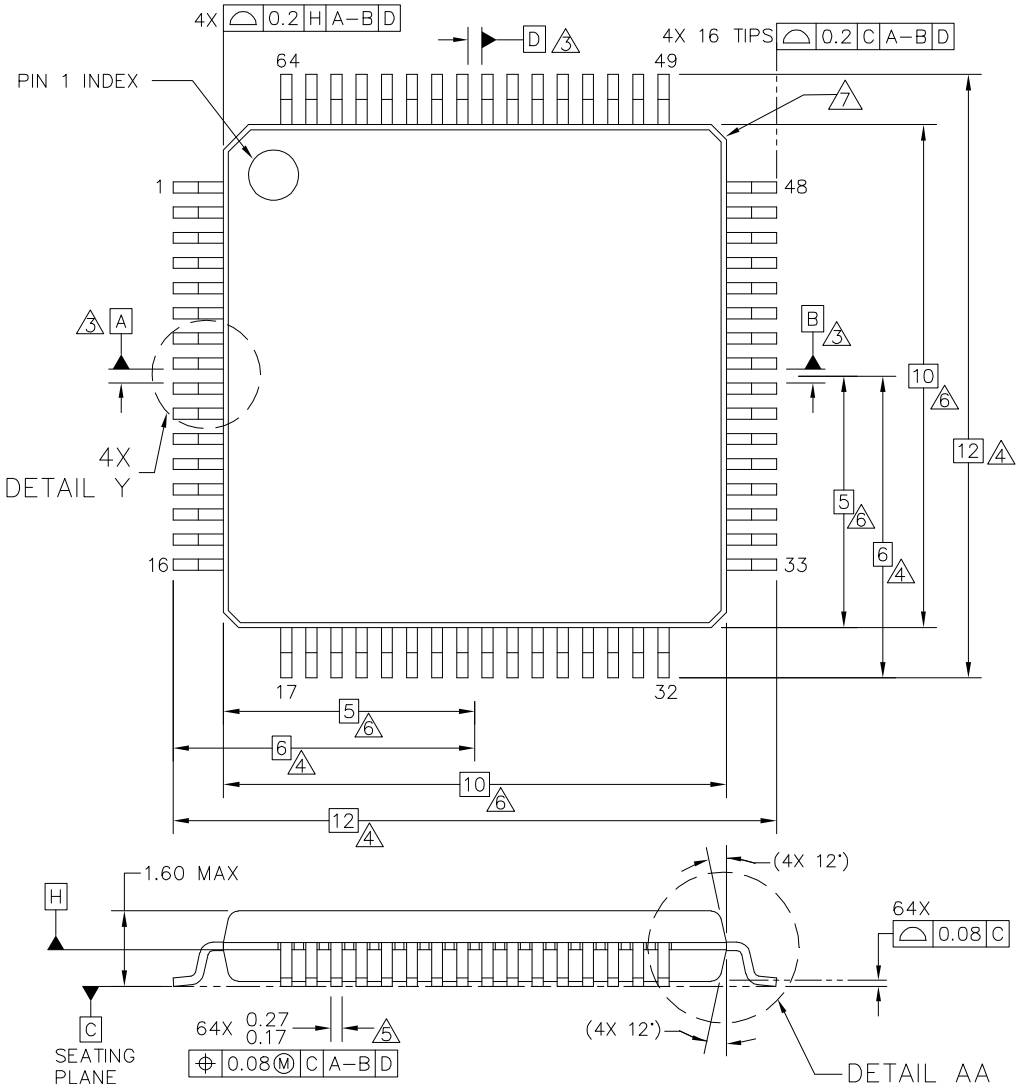

Figure 11. 64-pin LQFP package dimensions 1

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 6000	6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature upper limit	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Table 26. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	2.7	5.5	V
I_{DD}	Digital supply current	—	80	mA
V_{IO}	IO pin input voltage	V_{SS} – 0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

5.3 General

NOTE

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 32. Power consumption operating behaviors

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
HSRUN	I_{DD_HSRUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	44.50	46.36	mA
				105 °C	—	51.88	59.46	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	50.49	52.35	
				105 °C	—	58.31	65.89	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	60.51	62.37	
				105 °C	—	68.62	76.20	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	52.74	54.60	
				105 °C	—	60.76	68.34	
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	62.48	64.34	
				105 °C	—	70.75	78.33	
RUN	I_{DD_RUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	29.04	29.67	mA
				105 °C	—	34.82	40.43	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	33.29	33.92	
				105 °C	—	39.08	44.69	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	41.00	41.63	
				105 °C	—	47.00	52.61	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	34.59	35.22	
				105 °C	—	40.68	46.29	

Table continues on the next page...

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 33. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 34. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus clock	—	84	MHz	

Table continues on the next page...

Table 34. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FLASH}	Flash clock	—	25	MHz	
Normal RUN mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	50	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	
$f_{FlexCAN}$	FlexCAN clock	—	4	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

5.3.2.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

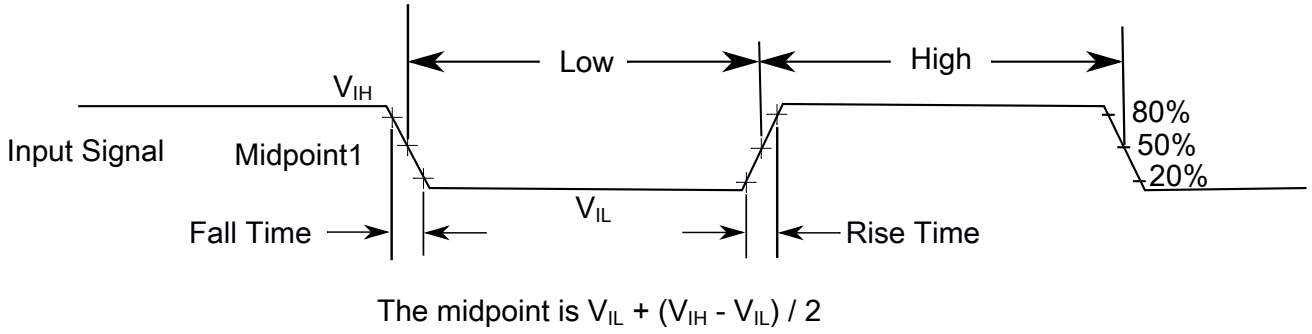

Figure 16. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Normal drive strength

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.1.2 Flash timing specifications — commands

Table 50. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk64k}$	• 64 KB data flash	—	—	0.5	ms	
$t_{rd1blk512k}$	• 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk64k}$	• 64 KB data flash	—	55	475	ms	
$t_{ersblk512k}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	500	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	500	4200	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
$t_{pgmpart64k}$	• 64 KB EEPROM backup	—	71	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	µs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram48k}$	• 48 KB EEPROM backup	—	1.0	1.5	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr8b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
	16-bit write to FlexRAM execution time:					

Table continues on the next page...

Table 50. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr16b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	
$t_{eewr32b48k}$	• 48 KB EEPROM backup	—	720	2125	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 51. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.1.4 Reliability specifications

Table 52. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2

Table continues on the next page...

Table 52. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree2k}$	• EEPROM backup to FlexRAM ratio = 2,048	20 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

5.4.5.1.1 12-bit ADC operating conditions

Table 53. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	3
V_{REFL}	ADC reference voltage low		– 100	0	100	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance		—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	

Table continues on the next page...

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

NOTE

High drive pin should be used for fast bit rate.

Table 59. LPSPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

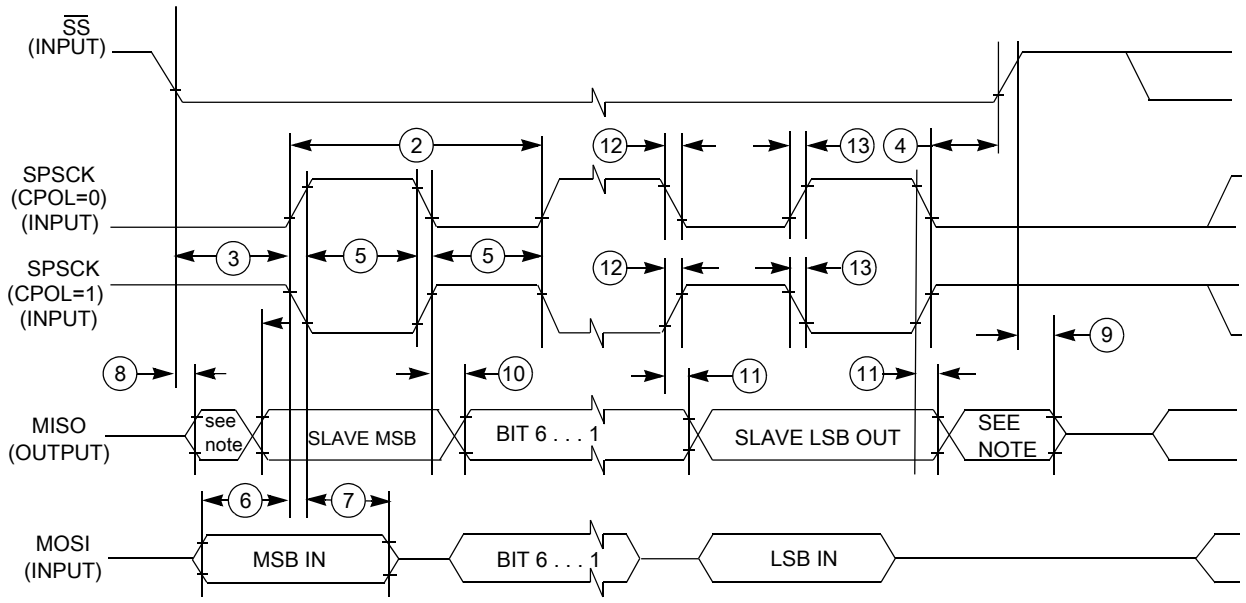

Figure 26. LPSPI slave mode timing (CPHA = 0)

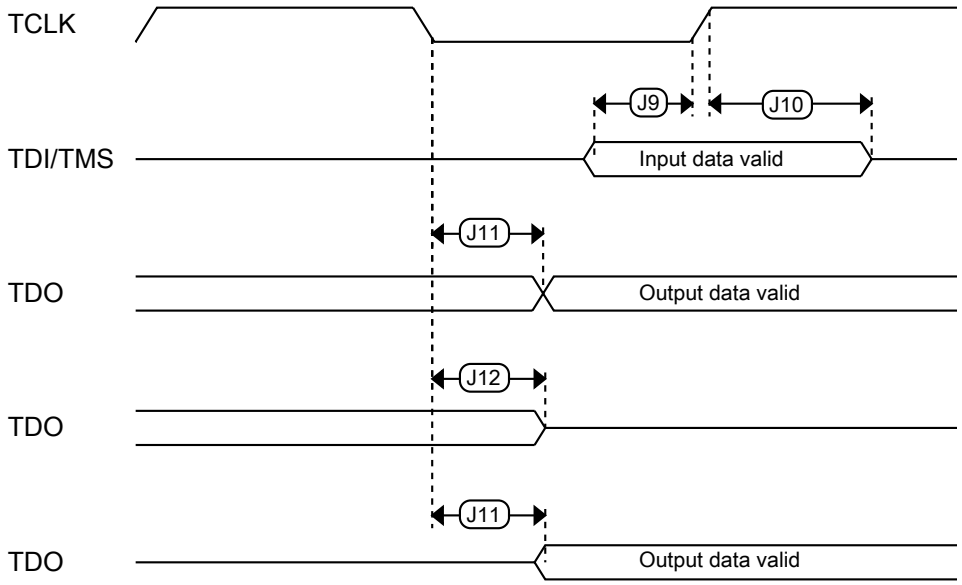

Figure 32. Test Access Port timing

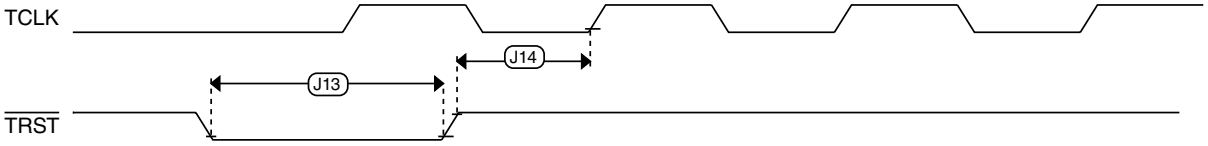

Figure 33. $\overline{\text{TRST}}$ timing

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

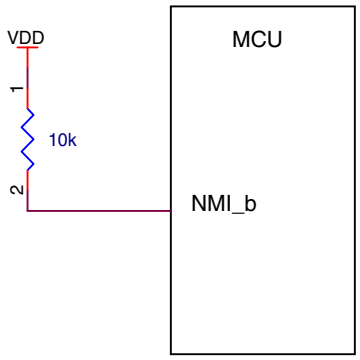

Figure 38. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

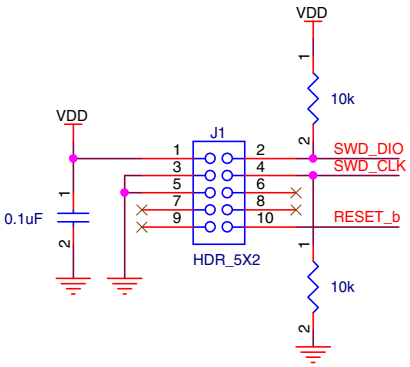

Figure 39. SWD debug interface

- Unused pin

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