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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	63
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3a4ca-au

10.16.1 BFC and BFI

Bit Field Clear and Bit Field Insert.

10.16.1.1 Syntax

```
BFC{cond} Rd, #lsb, #width
BFI{cond} Rd, Rn, #lsb, #width
```

where:

cond — is an optional condition code, see “Conditional execution” on page 91.

Rd — is the destination register.

Rn — is the source register.

lsb — is the position of the least significant bit of the bitfield.

lsb must be in the range 0 to 31.

width — is the width of the bitfield and must be in the range 1 to 32–*lsb*.

10.16.1.2 Operation

BFC clears a bitfield in a register. It clears *width* bits in *Rd*, starting at the low bit position *lsb*. Other bits in *Rd* are unchanged.

BFI copies a bitfield into one register from another register. It replaces *width* bits in *Rd* starting at the low bit position *lsb*, with *width* bits from *Rn* starting at bit[0]. Other bits in *Rd* are unchanged.

10.16.1.3 Restrictions

Do not use SP and do not use PC.

10.16.1.4 Condition flags

These instructions do not affect the flags.

10.16.1.5 Examples

```
BFC   R4, #8, #12       ; Clear bit 8 to bit 19 (12 bits) of R4 to 0
BFI   R9, R2, #8, #12   ; Replace bit 8 to bit 19 (12 bits) of R9 with
                        ; bit 0 to bit 11 from R2
```

10.21.4 Interrupt Control and State Register

The ICSR:

- provides:
  - set-pending and clear-pending bits for the PendSV and SysTick exceptions
- indicates:
  - the exception number of the exception being processed
  - whether there are preempted active exceptions
  - the exception number of the highest priority pending exception
  - whether any interrupts are pending.

See the register summary in Table 10-30 on page 165, and the Type descriptions in Table 10-33 on page 192, for the ICSR attributes. The bit assignments are:

31	30	29	28	27	26	25	24
Reserved	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved

23	22	21	20	19	18	17	16
Reserved for Debug	ISRPENDING	VECTPENDING					

15	14	13	12	11	10	9	8
VECTPENDING				RETTOBASE	Reserved		VECTACTIVE

7	6	5	4	3	2	1	0
VECTACTIVE							

- **PENDSVSET**

RW

PendSV set-pending bit.

Write:

0: no effect

1: changes PendSV exception state to pending.

Read:

0: PendSV exception is not pending

1: PendSV exception is pending.

Writing 1 to this bit is the only way to set the PendSV exception state to pending.

- **PENDSVCLR**

WO

PendSV clear-pending bit.

Write:

0: no effect

1: removes the pending state from the PendSV exception.

11. Debug and Test Features

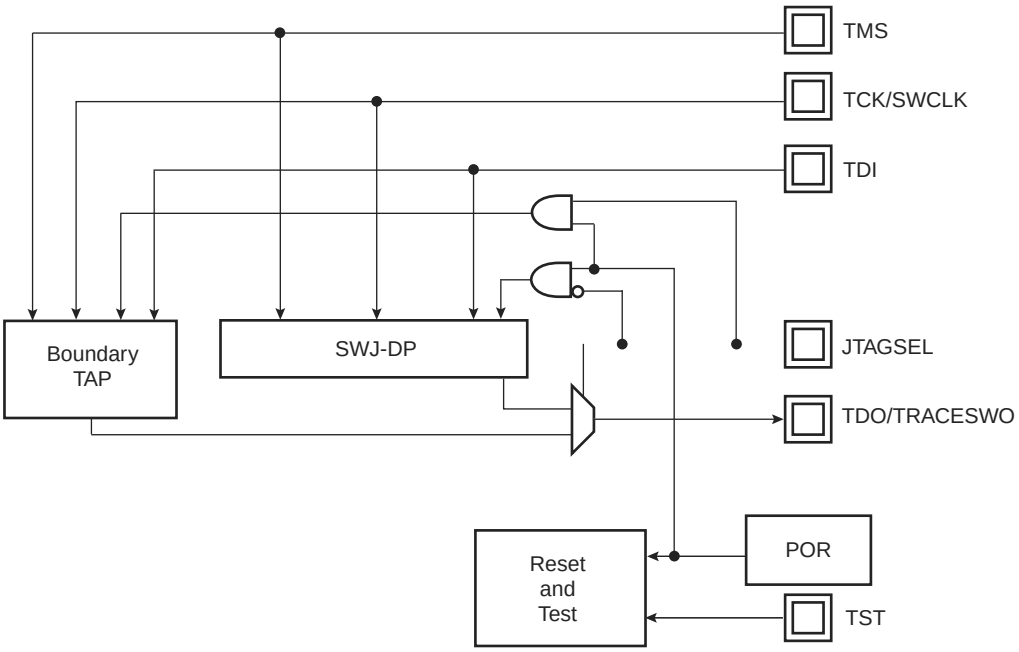
11.1 Description

The SAM3 Series microcontrollers feature a number of complementary debug and test capabilities. The Serial Wire/JTAG Debug Port (SWJ-DP) combining a Serial Wire Debug Port (SW-DP) and JTAG Debug (JTAG-DP) port is used for standard debugging functions, such as downloading code and single-stepping through programs. It also embeds a serial wire trace.

11.2 Embedded Characteristics

- Debug access to all memory and registers in the system, including Cortex-M3 register bank when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- IEEE1149.1 JTAG Boundary-scan on all digital pins

Figure 11-1. Debug and Test Block Diagram



18.5.1 EEFC Flash Mode Register

Name: EEFC_FMR

Address: 0x400E0A00 (0), 0x400E0C00 (1)

Access: Read-write

Offset: 0x00

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	FAM
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	FWS			
7	6	5	4	3	2	1	0
–		–	–	–	–	–	FRDY

- **FRDY: Ready Interrupt Enable**

0: Flash Ready does not generate an interrupt.

1: Flash Ready (to accept a new command) generates an interrupt.

- **FWS: Flash Wait State**

This field defines the number of wait states for read and write operations:

Number of cycles for Read/Write operations = FWS+1

- **FAM: Flash Access Mode**

0: 128-bit access in read Mode only, to enhance access speed.

1: 64-bit access in read Mode only, to enhance power consumption.

No Flash read should be done during change of this register.

25.18.20 SMC Timings Register

Name: SMC_TIMINGSx [x=0..7]

Address: 0x400E007C [0], 0x400E0090 [1], 0x400E00A4 [2], 0x400E00B8 [3], 0x400E00CC [4], 0x400E00E0 [5], 0x400E00F4 [6], 0x400E0108 [7]

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
NFSEL	RBNSEL			TWB			
23	22	21	20	19	18	17	16
–	–	–	–	TRR			
15	14	13	12	11	10	9	8
–	–	–	OCMS	TAR			
7	6	5	4	3	2	1	0
TADL				TCLR			

- **TCLR: CLE to REN Low Delay**

Command Latch Enable falling edge to Read Enable falling edge timing.

Latch Enable Falling to Read Enable Falling = (TCLR[3] * 64) + TCLR[2:0] clock cycles.

- **TADL: ALE to Data Start**

Last address latch cycle to the first rising edge of WEN for data input.

Last address latch to first rising edge of WEN = (TADL[3] * 64) + TADL[2:0] clock cycles.

- **TAR: ALE to REN Low Delay**

Address Latch Enable falling edge to Read Enable falling edge timing.

Address Latch Enable to Read Enable = (TAR[3] * 64) + TAR[2:0] clock cycles.

- **OCMS: Off Chip Memory Scrambling Enable**

When set to one, the memory scrambling is activated.

- **TRR: Ready to REN Low Delay**

Ready/Busy signal to Read Enable falling edge timing.

Read to REN = (TRR[3] * 64) + TRR[2:0] clock cycles.

- **TWB: WEN High to REN to Busy**

Write Enable rising edge to Ready/Busy falling edge timing.

Write Enable to Read/Busy = (TWB[3] * 64) + TWB[2:0] clock cycles.

- **RBNSEL: Ready/Busy Line Selection**

This field indicates the selected Ready/Busy Line from the RBN bundle.

- **CKG: Receive Clock Gating Selection**

Value	Name	Description	RK Pin
0	NONE	None	Input-only
1	CONTINUOUS	Continuous Receive Clock	Output
2	TRANSFER	Receive Clock only during data transfers	Output
3-7		Reserved	

- **START: Receive Start Selection**

Value	Name	Description
0	CONTINUOUS	Continuous, as soon as the receiver is enabled, and immediately after the end of transfer of the previous data.
1	TRANSMIT	Transmit start
2	RF_LOW	Detection of a low level on RF signal
3	RF_HIGH	Detection of a high level on RF signal
4	RF_FALLING	Detection of a falling edge on RF signal
5	RF_RISING	Detection of a rising edge on RF signal
6	RF_LEVEL	Detection of any level change on RF signal
7	RF_EDGE	Detection of any edge on RF signal
8	CMP_0	Compare 0

- **STOP: Receive Stop Selection**

0 = After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.

1 = After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

- **STTDLY: Receive Start Delay**

If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the actual start of reception. When the Receiver is programmed to start synchronously with the Transmitter, the delay is also applied.

Note: It is very important that STTDLY be set carefully. If STTDLY must be set, it should be done in relation to TAG (Receive Sync Data) reception.

- **PERIOD: Receive Period Divider Selection**

This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync Signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each 2 x (PERIOD+1) Receive Clock.

31. Parallel Input/Output Controller (PIO)

31.1 Description

The Parallel Input/Output Controller (PIO) manages up to 32 fully programmable input/output lines. Each I/O line may be dedicated as a general-purpose I/O or be assigned to a function of an embedded peripheral. This assures effective optimization of the pins of a product.

Each I/O line is associated with a bit number in all of the 32-bit registers of the 32-bit wide User Interface.

Each I/O line of the PIO Controller features:

- An input change interrupt enabling level change detection on any I/O line.
- Additional Interrupt modes enabling rising edge, falling edge, low level or high level detection on any I/O line.
- A glitch filter providing rejection of glitches lower than one-half of system clock cycle.
- A debouncing filter providing rejection of unwanted pulses from key or push button operations.
- Multi-drive capability similar to an open drain I/O line.
- Control of the pull-up of the I/O line.
- Input visibility and output control.

The PIO Controller also features a synchronous output providing up to 32 bits of data output in a single write operation.

31.2 Embedded Characteristics

- Up to 4 PIO Controllers, PIOA, PIOB, PIOC, PIOD, PIOE and PIOF controlling a maximum of 103 I/O Lines
- Each PIO Controller controls up to 32 programmable I/O Lines

Table 31-1. PIO Lines per PIO according to Version

Version	100 pin SAM3X/A	144 pin SAM3X	217 pin SAM3X8H[1]
PIOA	30		32
PIOB	32		
PIOC	1	31	
PIOD	-	10	31
PIOE	-	-	32
PIOF	-	-	6
Total	63	103	164

Note: 1.This device is not commercially available. Mounted only on the SAM3X-EK evaluation kit.

- Fully programmable through Set/Clear Registers
- Multiplexing of four peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change, rising edge, falling edge, low level and level interrupt
  - Debouncing and Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull-up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

36.7.10 TC Interrupt Enable Register

Name: TC_IERx [x=0..2]

Address: 0x40080024 (0)[0], 0x40080064 (0)[1], 0x400800A4 (0)[2], 0x40084024 (1)[0], 0x40084064 (1)[1], 0x400840A4 (1)[2], 0x40088024 (2)[0], 0x40088064 (2)[1], 0x400880A4 (2)[2]

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- **COVFS: Counter Overflow**

0: No effect.

1: Enables the Counter Overflow Interrupt.

- **LOVRS: Load Overrun**

0: No effect.

1: Enables the Load Overrun Interrupt.

- **CPAS: RA Compare**

0: No effect.

1: Enables the RA Compare Interrupt.

- **CPBS: RB Compare**

0: No effect.

1: Enables the RB Compare Interrupt.

- **CPCS: RC Compare**

0: No effect.

1: Enables the RC Compare Interrupt.

- **LDRAS: RA Loading**

0: No effect.

1: Enables the RA Load Interrupt.

- **LDRBS: RB Loading**

0: No effect.

1: Enables the RB Load Interrupt.

- **ETRGS: External Trigger**

0: No effect.

1: Enables the External Trigger Interrupt.

36.7.11 TC Interrupt Disable Register

Name: TC_IDRx [x=0..2]

Address: 0x40080028 (0)[0], 0x40080068 (0)[1], 0x400800A8 (0)[2], 0x40084028 (1)[0], 0x40084068 (1)[1], 0x400840A8 (1)[2], 0x40088028 (2)[0], 0x40088068 (2)[1], 0x400880A8 (2)[2]

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS

- **COVFS: Counter Overflow**

0: No effect.

1: Disables the Counter Overflow Interrupt.

- **LOVRS: Load Overrun**

0: No effect.

1: Disables the Load Overrun Interrupt (if TC_CMRx.WAVE = 0).

- **CPAS: RA Compare**

0: No effect.

1: Disables the RA Compare Interrupt (if TC_CMRx.WAVE = 1).

- **CPBS: RB Compare**

0: No effect.

1: Disables the RB Compare Interrupt (if TC_CMRx.WAVE = 1).

- **CPCS: RC Compare**

0: No effect.

1: Disables the RC Compare Interrupt.

- **LDRAS: RA Loading**

0: No effect.

1: Disables the RA Load Interrupt (if TC_CMRx.WAVE = 0).

- **LDRBS: RB Loading**

0: No effect.

1: Disables the RB Load Interrupt (if TC_CMRx.WAVE = 0).

36.7.20 TC Write Protection Mode Register

Name: TC_WPMR

Address: 0x400800E4 (0), 0x400840E4 (1), 0x400880E4 (2)

Access: Read/Write

31	30	29	28	27	26	25	24
WPKEY							

23	22	21	20	19	18	17	16
WPKEY							

15	14	13	12	11	10	9	8
WPKEY							

7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPEN

- **WPEN: Write Protection Enable**

0: Disables the write protection if WPKEY corresponds to 0x54494D (“TIM” in ASCII).

1: Enables the write protection if WPKEY corresponds to 0x54494D (“TIM” in ASCII).

The Timer Counter clock of the first channel must be enabled to access this register.

See Section 36.6.17 ”Register Write Protection”, for a list of registers that can be write-protected and Timer Counter clock conditions.

- **WPKEY: Write Protection Key**

Value	Name	Description
0x54494D	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

37.8.6 READ_SINGLE_BLOCK Operation using DMA Controller

37.8.6.1 Block Length is Multiple of 4

1. Wait until the current command execution has successfully completed.
   a. Check that CMDRDY and NOTBUSY are asserted in HSMCI_SR.
2. Program the block length in the card. This value defines the value *block_length.*
3. Program the block length in the HSMCI configuration register with *block_length* value.
4. Set RDPROOF bit in HSMCI_MR to avoid overflow.
5. Program HSMCI_DMA register with the following fields:
   – ROPT field is set to 0.
   – OFFSET field is set to 0.
   – CHKSIZE is user defined.
   – DMAEN is set to true to enable DMAC hardware handshaking in the HSMCI. This bit was previously set to false.
6. Issue a READ_SINGLE_BLOCK command.
7. Program the DMA controller.
   a. Read the channel Register to choose an available (disabled) channel.
   b. Clear any pending interrupts on the channel from the previous DMA transfer by reading the DMAC_EBCISR register.
   c. Program the channel registers.
   d. The DMAC_SADDRx register for channel x must be set with the starting address of the HSMCI_FIFO address.
   e. The DMAC_DADDRx register for channel x must be word aligned.
   f. Program DMAC_CTRLAx register of channel x with the following field's values:
      –DST_WIDTH is set to WORD.
      –SRC_WIDTH is set to WORD.
      –SCSIZE must be set according to the value of HSMCI_DMA, CHKSIZE field.
      –BTSIZE is programmed with *block_length/4.*
   g. Program DMAC_CTRLBx register for channel x with the following field's values:
      – DST_INCR is set to INCR.
      – SRC_INCR is set to INCR.
      – FC field is programmed with peripheral to memory flow control mode.
      – both DST_DSCR and SRC_DSCR are set to 1 (descriptor fetch is disabled).
      – DIF and SIF are set with their respective layer ID. If SIF is different from DIF, the DMA controller is able to prefetch data and write HSMCI simultaneously.
   h. Program DMAC_CFGx register for channel x with the following field's values:
      –FIFOCFG defines the watermark of the DMA channel FIFO.
      –SRC_H2SEL is set to true to enable hardware handshaking on the destination.
      –SRC_PER is programmed with the hardware handshaking ID of the targeted HSMCI Host Controller.
      –Enable Channel x, writing one to DMAC_CHER[x]. The DMAC is ready and waiting for request.
8. Wait for XFRDONE in HSMCI_SR register.

38.7.22 PWM Output Selection Clear Update Register

Name: PWM_OSCUPD

Address: 0x40094058

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
OSCUPL7	OSCUPDL6	OSCUPL5	OSCUPL4	OSCUPL3	OSCUPL2	OSCUPL1	OSCUPL0

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
OSCUPH7	OSCUPH6	OSCUPH5	OSCUPH4	OSCUPH3	OSCUPH2	OSCUPH1	OSCUPH0

- **OSCUPHx: Output Selection Clear for PWMH output of the channel x**

0 = No effect.

1 = Dead-time generator output DTOHx selected as PWMH output of channel x at the beginning of the next channel x PWM period.

- **OSCUPLx: Output Selection Clear for PWML output of the channel x**

0 = No effect.

1 = Dead-time generator output DTOLx selected as PWML output of channel x at the beginning of the next channel x PWM period.

39. USB On-The-Go Interface (UOTGHS)

39.1 Description

The Universal Serial Bus (USB) MCU device complies with the Universal Serial Bus (USB) 2.0 specification in all speeds.

Each pipe/endpoint can be configured in one of several USB transfer types. It can be associated with one, two or three banks of a DPRAM used to store the current data payload. If two or three banks are used, then one DPRAM bank is read or written by the CPU or the DMA, while the other is read or written by the UOTGHS core. This feature is mandatory for isochronous pipes/endpoints.

Table 39-1 on page 1053 describes the hardware configuration of the USB MCU device.

Table 39-1. Description of USB Pipes/Endpoints

Pipe/Endpoint	Mnemonic	Max. Nb. Banks	DMA	High Band Width	Max. Pipe/ Endpoint Size	Type
0	PEP_0	1	N	N	64	Control
1	PEP_1	3	Y	1	1024	Isochronous/Bulk/Interrupt/Control
2	PEP_2	3	Y	Y	1024	Isochronous/Bulk/Interrupt/Control
3	PEP_3	2	Y	Y	1024	Isochronous/Bulk/Interrupt/Control
4	PEP_4	2	Y	Y	1024	Isochronous/Bulk/Interrupt/Control
5	PEP_5	2	Y	Y	1024	Isochronous/Bulk/Interrupt/Control
6	PEP_6	2	Y	Y	1024	Isochronous/Bulk/Interrupt/Control
7	PEP_7	2	N	Y	1024	Isochronous/Bulk/Interrupt/Control
8	PEP_8	2	_	Y	1024	Isochronous/Bulk/Interrupt/Control
9	PEP_9	2	_	Y	1024	Isochronous/Bulk/Interrupt/Control

Note: Bit fields are presented throughout the document as follows: ‘REGISTER. FIELD’ (e.g. UOTGHS_CTRL.USBE)

39.2 Embedded Characteristics

- Compatible with the USB 2.0 specification
- Supports High (480 Mbps), Full (12 Mbps) and Low (1.5 Mbps) speed communication and On-The-Go
- 10 pipes/endpoints
- 4096 bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 3 memory banks per Pipe/Endpoint (Not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint configuration and management with dedicated DMA channels
- On-Chip UTMI transceiver including Pull-Ups/Pull-downs
- On-Chip OTG pad including VBUS analog comparator

39.6.2.5 Device Global Interrupt Mask Register

Name: UOTGHS_DEVIMR

Address: 0x400AC010

Access: Read-only

31	30	29	28	27	26	25	24
–	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
–	–	PEP_9	PEP_8	PEP_7	PEP_6	PEP_5	PEP_4
15	14	13	12	11	10	9	8
PEP_3	PEP_2	PEP_1	PEP_0	–	–	–	–
7	6	5	4	3	2	1	0
–	UPRSME	EORSME	WAKEUPE	EORSTE	SOFE	MSOFE	SUSPE

- **DMA_x: DMA Channel x Interrupt Mask**

0: The interrupt is disabled.

1: The interrupt is enabled.

This bit is set when DMA_x bit in UOTGHS_DEVIER is written to one.

This bit is cleared when DMA_x bit in UOTGHS_DEVIDR is written to one.

- **PEP_x: Endpoint x Interrupt Mask**

0: The interrupt is disabled.

1: The interrupt is enabled.

This bit is set when PEP_x bit in UOTGHS_DEVIER is written to one.

This bit is cleared when PEP_x bit in UOTGHS_DEVIDR is written to one.

- **UPRSME: Upstream Resume Interrupt Mask**

0: The interrupt is disabled.

1: The interrupt is enabled.

This bit is set when UPRSMES bit in UOTGHS_DEVIER is written to one.

This bit is cleared when UPRSMEC bit in UOTGHS_DEVIDR is written to one.

- **EORSME: End of Resume Interrupt Mask**

0: The interrupt is disabled.

1: The interrupt is enabled.

This bit is set when EORSMES bit in UOTGHS_DEVIER is written to one.

This bit is cleared when EORSMEC bit in UOTGHS_DEVIDR is written to one.

- **WAKEUPE: Wake-Up Interrupt Mask**

0: The interrupt is disabled.

1: The interrupt is enabled.

This bit is set when WAKEUPES bit in UOTGHS_DEVIER is written to one.

This bit is cleared when WAKEUPEC bit in UOTGHS_DEVIDR is written to one.

39.6.3.5 Host Global Interrupt Mask Register

Name: UOTGHS_HSTIMR

Address: 0x400AC410

Access: Read-only

31	30	29	28	27	26	25	24
–	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	PEP_9	PEP_8
15	14	13	12	11	10	9	8
PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
7	6	5	4	3	2	1	0
–	HWUPIE	HSOFIE	RXRSMIE	RSMEDIE	RSTIE	DDISCIE	DCONNIE

- **DMA_x: DMA Channel x Interrupt Enable**

This bit is set when the corresponding bit in UOTGHS_HSTIER is written to one. This will enable the DMA Channel x Interrupt (UOTGHS_HSTISR.DMA_x).

This bit is cleared when the corresponding bit in UOTGHS_HSTIDR is written to one. This will disable the DMA Channel x Interrupt (UOTGHS_HSTISR.DMA_x).

- **PEP_x: Pipe x Interrupt Enable**

This bit is set when the corresponding bit in UOTGHS_HSTIER is written to one. This will enable the Pipe x Interrupt (UOTGHS_HSTISR.PEP_x).

This bit is cleared when the PEP_x bit is written to one. This will disable the Pipe x Interrupt (PEP_x).

- **HWUPIE: Host Wake-Up Interrupt Enable**

This bit is set when UOTGHS_HSTIER.HWUPIES bit is written to one. This will enable the Host Wake-up Interrupt (UOTGHS_HSTISR.HWUPI).

This bit is cleared when UOTGHS_HSTIDR.HWUPIEC bit is written to one. This will disable the Host Wake-up Interrupt (UOTGHS_HSTISR.HWUPI).

- **HSOFIE: Host Start of Frame Interrupt Enable**

This bit is set when UOTGHS_HSTIER.HSOFIES bit is written to one. This will enable the Host Start of Frame interrupt (UOTGHS_HSTISR.HSOFI).

This bit is cleared when UOTGHS_HSTIDR.HSOFIEC bit is written to one. This will disable the Host Start of Frame interrupt (UOTGHS_HSTISR.HSOFI).

- **RXRSMIE: Upstream Resume Received Interrupt Enable**

This bit is set when UOTGHS_HSTIER.RXRSMIES bit is written to one. This will enable the Upstream Resume Received interrupt (UOTGHS_HSTISR.RXRSMI).

This bit is cleared when UOTGHS_HSTIDR.RXRSMIEC bit is written to one. This will disable the Downstream Resume interrupt (UOTGHS_HSTISR.RXRSMI).

- **RSMEDIE: Downstream Resume Sent Interrupt Enable**

This bit is set when UOTGHS_HSTIER.RSMEDIES bit is written to one. This will enable the Downstream Resume interrupt (UOTGHS_HSTISR.RSMEDI).

This bit is cleared when UOTGHS_HSTIDR.RSMEDIEC bit is written to one. This will disable the Downstream Resume interrupt (UOTGHS_HSTISR.RSMEDI).

41.6.26.16 Excessive Length Errors Register

Name: EMAC_ELE

Address: 0x400B0078

Access: Read-write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
EXL							

- **EXL: Excessive Length Errors**

An 8-bit register counting the number of frames received exceeding 1518 bytes (1536 if bit 8 set in network configuration register) in length but do not have either a CRC error, an alignment error nor a receive symbol error.

42.3.4 TRNG Interrupt Mask Register

Name: TRNG_IMR

Address: 0x400BC018

Reset: 0x0000_0000

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DATRDY

- **DATRDY: Data Ready Interrupt Mask**

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Figure 45-3. Zero-Power-on Reset Characteristics

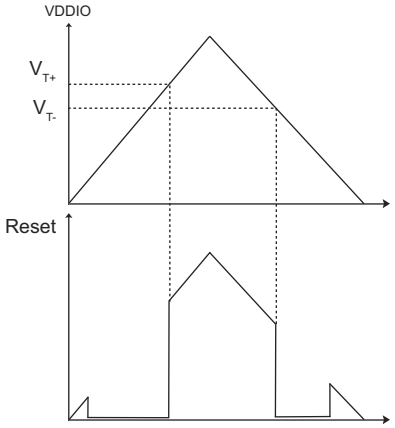


Table 45-8. DC Flash Characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(standby)}$	Standby current	@ 25°C onto VDDCORE = 1.8V	< 1	1.5	µA
		@ 85°C onto VDDCORE = 1.8V	14	40	
		@ 25°C onto VDDCORE = 1.95V	< 1	1.8	
		@ 85°C onto VDDCORE = 1.95V	15	50	
I_{CC}	Active current	128-bit Mode Read Access:			mA
		Maximum Read Frequency onto VDDCORE = 1.8V @ 25 °C	15	20	
		Maximum Read Frequency onto VDDCORE = 1.95V @ 25 °C	20	25	
		64-bit Mode Read Access:			
		Maximum Read Frequency onto VDDCORE = 1.8V @ 25 °C	7.5	10	
		Maximum Read Frequency onto VDDCORE = 1.95V @ 25 °C	10	12.5	
		Write onto VDDCORE = 1.8V @ 25 °C	3.6	4.5	
		Write onto VDDCORE = 1.95V @ 25 °C	5.0	6.0	

45.8 Temperature Sensor

The temperature sensor is connected to channel 15 of the ADC.

The temperature sensor provides an output voltage (V_{O_TS}) that is proportional to absolute temperature (PTAT). V_{O_TS} linearly varies with a temperature slope dV_{O_TS}/dT = 2.65 mV/°C.

V_{O_TS} equals 0.8V at T_A 27°C, with a ±15% accuracy. The V_{O_TS} slope versus temperature dV_{O_TS}/dT = 2.65 mV/°C only shows a ±5% slight variation over process, mismatch and supply voltage.

The user needs to calibrate it (offset calibration) at ambient temperature to eliminate the V_{O_TS} spread at ambient temperature (±15%).

Table 45-39. Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{O_TS}	Output Voltage	T_A = 27° C		0.800		V
$V_{O\_TS(accuracy)}$	Output Voltage Accuracy	T_A = 27° C	-15		+15	%
dV_{O_TS}/dT	Temperature Sensitivity (Slope Voltage vs Temperature)			2.65		mV/°C
	Slope accuracy		-5		+5	%
	Temperature accuracy	After offset calibration Over temperature range -40 to 85 °C	-5		+5	°C
		After offset calibration Over temperature range 0 to 80 °C	-3		+3	°C
t_{START}	Startup Time	After ADC_ACR.TSON =1		20	40	µs
z_o	Output Impedance				30	Ω
$I_{VDDCORE}$	Current Consumption			50	100	µA