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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	63
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam3x4ca-cu

Table 5-1. Low Power Mode Configuration Summary

Mode	VDDBU Region (1)	Regulator	Core Memory Peripherals	Mode Entry	Potential Wake-up Sources	Core at Wake-up	PIO State While in Low Power Mode	PIO State at Wake-up	Consumption(2) (3)	Wake-up Time(4)
Backup Mode	ON	OFF SHDN = 0	OFF (not powered)	WFE + SLEEPDEEP = 1	FWUP pin Pins WKUP0–15 BOD alarm RTC alarm RTT alarm	Reset	Previous state saved	PIOA & PIOB & PIOC & PIOD & PIOE & PIOF Inputs with pull-ups	2.5 µA typ(5)	< 0.5 ms
Wait Mode	ON	ON SHDN = 1	Powered (not clocked)	WFE + SLEEPDEEP = 0 + LPM = 1	Any event from Fast Startup: - through pins WKUP0–15 - RTC alarm - RTT alarm - USB wake-up	Clocked back	Previous state saved	Unchanged	18.4 µA/26.6 µA(6)	< 10 µs
Sleep Mode	ON	ON SHDN = 1	Powered(7) (not clocked)	WFE or WFI + SLEEPDEEP = 0 + LPM = 0	Entry mode = WFI interrupt only Entry mode = WFE Any enabled interrupt and/or any event from Fast Startup: - through pins WKUP0–15 - RTC alarm - RTT alarm - USB wake-up	Clocked back	Previous state saved	Unchanged	(7)	(7)

Notes:
1. SUPC, 32 kHz Oscillator, RTC, RTT, GPBR, POR.
2. The external loads on PIOs are not taken into account in the calculation.
3. BOD current consumption is not included.
4. When considering the wake-up time, the time required to start the PLL is not taken into account. Once started, the device works with the 4/8/12 MHz Fast RC oscillator. The user has to add the PLL startup time if it is needed in the system. The wake-up time is defined as the time taken for wake-up until the first instruction is fetched.
5. Current consumption on VDDBU.
6. 18.4 µA on VDDCORE, 26.6 µA for total current consumption (using internal voltage regulator).
7. Depends on MCK frequency. In this mode, the core is supplied and not clocked but some peripherals can be clocked.

10.20.2 Interrupt Set-enable Registers

The ISER0-ISER1 register enables interrupts, and show which interrupts are enabled. See:

- the register summary in Table 10-27 on page 153 for the register attributes
- Table 10-28 on page 154 for which interrupts are controlled by each register.

The bit assignments are:

31	30	29	28	27	26	25	24
SETENA bits							

23	22	21	20	19	18	17	16
SETENA bits							

15	14	13	12	11	10	9	8
SETENA bits							

7	6	5	4	3	2	1	0
SETENA bits							

- **SETENA**

Interrupt set-enable bits.

Write:

0: no effect

1: enable interrupt.

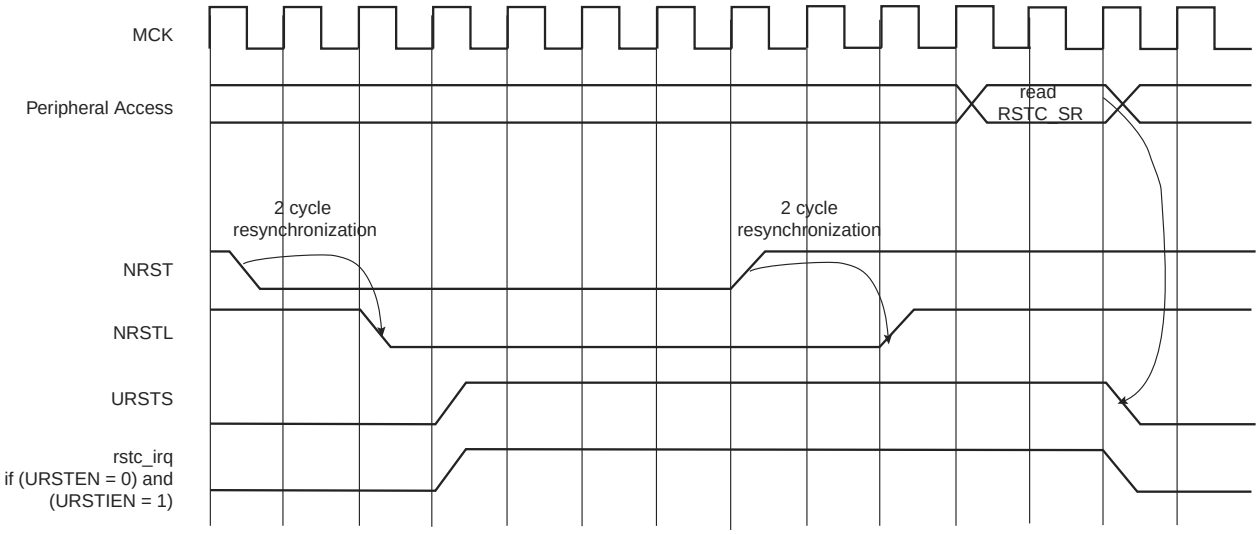
Read:

0: interrupt disabled

1: interrupt enabled.

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority. If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

Figure 12-7. Reset Controller Status and Interrupt



20. SAM3X/A Boot Program

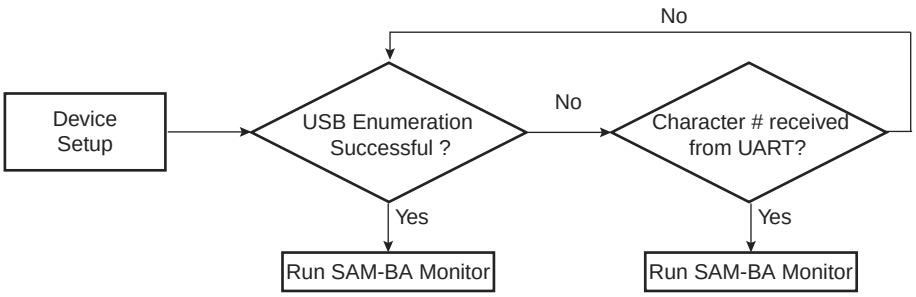
20.1 Description

The SAM-BA Boot Program integrates an array of programs permitting download and/or upload into the different memories of the product.

20.2 Flow Diagram

The Boot Program implements the algorithm illustrated in Figure 20-1.

Figure 20-1. Boot Program Algorithm Flow Diagram



The SAM-BA Boot program seeks to detect a source clock either from the embedded main oscillator with external crystal (main oscillator enabled) or from a 12 MHz signal applied to the XIN pin (Main oscillator in Bypass mode).

If a clock is found from the two possible sources above, the boot program checks to verify that the frequency is 12 MHz (taking into account the frequency range of the 32 kHz RC oscillator). If the frequency is 12 MHz, USB activation is allowed, else (no clock or frequency other than 12 MHz), the internal 12 MHz RC oscillator is used as main clock and USB clock is not allowed due to frequency drift of the 12 MHz RC oscillator.

20.3 Device Initialization

The initialization sequence is the following:

1. Stack setup
2. Set up the Embedded Flash Controller
3. External Clock detection (quartz or external clock on XIN)
4. If quartz or external clock is 12.000 MHz, allow USB activation
5. Else, does not allow USB activation and use internal RC 12 MHz
6. Main oscillator frequency detection if no external clock detected
7. Switch Master Clock on Main Oscillator
8. C variable initialization
9. PLLA setup: PLLA is initialized to generate a 48 MHz clock
10. UPLL setup in case of USB activation allowed
11. Disable of the Watchdog
12. Initialization of the UART (115200 bauds, 8, N, 1)
13. Initialization of the USB Device Port (in case of USB activation allowed)
14. Wait for one of the following events
    a. Check if USB device enumeration has occurred
    b. Check if characters have been received in the UART
15. Jump to SAM-BA Monitor (see Section 20.4 ”SAM-BA Monitor”)

29. Chip Identifier (CHIPID)

29.1 Description

Chip Identifier registers permit recognition of the device and its revision. These registers provide the sizes and types of the on-chip memories, as well as the set of embedded peripherals.

Two chip identifier registers are embedded: CHIPID_CIDR (Chip ID Register) and CHIPID_EXID (Extension ID). Both registers contain a hard-wired value that is read-only. The first register contains the following fields:

- EXT - shows the use of the extension identifier register
- NVPTYP and NVPSIZ - identifies the type of embedded non-volatile memory and its size
- ARCH - identifies the set of embedded peripherals
- SRAMSIZ - indicates the size of the embedded SRAM
- EPROC - indicates the embedded ARM processor
- VERSION - gives the revision of the silicon

The second register is device-dependent and reads 0 if the bit EXT is 0.

29.2 Embedded Characteristics

- Chip ID Registers
  - Identification of the Device Revision, Sizes of the Embedded Memories, Set of Peripherals, Embedded Processor

Table 29-1. ATSAM3A/X Chip IDs Register

Chip Name	CHIPID_CIDR	CHIPID_EXID
ATSAM3X8H(1) (Rev A)	0x286E0A60	0x0
ATSAM3X8E (Rev A)	0x285E0A60	0x0
ATSAM3X4E (Rev A)	0x285B0960	0x0
ATSAM3X8C (Rev A)	0x284E0A60	0x0
ATSAM3X4C (Rev A)	0x284B0960	0x0
ATSAM3A8C (Rev A)	0x283E0A60	0x0
ATSAM3A4C (Rev A)	0x283B0960	0x0

Note: 1. This device is not commercially available. Mounted only on the SAM3X-EK evaluation kit.

31.7.18 PIO Multi-driver Enable Register

Name: PIO_MDER

Address: 0x400E0E50 (PIOA), 0x400E1050 (PIOB), 0x400E1250 (PIOC), 0x400E1450 (PIOD), 0x400E1650 (PIOE), 0x400E1850 (PIOF)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in “PIO Write Protect Mode Register” .

- **P0-P31: Multi Drive Enable.**

0: No effect.

1: Enables Multi Drive on the I/O line.

33.11.4 TWI Internal Address Register

Name: TWI_IADR

Address: 0x4008C00C (0), 0x4009000C (1)

Access: Read-write

Reset: 0x00000000

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
IADR							

15	14	13	12	11	10	9	8
IADR							

7	6	5	4	3	2	1	0
IADR							

- **IADR: Internal Address**

0, 1, 2 or 3 bytes depending on IADRSZ.

37.14.19 HSMCI Write Protect Status Register

Name: HSMCI_WPSR

Address: 0x400000E8

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
WP_VSRC							
15	14	13	12	11	10	9	8
WP_VSRC							
7	6	5	4	3	2	1	0
–	–	–	–	WP_VS			

- **WP_VS: Write Protection Violation Status**

Value	Name	Description
0	NONE	No Write Protection Violation occurred since the last read of this register (WP_SR)
1	WRITE	Write Protection detected unauthorized attempt to write a control register had occurred (since the last read.)
2	RESET	Software reset had been performed while Write Protection was enabled (since the last read).
3	BOTH	Both Write Protection violation and software reset with Write Protection enabled have occurred since the last read.

- **WP_VSRC: Write Protection Violation SouRCe**

When WPVS is active, this field indicates the write-protected register (through address offset or code) in which a write access has been attempted.

38.7.3 PWM Disable Register

Name: PWM_DIS

Address: 0x40094008

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
CHID7	CHID6	CHID5	CHID4	CHID3	CHID2	CHID1	CHID0

This register can only be written if the bits WPSWS1 and WPHWS1 are cleared in “PWM Write Protect Status Register” on page 1039.

- **CHIDx: Channel ID**

0 = No effect.

1 = Disable PWM output for channel x.

- **CES: Counter Event Selection**

The bit CES defines when the channel counter event occurs when the period is center aligned (flag CHIDx in the “PWM Interrupt Status Register 1” on page 1013).

CALG = 0 (Left Alignment):

0/1 = The channel counter event occurs at the end of the PWM period.

CALG = 1 (Center Alignment):

0 = The channel counter event occurs at the end of the PWM period.

1 = The channel counter event occurs at the end of the PWM period and at half the PWM period.

- **DTE: Dead-Time Generator Enable**

0 = The dead-time generator is disabled.

1 = The dead-time generator is enabled.

- **DTHI: Dead-Time PWMHx Output Inverted**

0 = The dead-time PWMHx output is not inverted.

1 = The dead-time PWMHx output is inverted.

- **DTLI: Dead-Time PWMLx Output Inverted**

0 = The dead-time PWMLx output is not inverted.

1 = The dead-time PWMLx output is inverted.

See Section 39.5.1.6 for more details about DPRAM management.

Once the pipe is correctly configured (UOTGHS_HSTPIPISRx.CFGOK is one), only the UOTGHS_HSTPIPCFGx.PTOKEN and UOTGHS_HSTPIPCFGx.INTFRQ fields can be written by software. UOTGHS_HSTPIPCFGx.INTFRQ is meaningless for non-interrupt pipes.

When starting an enumeration, the user gets the device descriptor by sending a GET_DESCRIPTOR USB request. This descriptor contains the maximal packet size of the device default control endpoint (bMaxPacketSize0) and the user re-configures the size of the default control pipe with this size parameter.

39.5.3.7 Address Setup

Once the device has answered the first host requests with default device address 0, the host assigns a new address to the device. The host controller has to send a USB reset to the device and to send a SET_ADDRESS (addr) SETUP request with the new address to be used by the device. Once this SETUP transaction is over, the user writes the new address into the USB Host Address for Pipe x field in the USB Host Device Address register (HSTADDR.HSTADDRPx). All following requests, on all pipes, will be performed using this new address.

When the host controller sends a USB reset, the HSTADDRPx field is reset by hardware and the following host requests will be performed using default device address 0.

39.5.3.8 Remote Wake-up

The controller host mode enters the Suspend state when the UOTGHS_HSTCTRL.SOFE bit is written to zero. No more “Start of Frame” is sent on the USB bus and the USB device enters the Suspend state 3 ms later.

The device awakes the host by sending an Upstream Resume (Remote Wake-Up feature). When the host controller detects a non-idle state on the USB bus, it sets the Host Wake-Up interrupt (UOTGHS_HSTISR.HWUPI) bit. If the non-idle bus state corresponds to an Upstream Resume (K state), the Upstream Resume Received Interrupt (UOTGHS_HSTISR.RXRSMI) bit is set. The user has to generate a Downstream Resume within 1 ms and for at least 20 ms by writing a one to the Send USB Resume (UOTGHS_HSTCTRL.RESUME) bit. It is mandatory to write a one to UOTGHS_HSTCTRL.SOFE before writing a one to UOTGHS_HSTCTRL.RESUME to enter the Ready state, else UOTGHS_HSTCTRL.RESUME will have no effect.

39.5.3.9 Management of Control Pipes

A control transaction is composed of three stages:

- SETUP
- Data (IN or OUT)
- Status (OUT or IN)

The user has to change the pipe token according to each stage.

For the control pipe, and only for it, each token is assigned a specific initial data toggle sequence:

- SETUP: Data0
- IN: Data1
- OUT: Data1

39.5.3.10 Management of IN Pipes

IN packets are sent by the USB device controller upon IN requests from the host. All data which acknowledges or not the bank can be read when it is empty.

The pipe must be configured first.

39.6 USB On-The-Go Interface (UOTGHS) User Interface

Table 39-5. Register Mapping

Offset	Register	Name	Access	Reset
0x0000	Device General Control Register	UOTGHS_DEVCTRL	Read-write	0x00000100
0x0004	Device Global Interrupt Status Register	UOTGHS_DEVISR	Read-only	0x00000000
0x0008	Device Global Interrupt Clear Register	UOTGHS_DEVICR	Write-only	
0x000C	Device Global Interrupt Set Register	UOTGHS_DEVIFR	Write-only	
0x0010	Device Global Interrupt Mask Register	UOTGHS_DEVIMR	Read-only	0x00000000
0x0014	Device Global Interrupt Disable Register	UOTGHS_DEVIDR	Write-only	
0x0018	Device Global Interrupt Enable Register	UOTGHS_DEVIER	Write-only	
0x001C	Device Endpoint Register	UOTGHS_DEVEPT	Read-write	0x00000000
0x0020	Device Frame Number Register	UOTGHS_DEVFNUM	Read-only	0x00000000
0x0100 + (n * 0x04) + 0x00	Device Endpoint Configuration Register	UOTGHS_DEVEPTCFG	Read-write	0x00002000
0x0100 + (n * 0x04) + 0x30	Device Endpoint Status Register	UOTGHS_DEVEPTISR	Read-only	0x00000100
0x0100 + (n * 0x04) + 0x60	Device Endpoint Clear Register	UOTGHS_DEVEPTICR	Write-only	
0x0100 + (n * 0x04) + 0x90	Device Endpoint Set Register	UOTGHS_DEVEPTIFR	Write-only	
0x0100 + (n * 0x04) + 0x0C0	Device Endpoint Mask Register	UOTGHS_DEVEPTIMR	Read-only	0x00000000
0x0100 + (n * 0x04) + 0x0F0	Device Endpoint Enable Register	UOTGHS_DEVEPTIER	Write-only	
0x0100 + (n * 0x04) + 0x0120	Device Endpoint Disable Register	UOTGHS_DEVEPTIDR	Write-only	
0x0300 + (n * 0x10)+0x00	Device DMA Channel Next Descriptor Address Register	UOTGHS_DEVDMANXTDSC	Read-write	0x00000000
0x0300 + (n * 0x10)+0x04	Device DMA Channel Address Register	UOTGHS_DEVDMAADDRESS	Read-write	0x00000000
0x0300 + (n * 0x10)+0x08	Device DMA Channel Control Register	UOTGHS_DEVDMACONTROL	Read-write	0x00000000
0x0300 + (n * 0x10)+0x0C	Device DMA Channel Status Register	UOTGHS_DEVDMASTATUS	Read-write	0x00000000
0x0400	Host General Control Register	UOTGHS_HSTCTRL	Read-write	0x00000000
0x0404	Host Global Interrupt Status Register	UOTGHS_HSTISR	Read-only	0x00000000
0x0408	Host Global Interrupt Clear Register	UOTGHS_HSTICR	Write-only	
0x040C	Host Global Interrupt Set Register	UOTGHS_HSTIFR	Write-only	
0x0410	Host Global Interrupt Mask Register	UOTGHS_HSTIMR	Read-only	0x00000000
0x0414	Host Global Interrupt Disable Register	UOTGHS_HSTIDR	Write-only	
0x0418	Host Global Interrupt Enable Register	UOTGHS_HSTIER	Write-only	
0x0041C	Host Pipe Register	UOTGHS_HSTPIP	Read-write	0x00000000
0x0420	Host Frame Number Register	UOTGHS_HSTFNUM	Read-write	0x00000000
0x0424	Host Address 1 Register	UOTGHS_HSTADDR1	Read-write	0x00000000
0x0428	Host Address 2 Register	UOTGHS_HSTADDR2	Read-write	0x00000000
0x042C	Host Address 3 Register	UOTGHS_HSTADDR3	Read-write	0x00000000
0x0500 + (n * 0x04) + 0x00	Host Pipe Configuration Register	UOTGHS_HSTPIPCFG	Read-write	0x00000000
0x0500 + (n * 0x04) + 0x30	Host Pipe Status Register	UOTGHS_HSTPIPISR	Read-only	0x00000000

39.6.2.2 Device Global Interrupt Status Register

Name: UOTGHS_DEVISR

Address: 0x400AC004

Access: Read-only

31	30	29	28	27	26	25	24
–	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	–
23	22	21	20	19	18	17	16
–	–	PEP_9	PEP_8	PEP_7	PEP_6	PEP_5	PEP_4
15	14	13	12	11	10	9	8
PEP_3	PEP_2	PEP_1	PEP_0	–	–	–	–
7	6	5	4	3	2	1	0
–	UPRSM	EORSM	WAKEUP	EORST	SOF	MSOF	SUSP

- **DMA_x: DMA Channel x Interrupt**

This bit is set when an interrupt is triggered by the DMA channel x. This triggers a USB interrupt if DMA_x is one.

This bit is cleared when the UOTGHS_DEVDMASTATUSx interrupt source is cleared.

- **PEP_x: Endpoint x Interrupt**

This bit is set when an interrupt is triggered by the endpoint x (UOTGHS_DEVEPTISRx, UOTGHS_DEVEPTIMRx). This triggers a USB interrupt if UOTGHS_DEVIMR.PEP_x is one.

This bit is cleared when the interrupt source is serviced.

- **UPRSM: Upstream Resume Interrupt**

This bit is set when the UOTGHS sends a resume signal called “Upstream Resume”. This triggers a USB interrupt if UOTGHS_DEVIMR.UPRSME is one.

This bit is cleared when the UOTGHS_DEVICR.UPRSMC bit is written to one to acknowledge the interrupt (USB clock inputs must be enabled before).

- **EORSM: End of Resume Interrupt**

This bit is set when the UOTGHS detects a valid “End of Resume” signal initiated by the host. This triggers a USB interrupt if UOTGHS_DEVIMR.EORSME is one.

This bit is cleared when the UOTGHS_DEVICR.EORSMC bit is written to one to acknowledge the interrupt.

- **WAKEUP: Wake-Up Interrupt**

This bit is set when the UOTGHS is reactivated by a filtered non-idle signal from the lines (not by an upstream resume). This triggers an interrupt if UOTGHS_DEVIMR.WAKEUPE is one.

This bit is cleared when the UOTGHS_DEVICR.WAKEUPC bit is written to one to acknowledge the interrupt (USB clock inputs must be enabled before).

This bit is cleared when the Suspend (SUSP) interrupt bit is set.

This interrupt is generated even if the clock is frozen by the UOTGHS_CTRL.FRZCLK bit.

- **EORST: End of Reset Interrupt**

This bit is set when a USB “End of Reset” has been detected. This triggers a USB interrupt if UOTGHS_DEVIMR.EORSTE is one.

This bit is cleared when the UOTGHS_DEVICR.EORSTC bit is written to one to acknowledge the interrupt.

- **NAKOUTE: NAKed OUT Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.NAKOUTES bit is written to one. This will enable the NAKed OUT interrupt (UOTGHS_DEVEPTISRx.NAKOUTI).

This bit is cleared when UOTGHS_DEVEPTIDRx.NAKOUTEC bit is written to one. This will disable the NAKed OUT interrupt (UOTGHS_DEVEPTISRx.NAKOUTI).

- **HBISOINERRE: High Bandwidth Isochronous IN Error Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.HBISOINERRES bit is written to one. This will enable the HBISOINERRI interrupt.

This bit is cleared when UOTGHS_DEVEPTIDRx.HBISOINERREC bit disable the HBISOINERRI interrupt.

- **RXSTPE: Received SETUP Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.RXSTPES bit is written to one. This will enable the Received SETUP interrupt (UOTGHS_DEVEPTISRx.RXSTPI).

This bit is cleared when UOTGHS_DEVEPTIERx.RXSTPEC bit is written to one. This will disable the Received SETUP interrupt (UOTGHS_DEVEPTISRx.RXSTPI).

- **UNDERFE: Underflow Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.UNDERFES bit is written to one. This will enable the Underflow interrupt (UOTGHS_DEVEPTISRx.UNDERFI).

This bit is cleared when UOTGHS_DEVEPTIDRx.UNDERFEC bit is written to one. This will disable the Underflow interrupt (UOTGHS_DEVEPTISRx.UNDERFI).

- **RXOUTE: Received OUT Data Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.RXOUTES bit is written to one. This will enable the Received OUT Data interrupt (UOTGHS_DEVEPTISRx.RXOUTI).

This bit is cleared when the UOTGHS_DEVEPTIDRx.RXOUTEC bit is written to one. This will disable the Received OUT Data interrupt (UOTGHS_DEVEPTISRx.RXOUTI).

- **TXINE: Transmitted IN Data Interrupt**

This bit is set when UOTGHS_DEVEPTIERx.TXINES bit is written to one. This will enable the Transmitted IN Data interrupt (UOTGHS_DEVEPTISRx.TXINI).

This bit is cleared when UOTGHS_DEVEPTIDRx.TXINEC bit is written to one. This will disable the Transmitted IN Data interrupt (UOTGHS_DEVEPTISRx.TXINI).

- **NBUSYBKES: Number of Busy Banks Interrupt Enable**

Writing a one to this bit will set NBUSYBKE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **ERRORTRANSES: Transaction Error Interrupt Enable**

Writing a one to this bit will set ERRORTRANSE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **DATAXES: DataX Interrupt Enable**

Writing a one to this bit will set DATAXE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **MDATAES: MData Interrupt Enable**

Writing a one to this bit will set MDATAE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **SHORTPACKETES: Short Packet Interrupt Enable**

Writing a one to this bit will set SHORTPACKETE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **STALLEDES: STALLed Interrupt Enable**

Writing a one to this bit will set STALLEDE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **CRCERRES: CRC Error Interrupt Enable**

Writing a one to this bit will set CRCERRE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **OVERFES: Overflow Interrupt Enable**

Writing a one to this bit will set OVERFE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

- **NAKINES: NAKed IN Interrupt Enable**

Writing a one to this bit will set NAKINE bit in UOTGHS_DEVEPTIMRx.

Writing a zero to this bit has no effect.

This bit always reads as zero.

39.6.3.9 Host Address 1 Register

Name: UOTGHS_HSTADDR1

Address: 0x400AC424

Access: Read-write

31	30	29	28	27	26	25	24
–	HSTADDRP3						
23	22	21	20	19	18	17	16
–	HSTADDRP2						
15	14	13	12	11	10	9	8
–	HSTADDRP1						
7	6	5	4	3	2	1	0
–	HSTADDRP0						

- **HSTADDRP3: USB Host Address**

This field contains the address of the Pipe3 of the USB Device.

This field is cleared when a USB reset is requested.

- **HSTADDRP2: USB Host Address**

This field contains the address of the Pipe2 of the USB Device.

This field is cleared when a USB reset is requested.

- **HSTADDRP1: USB Host Address**

This field contains the address of the Pipe1 of the USB Device.

This field is cleared when a USB reset is requested.

- **HSTADDRP0: USB Host Address**

This field contains the address of the Pipe0 of the USB Device.

This field is cleared when a USB reset is requested.

- **PBK: Pipe Banks**

This field contains the number of banks for the pipe.

Value	Name	Description
0	1_BANK	Single-bank pipe
1	2_BANK	Double-bank pipe
2	3_BANK	Triple-bank pipe
3		Reserved

For control endpoints, a single-bank pipe (0b00) should be selected.

This field is cleared upon sending a USB reset.

- **ALLOC: Pipe Memory Allocate**

Writing a one to this bit will allocate the pipe memory.

Writing a zero to this bit will free the pipe memory.

This bit is cleared when a USB Reset is requested.

Refer to the DPRAM Management chapter for more details.

Figure 45-8. Active Mode Measurement Setup for VDDCORE at 1.8V

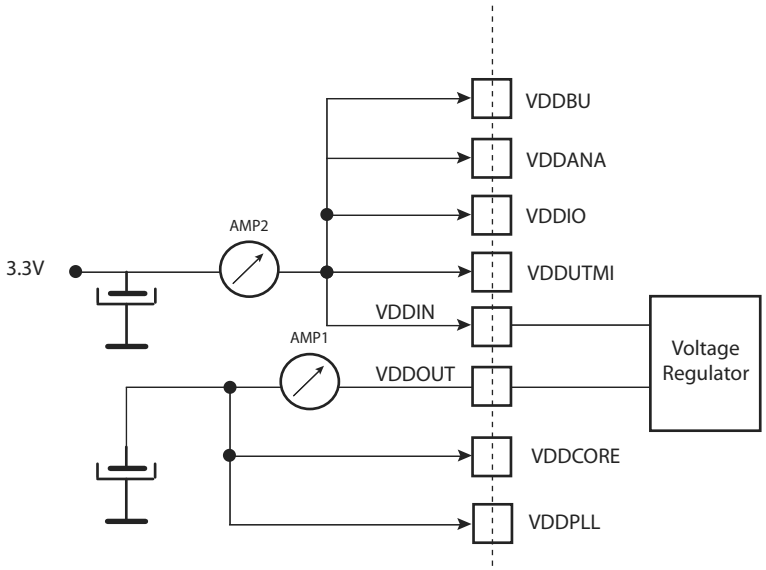
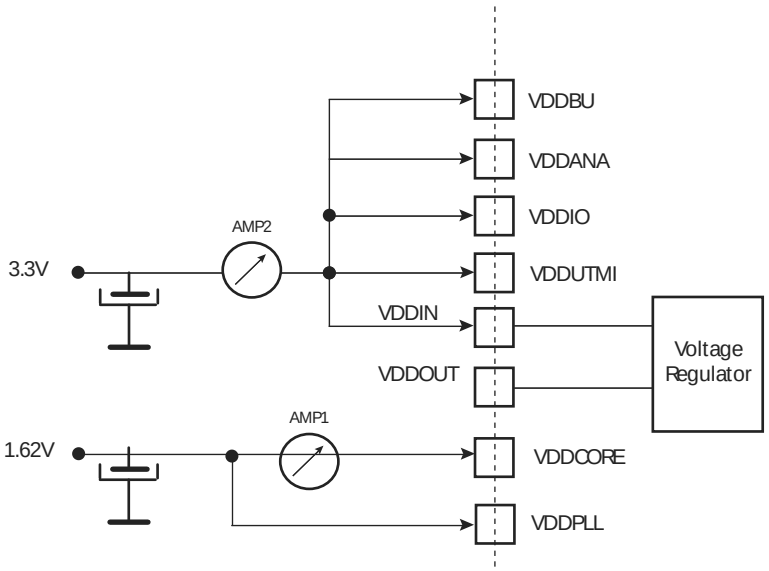


Figure 45-9. Active Mode Measurement Setup for VDDCORE at 1.62V

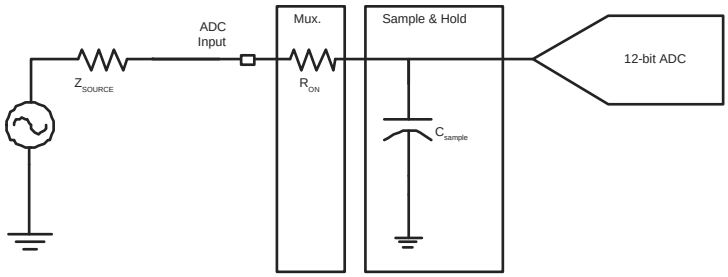


The following tables give Active mode current consumption in typical conditions.

45.7.2.1 Track and Hold Time versus Source Output Impedance

The following figure gives a simplified acquisition path.

Figure 45-18. Simplified Acquisition Path



During the tracking phase the ADC needs to track the input signal during the tracking time shown below:

- 10-bit mode: $t_{TRACK} = 0.042 \times Z_{SOURCE} + 160$
- 12-bit mode: $t_{TRACK} = 0.054 \times Z_{SOURCE} + 205$

With t_{TRACK} expressed in ns and Z_{SOURCE} expressed in ohms.

Two cases must be considered:

1. The calculated tracking time (t_{TRACK}) is lower than 15 t_{CP_ADC}.
   Set TRANSFER = 1 and TRACKTIM = 0 in ADC_MR.
   In this case, the allowed Z_{SOURCE} can be computed versus the ADC frequency with the hypothesis of $t_{TRACK} = 15 \times t_{CP\_ADC}$
   Where $t_{CP\_ADC} = 1/f_{ADC}$. See Table 45-37.
2. The calculated tracking time (t_{TRACK}) is higher than 15 t_{CP_ADC}.
   Set TRANSFER = 1 and TRACKTIM = 0 in ADC_MR.
   In this case, a timer will trigger the ADC in order to set the correct sampling rate according to the Track time.

The maximum possible sampling frequency will be defined by t_{TRACK} in nanoseconds, computed by the previous formula but with minus $15 \times t_{CP\_ADC}$ and plus TRANSFER time.

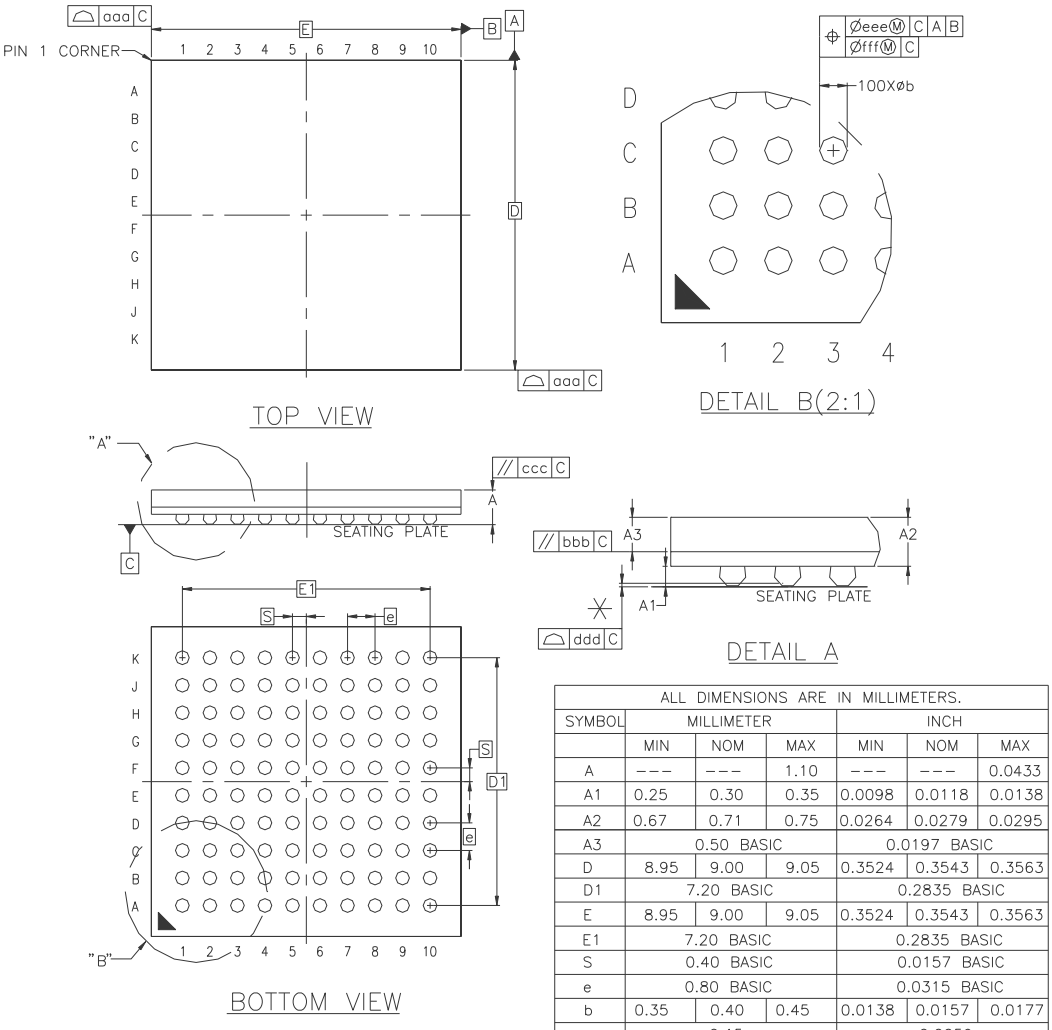
- 10 bit mode: $1/f_S = t_{TRACK} - 15 \times t_{CP\_ADC} + 5\ t_{CP\_ADC}$
- 12 bit mode: $1/f_S = t_{TRACK} - 15 \times t_{CP\_ADC} + 5\ t_{CP\_ADC}$

Note: C_{sample} and R_{ON} are taken into account in the formulas.

Table 45-37. Source Impedance Values

f_{ADC} = ADC clock (MHz)	Z_{SOURCE} (kΩ) for 12 bits	Z_{SOURCE} (kΩ) for 10 bits
20.00	10	14
16.00	14	19
10.67	22	30
8.00	31	41
6.40	40	52
5.33	48	63
4.57	57	74
4.00	66	85

Figure 46-2. 100-ball TFBGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0433
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 46-4. 100-ball TFBGA Package Reference - Soldering Information (Substrate Level)

Ball Land	Diameter 0.45 mm
Soldering Mask Opening	0.35 mm

Table 46-5. 100-ball TFBGA Device and Package Maximum Weight

141	mg

Table 46-6. 100-ball TFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 46-7. 100-ball TFBGA Package Reference

JEDEC Drawing Reference	MO-275-DDAC-1
JESD97 Classification	e8