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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
	2
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l054a24dl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



#### 1. GENERAL DESCRIPTION

The W78L054A is an 8-bit microcontroller which can accommodate a wide supply voltage range with low power consumption. The instruction set for the W78L054A is fully compatible with the standard 8051. The W78L054A contains an 16K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L054A allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

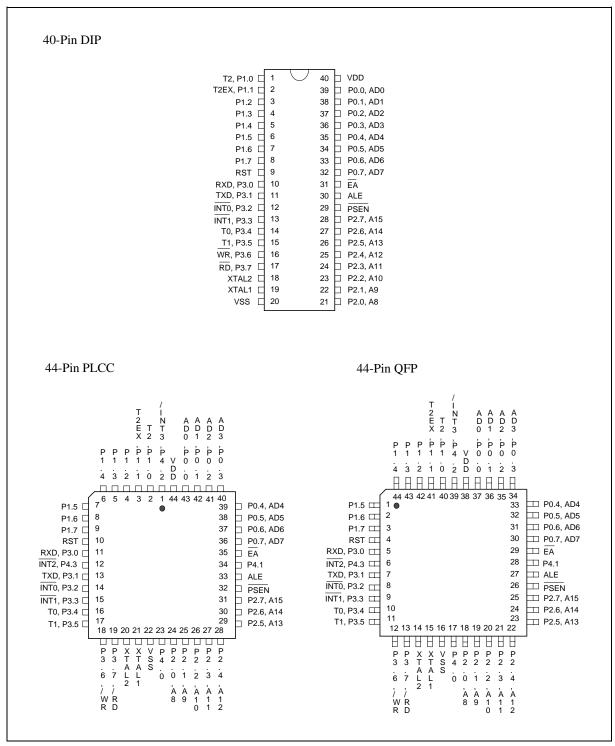
The W78L054A microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

#### 2. FEATURES

- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- · 256 bytes of on-chip scratchpad RAM
- 16 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional INT2 / INT3 (available on 44-pin PLCC/QFP package)
- Three 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Eight sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- · Code protection mechanism
- · Packages:
  - Lead Free (RoHS) DIP 40: W78L054A24DL
  - Lead Free (RoHS) PLCC 44: W78L054A24PL
  - Lead Free (RoHS) PQFP 44: W78L054A24FL



#### 3. PIN CONFIGURATIONS



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## 4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
ĒĀ	<b>EXTERNAL ACCESS ENABLE</b> : This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and
LA	data will not be presented on the bus if EA pin is high and the program counter is within on-chip ROM area.
PSEN	PROGRAM STORE ENABLE: PSEN enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is
	performed, no PSEN strobe signal outputs from this pin.
ALE	ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	<b>RESET</b> : A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
Vss	GROUND: Ground potential
Vdd	POWER SUPPLY: Supply voltage for operation.
P0.0–P0.7	<b>PORT 0</b> : Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The Port 0 is also an open-drain port and external pull-ups need to be connected while in programming.
P1.0–P1.7	<b>PORT 1</b> : Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below:
P1.0-P1.7	T2(P1.0): Timer/Counter 2 external count input
	T2EX(P1.1): Timer/Counter 2 Reload/Capture control
P2.0-P2.7	<b>PORT 2</b> : Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
	<b>PORT 3</b> : Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below:  RXD(P3.0): Serial Port receiver input  TXD(P3.1): Serial Port transmitter output
	INTO (P3.2) : External Interrupt 0
P3.0-P3.7	INT1(P3.3): External Interrupt 1 T0(P3.4): Timer 0 External Input T1(P3.5): Timer 1 External Input
	WR (P3.6) :External Data Memory Write Strobe
	RD (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	<b>PORT 4:</b> Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources (INT2 /INT3).



#### 5. FUNCTIONAL DESCRIPTION

The W78L054A architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

#### Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78L054A: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, autoreload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

#### **New Defined Peripheral**

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt INT2. INT3 has been added to either the PLCC or QFP 44 pin package. And description follows:

#### 1. INT2 / INT3

Two additional external interrupts, INT2 and INT3, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

#### XICON - external interrupt control (C0H)

PX3 EX3 IE3 IT3 PX2 EX2 IE2
-----------------------------

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

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Publication Release Date: December 4, 2006 Revision A6



## 5.1 Eight-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

#### **2. PORT4**

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ( $\overline{\text{INT2}}$ ,  $\overline{\text{INT3}}$ ).

### Example:

P4 REG 0D8H

MOV P4, #0AH ; Output data "A" through P4.0–P4.3. MOV A. P4 : Read P4 status to Accumulator.

ORL P4.#0000001B ANL P4.#1111110B

#### 3. Reduce EMI Emission

Because of on-chip Flash EPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space. The AO bit in the AUXR register, when set, disables the ALE output. In order to reduce EMI emission from oscillation circuitry, W78L054A allows user to diminish the gain of on-chip oscillator amplifiers by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

#### \*\*\*AUXR - Auxiliary register (8EH)

AO: Turn off ALE output.



#### 6. ON-CHIP FLASH EPROM CHARACTERISTICS

The W78L054A has several modes to program the on-chip Flash EPROM. All these operations are configured by the pins RST, ALE,  $\overline{\text{PSEN}}$ , A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3),  $\overline{\text{CE}}$  (P3.6),  $\overline{\text{OE}}$  (P3.7), A0(P1.0) and VPP( $\overline{\text{EA}}$ ). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

### **Read Operation**

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

### **Output Disable Condition**

When the  $\overline{OE}$  is set to high, no data output appears on the D7..D0.

#### **Program Operation**

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the Vpp is reach to Vcp (12.5V) level,  $\overline{CE}$  set to low, and  $\overline{OE}$  set to high.

#### **Program Verify Operation**

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

#### **Erase Operation**

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the Vpp is reach to Vep level,  $\overline{CE}$  set to low, and  $\overline{OE}$  set to high.

## **Erase Verify Operation**

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if Vpp = Vep(14.5V),  $\overline{CE}$  is high and  $\overline{OE}$  is low.

#### **Program/Erase Inhibit Operation**

This operation allows parallel erasing or programming of multiple chips with different data. When  $P3.6(\overline{CE}) = VIH$ ,  $P3.7(\overline{OE}) = VIH$ , erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

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OPERATIONS	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 (CE)	P3.7 (OE)	EA (VPP)	P2, P1 (A15A0)	P0 (D7D0)	NOTE
Read	0	0	0	0	0	0	1	Address	Data Out	
Output Disable	0	0	0	0	0	1	1	Х	Hi-Z	
Program	0	0	0	0	0	1	VCP	Address	Data In	
Program Verify	0	0	0	0	1	0	VCP	Address	Data Out	@3
Erase	1	0	0	0	0	1	VEP	A0:0, others: X	Data In 0FFH	@4
Erase Verify	1	0	0	0	1	0	VEP	Address	Data Out	@5
Program/Erase Inhibit	Х	0	0	0	1	1	VCP/ VEP	Х	Х	

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#### Notes:

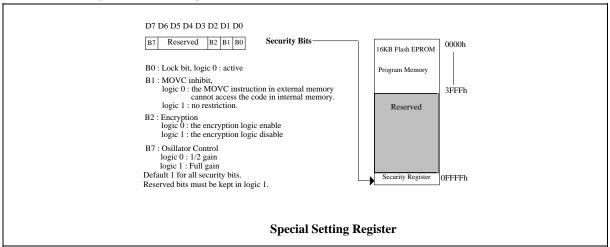
- 1. All these operations happen in RST = VIH, ALE = VIL and  $\overline{\text{PSEN}}$  = VIH.
- 2. VCP = 12.5V, VEP = 14.5V, VIH = VDD, VIL = VSS.
- 3. The program verify operation follows behind the program operation.
- 4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
- 5. The erase verify operation follows behind the erase operation.



#### 7. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78L054A has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The Security register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



#### Lock bit

This bit is used to protect the customer's program code in the W78L054A. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

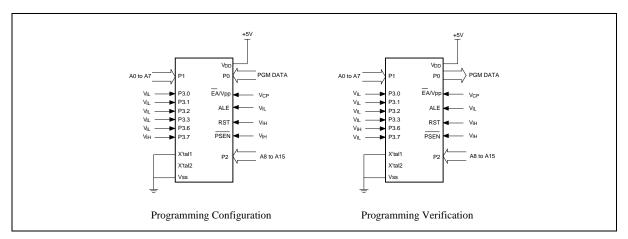
#### **MOVC Inhibit**

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

#### **Encryption**

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.

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## 8. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	VDD-Vss	-0.3	+7.0	٧
Input Voltage	VIN	Vss -0.3	VDD +0.3	V
Operating Temperature	TA	0	70	°C
Storage Temperature	Тѕт	-55	+150	°C

**Note**: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

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## 9. DC CHARACTERISTICS

Vss = 0V,  $TA = 25^{\circ}$  C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
TANAMETER	OTIVI.	MIN.	MAX.	ONT	TEST CONDITIONS
Operating Voltage	VDD	2.4	5.5	V	
Operating Current	IDD	-	20	mA	No load VDD = 5.5V
Operating Current	IDD	-	3	mA	No load VDD = 2.4V
Idle Current	lidle	-	6	mA	VDD = 5.5V, Fosc =20 MHz
idle Current	IIDLE	-	1.5	mA	VDD = 2.4V, Fosc =12 MHz
Power Down Current	IPWDN	-	50	μΑ	VDD = 5.5V, Fosc =20 MHz
Power Down Current	- 20 μA		VDD = 2.4V, Fosc =12 MHz		
Input Current	linia	<b>5</b> 0	.10	^	VDD = 5.5V
P1, P2, P3, P4	lin1	-50	+10	μА	VIN = 0V or VDD
Input Current	lın2	-10	+300		VDD = 5.5V
RST	IIINZ	-10	+300	μΑ	0 < VIN < VDD
Input Leakage Current	luz	40	. 10		VDD = 5.5V
P0, <del>EA</del>	ILK	-10	+10	μΑ	0V < VIN < VDD
Logic 1 to 0 Transition					VDD = 5.5V
Current	ITL [*4]	-500	-	μΑ	VIN = 2.0V
P1, P2, P3, P4					
Input Low Voltage	VIL1	0	0.8	V	VDD = 4.5V
P0, P1, P2, P3, P4, EA	V 1L 1	0	0.5	V	VDD = 2.4V
Input Low Voltage	VIL2	0	0.8	V	VDD = 4.5V
RST[*1]	V ILZ	0	0.3	V	VDD = 2.4V

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#### DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
PARAWETER	STIVI.	MIN.	MAX.	UNIT	TEST CONDITIONS
Input High Voltage	VIH1	2.4	VDD +0.2	V	VDD = 5.5V
P0, P1, P2, P3, P4, <del>EA</del>	VIH1	1.4	VDD +0.2	٧	VDD = 2.4V
Input High Voltage	VIH2	3.5	VDD +0.2	<b>V</b>	VDD = 5.5V
RST[*1]	VIIIZ	1.7	VDD +0.2	>	VDD = 2.4V
Input High Voltage	VIH3	3.5	VDD +0.2	V	VDD = 5.5V
XTAL1 [*3]	VIDS	1.6	VDD +0.2	<b>V</b>	VDD = 2.4V
Output Low Voltage	VOL1	ı	0.45	>	VDD = 4.5V, IOL = +2 mA
P1, P2, P3, P4	VOLI	1	0.25	>	VDD = 2.4V, IOL = +1 mA
Output Low Voltage	\/a. a	1	0.45	>	VDD = 4.5V, IOL = +4 mA
P0, ALE, PSEN [*2]	VOL2	-	0.25	٧	VDD = 2.4V, IOL = +2 mA
Sink Current	Isk1	4	12	mA	VDD = 4.5V, Vin = 0.45V
P1, P2, P3, P4	15K1	1.8	5.4	mA	VDD = 2.4V, Vin = 0.45V
Sink Current	love	8	16	mA	VDD = 4.5V, Vin = 0.45V
P0, ALE, PSEN	ISK2	4.5	9	mA	VDD = 2.4V, Vin = 0.4V
Output High Voltage	Vous	2.4	-	V	$VDD = 4.5V$ , $IOH = -100 \mu A$
P1, P2, P3, P4	VOH1	1.4	-	V	$VDD = 2.4V, IOH = -8 \mu A$
Output High Voltage	1/0110	2.4	-	V	$VDD = 4.5V$ , $IOH = -400 \mu A$
P0, ALE, PSEN [*2]	VOH2	1.4	-	٧	$VDD = 2.4V$ , $IOH = -200 \mu A$
Source Current	lon.	-100	-250	μА	VDD = 4.5V, Vin = 2.4V
P1, P2, P3, P4	ISR1	-20	-50	μΑ	VDD = 2.4V, Vin = 1.4V
Source Current	lone	-8	-14	mA	VDD = 4.5V, Vin = 2.4V
P0, ALE, PSEN	ISR2	-1.9	-3.8	mA	VDD = 2.4V, Vin = 1.4V

#### Notes:

<sup>\*1.</sup> RST pin is a Schmitt trigger input.

<sup>\*2.</sup> P0, ALE and PSEN are tested in the external access mode.

<sup>\*3.</sup> XTAL1 is a CMOS input.

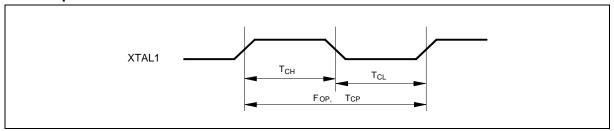
<sup>\*4.</sup> Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.



#### 10. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a  $\pm 20$  nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

#### **Clock Input Waveform**



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	20	MHz	1
Clock Period	Тср	50	-	-	nS	2
Clock High	Тсн	25	-	-	nS	3
Clock Low	TCL	25	-	-	nS	3

#### Notes:

- 1. The clock may be stopped indefinitely in either state.
- 2. The Tcp specification is used as a reference in other specifications.
- 3. There are no duty cycle requirements on the XTAL1 input.

#### **Program Fetch Cycle**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 Tcp -∆	-	-	nS	4
Address Hold from ALE Low	Таан	1 Tcp -∆	-	-	nS	1, 4
ALE Low to PSEN Low	TAPL	1 Tcp -∆	-	-	nS	4
PSEN Low to Data Valid	TPDA	-	-	2 Tcp	nS	2
Data Hold after PSEN High	TPDH	0	-	1 TCP	nS	3
Data Float after PSEN High	TPDZ	0	-	1 Tcp	nS	
ALE Pulse Width	TALW	2 Tcp -∆	2 TCP	-	nS	4
PSEN Pulse Width	TPSW	3 Tcp -Δ	3 Тср	-	nS	4

#### Notes:

- 1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
- 2. Memory access time is 3 Tcp.
- 3. Data have been latched internally prior to PSEN going high.
- 4. " $\Delta$ " (due to buffer driving delay and wire loading) is 20 nS.

## W78LE54/W78L054A

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## **Program Operation**

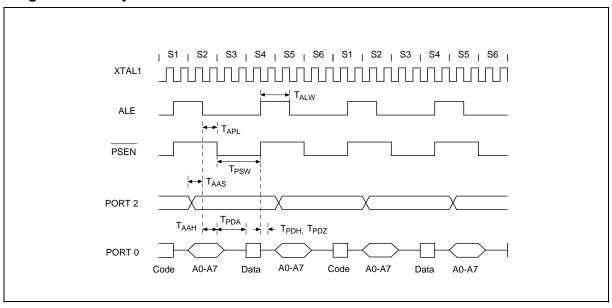
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	TVPS	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	TDH	2.0	-	-	μS
Address Setup Time	Tas	2.0	-	-	μS
Address Hold Time	Тан	0	-	-	μS
CE Program Pulse Width for Program Operation	TPWP	290	300	310	μS
OECTRL Setup Time	Tocs	2.0	-	-	μS
OECTRL Hold Time	Тосн	2.0	-	-	μS
OE Setup Time	Toes	2.0	-	-	μS
OE High to Output Float	TDFP	0	-	130	nS
Data Valid from OE	TOEV	-	-	150	nS

Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the PSEN pin must pull in VIH status.

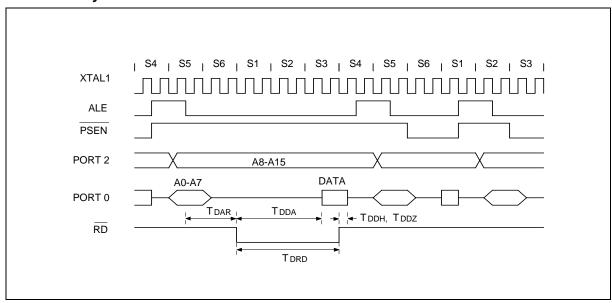


### 11. TIMING WAVEFORMS

### **Program Fetch Cycle**



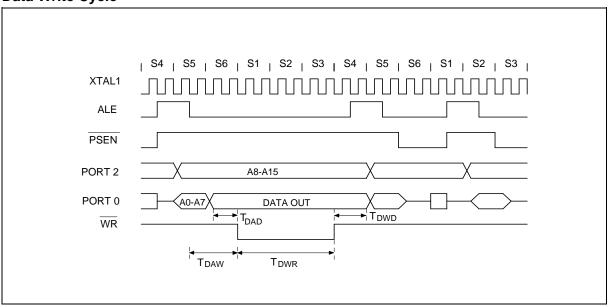
## **Data Read Cycle**



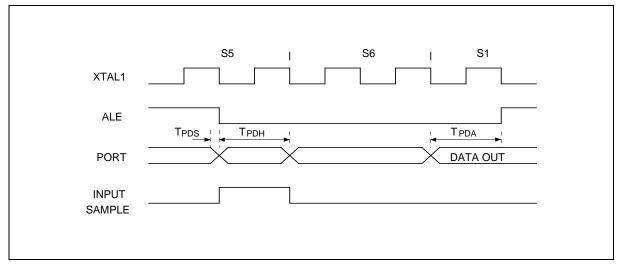


Timing Waveforms, continued

### **Data Write Cycle**



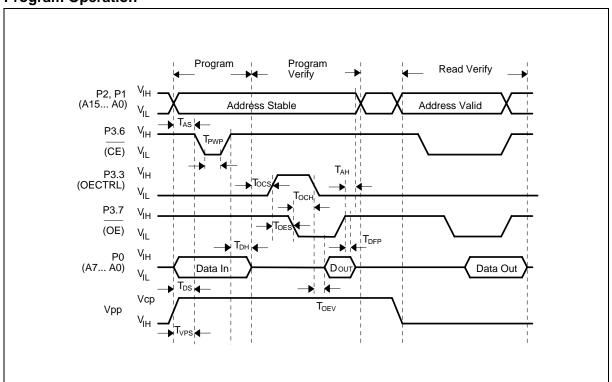
## **Port Access Cycle**





Timing Waveforms, continued

### **Program Operation**



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## 12. TYPICAL APPLICATION CIRCUITS

## **Expanded External Program Memory and Crystal**

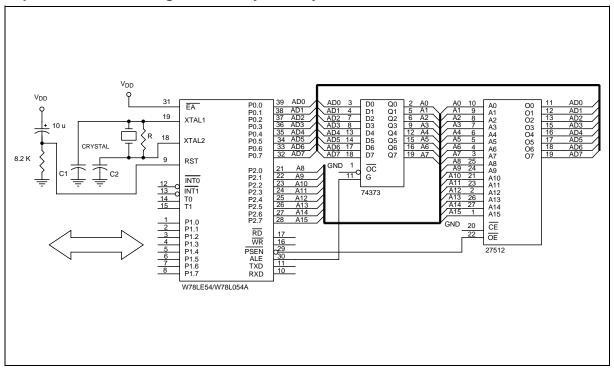


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
20 MHz	15P	15P	-

Above table shows the reference values for crystal applications (full gain).

Note: C1, C2, R components refer to Figure A.



Typical Application Circuits, continued

## **Expanded External Data Memory and Oscillator**

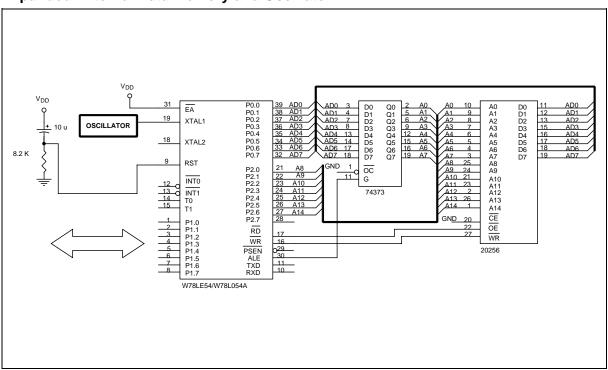
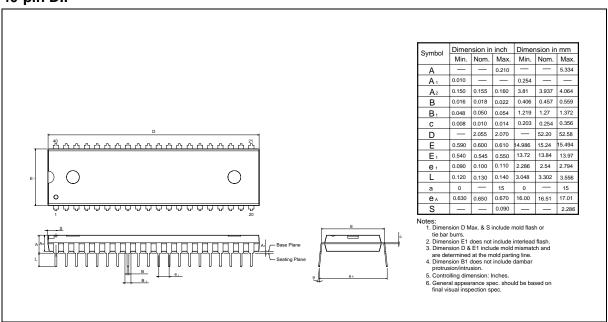


Figure B

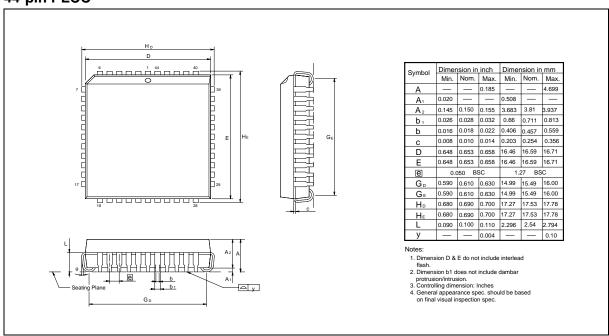


#### 13. PACKAGE DIMENSIONS

## 40-pin DIP



## 44-pin PLCC



## W78LE54/W78L054A



### **REVISION HISTORY**

VERSION	DATE	PAGE	REASONS FOR CHANGE
А3	December 2000		-
A4	April 19, 2005	23	Add Important Notice
A5	October 2, 2006		Remove block diagram
A6	December 4, 2006	2	Remove all Leaded package parts

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