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Details	
Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
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Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 33x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk60dx256zvll10

Chapter 34
Analog-to-Digital Converter (ADC)

Table 4-3. Peripheral bridge 1 slot assignments (continued)

System 32-bit base address	Slot number	Module
0x400E_7000	103	—
0x400E_8000	104	—
0x400E_9000	105	—
0x400E_A000	106	UART 4
0x400E_B000	107	—
0x400E_C000	108	—
0x400E_D000	109	—
0x400E_E000	110	—
0x400E_F000	111	—
0x400F_0000	112	—
0x400F_1000	113	—
0x400F_2000	114	—
0x400F_3000	115	—
0x400F_4000	116	—
0x400F_5000	117	—
0x400F_6000	118	—
0x400F_7000	119	—
0x400F_8000	120	—
0x400F_9000	121	—
0x400F_A000	122	—
0x400F_B000	123	—
0x400F_C000	124	—
0x400F_D000	125	—
0x400F_E000	126	—
0x400F_F000	Not an AIPS-Lite slot. The 32-bit general purpose input/output module that shares the crossbar switch slave port with the AIPS-Lite is accessed at this address.	

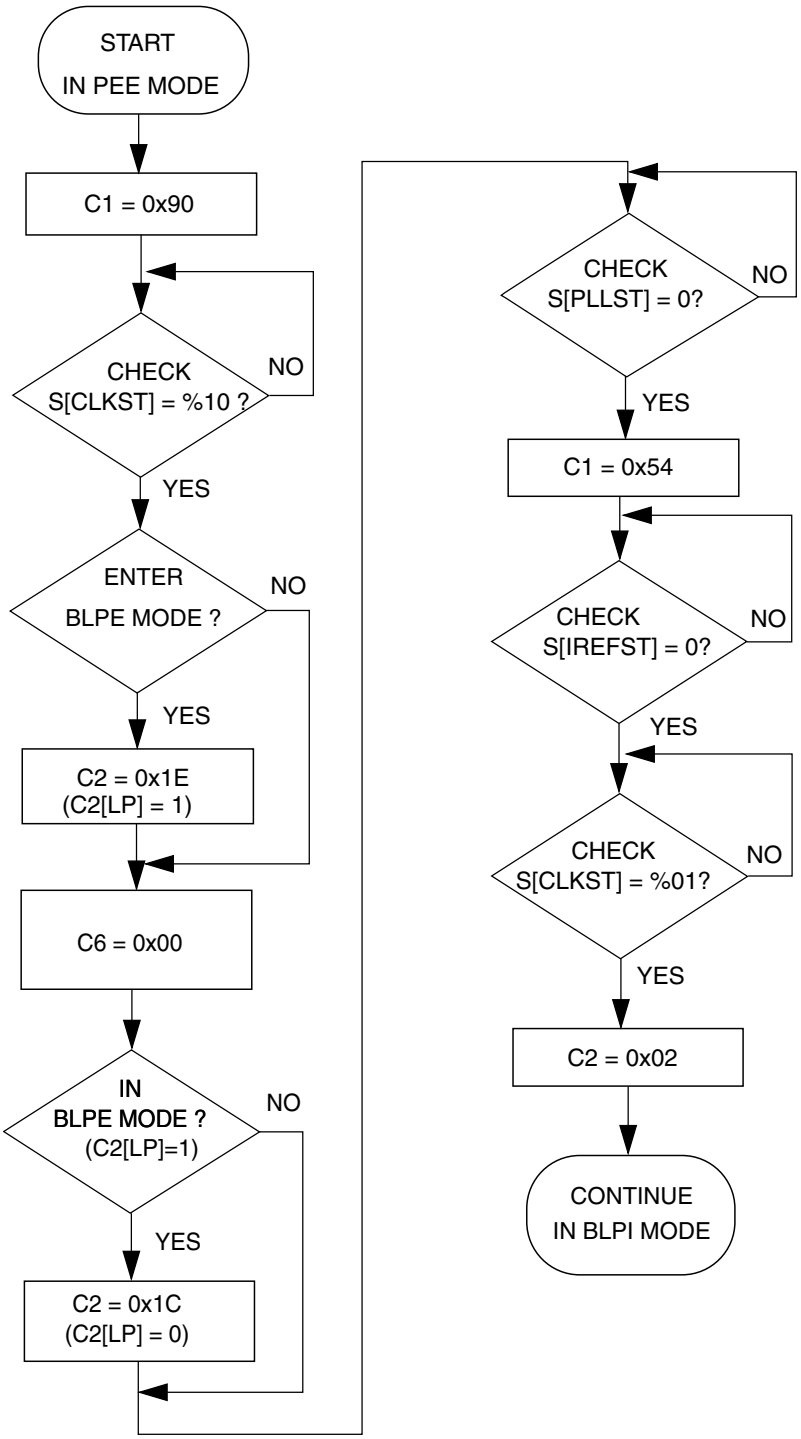


Figure 24-14. Flowchart of PEE to BLPI Mode Transition using an 4 MHz crystal

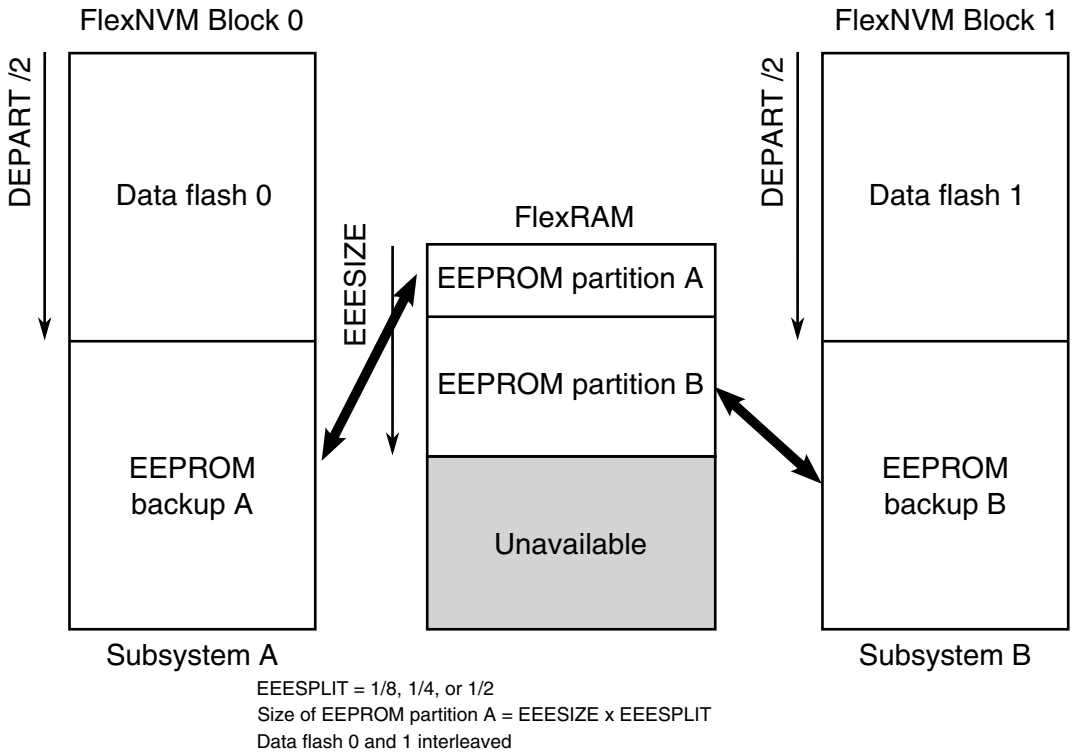


Figure 28-32. FlexRAM to FlexNVM Memory Mapping with 2 Sub-systems

28.4.3.3 EEPROM Implementation Overview

Out of reset with the FSTAT[CCIF] bit clear, the partition settings (EEESIZE, DEPART, EEESPLIT) are read from the data flash IFR and the EEPROM file system is initialized accordingly. The EEPROM file system locates all valid EEPROM data records in EEPROM backup and copies the newest data to FlexRAM. The FSTAT[CCIF] and FCNFG[EEERDY] bits are set after data from all valid EEPROM data records is copied to the FlexRAM. After the CCIF bit is set, the FlexRAM is available for read or write access.

When configured for EEPROM use, writes to an unprotected location in FlexRAM invokes the EEPROM file system to program a new EEPROM data record in the EEPROM backup memory in a round-robin fashion. As needed, the EEPROM file system identifies the EEPROM backup sector that is being erased for future use and partially erases that EEPROM backup sector. After a write to the FlexRAM, the FlexRAM is not accessible until the FSTAT[CCIF] bit is set. The FCNFG[EEERDY] bit will also be set. If enabled, the interrupt associated with the FSTAT[CCIF] bit can be used to determine when the FlexRAM is available for read or write access.

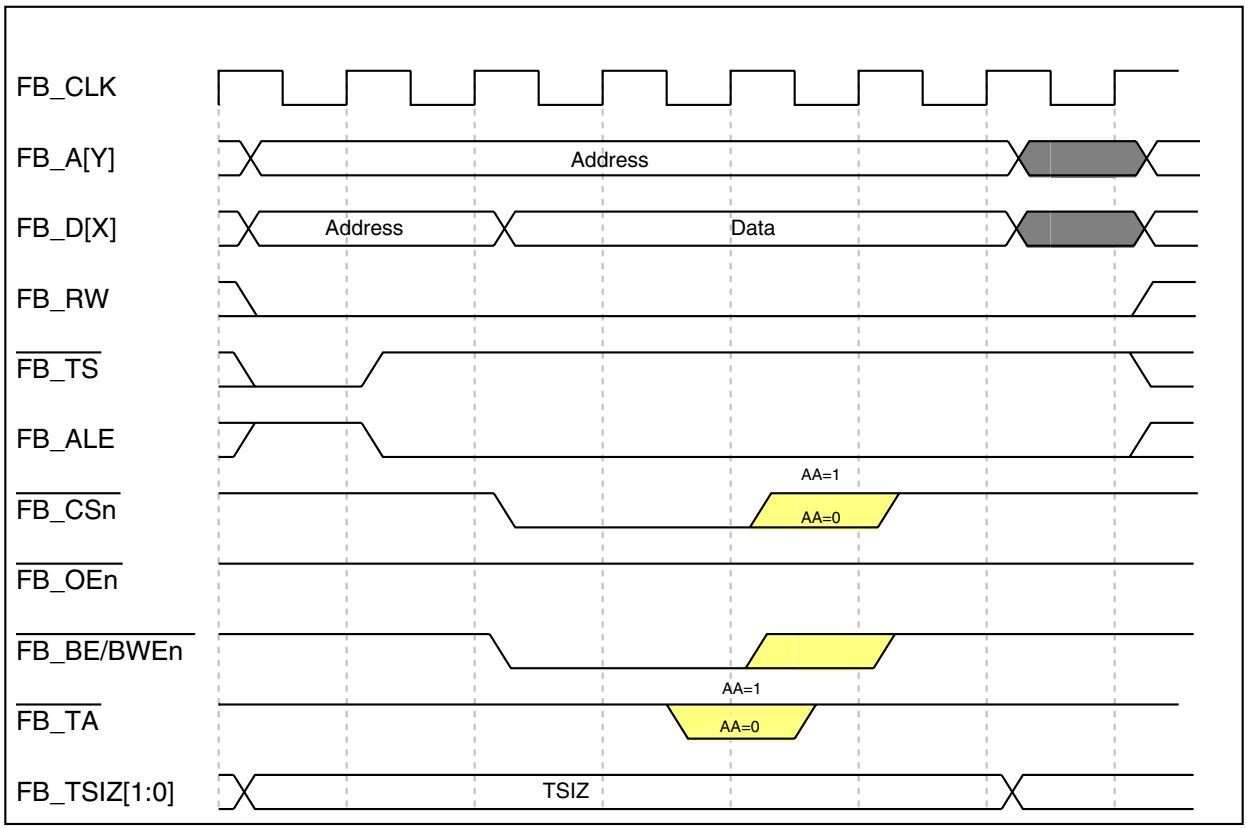


Figure 29-44. Write Cycle with Two-Clock Address Setup and Two-Clock Hold (One Wait State)

29.4.7 Burst Cycles

The device can be programmed to initiate burst cycles if its transfer size exceeds the port size of the selected destination. The initiation of a burst cycle is encoded on the size pins. For burst transfers to smaller port sizes, FB_TSIZ[1:0] indicates the size of the entire transfer. For example, with bursting enabled, a 16-bit transfer to an 8-bit port takes two beats (two byte-sized transfers), for which FB_TSIZ[1:0] equals 10b throughout. A 32-bit transfer to an 8-bit port would take a 4-byte burst cycle, for which FB_TSIZ[1:0] equals 00b throughout.

With bursting disabled, any transfer larger than the port size breaks into multiple individual transfers. With bursting enabled, an access larger than port size results in a burst cycle of multiple beats. The following table shows the result of such transfer translations.

- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable voltage reference: external or alternate
- Self-calibration mode
- Programmable Gain Amplifier (PGA) with up to x64 gain

34.1.2 Block diagram

The following figure is the ADC module block diagram.

DACx_C1 field descriptions (continued)

Field	Description
	01 2 words 10 3 words 11 4 words
2–1 DACBFMD	DAC buffer work mode select 00 Normal Mode 01 Swing Mode 10 One-Time Scan Mode 11 Reserved
0 DACBFEN	DAC buffer enable 0 Buffer read pointer disabled. The converted data is always the first word of the buffer. 1 Buffer read pointer enabled. The converted data is the word that the read pointer points to. It means converted data can be from any word of the buffer.

36.4.6 DAC Control Register 2 (DACx_C2)

Addresses: DAC0_C2 is 400C_C000h base + 23h offset = 400C_C023h

Bit	7	6	5	4	3	2	1	0
Read Write	DACBFRP				DACBFUP			
Reset	0	0	0	0	1	1	1	1

DACx_C2 field descriptions

Field	Description
7–4 DACBFRP	DAC buffer read pointer These 4 bits keep the current value of the buffer read pointer.
3–0 DACBFUP	DAC buffer upper limit These 4 bits select the buffer's upper limit. The buffer read pointer cannot exceed it.

36.5 Functional Description

The 12-bit DAC module can select one of the two reference inputs — DACREF_1 and DACREF_2 as the DAC reference voltage (V_{in}) by DACRFS bit of C0 register. Refer to the module introduction for information on the source for DACREF_1 and DACREF_2. When the DAC is enabled, it converts the data in DACDAT0[11:0] or the data from the DAC data buffer to a stepped analog output voltage. The output voltage range is from $V_{in}/4096$ to V_{in}, and the step is $V_{in}/4096$.

  - Bandgap enabled/standby (output buffer disabled)
  - Tight-regulation buffer mode (output buffer enabled)
- 1.2 V output at room temperature
- Dedicated output pin, VREF_OUT
- Load regulation in tight-regulation mode

37.1.3 Modes of Operation

The Voltage Reference continues normal operation in Run, Wait, and Stop modes. The Voltage Reference can also run in Very Low Power Run (VLPR), Very Low Power Wait (VLPW) and Very Low Power Stop (VLPS). The VREF regulator is not available in any Very Low Power modes and must be disabled (SC[REGEN]=0) before entering these modes. Note however that the accuracy of the output voltage will be reduced (by as much as several mVs) when the VREF regulator is not used.

NOTE

The assignment of module modes to core modes is chip-specific. For module-to-core mode assignments, see the chapter that describes how modules are configured.

37.1.4 VREF Signal Descriptions

The following table shows the Voltage Reference signals properties.

Table 37-1. VREF Signal Descriptions

Signal	Description	I/O
VREF_OUT	Internally-generated Voltage Reference output	O

NOTE

- In Disable mode, the status of the VREF_OUT signal is high-impedence.

37.2 Memory Map and Register Definition

FTMx_C*n*SC field descriptions (continued)

Field	Description
	This field is write protected. It can be written only when MODE[WPDIS] = 1.
4 MSA	Channel Mode Select Used for further selections in the channel logic. Its functionality is dependent on the channel mode. See Table 39-7. This field is write protected. It can be written only when MODE[WPDIS] = 1.
3 ELSB	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See Table 39-7. This field is write protected. It can be written only when MODE[WPDIS] = 1.
2 ELSA	Edge or Level Select The functionality of ELSB and ELSA depends on the channel mode. See Table 39-7. This field is write protected. It can be written only when MODE[WPDIS] = 1.
1 Reserved	This read-only field is reserved and always has the value zero.
0 DMA	DMA Enable Enables DMA transfers for the channel. 0 Disable DMA transfers. 1 Enable DMA transfers.

39.3.7 Channel (n) Value (FTMx_CV)

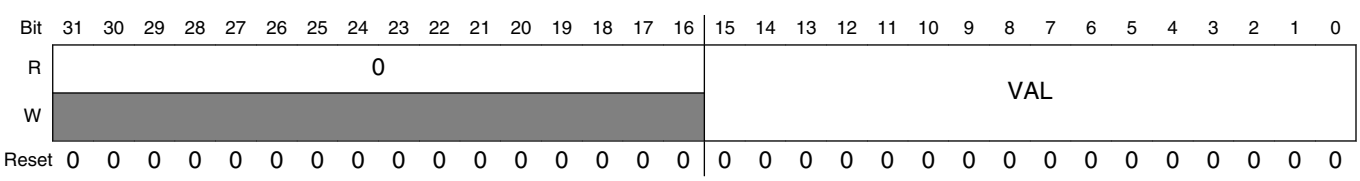
These registers contain the captured FTM counter value for the input modes or the match value for the output modes.

In input capture, capture test, and dual edge capture modes, any write to a CnV register is ignored.

In output modes, writing to a CnV register latches the value into a buffer. A CnV register is updated with the value of its write buffer according to Registers Updated from Write Buffers.

If FTMEN = 0, this write coherency mechanism may be manually reset by writing to the CnSC register (whether BDM mode is active or not).

Addresses: FTM0_C0V is 4003_8000h base + 10h offset = 4003_8010h



If (CLKS[1:0] ≠ 0:0 and FTMEN = 0), then MOD register is updated according to the CPWMS bit, that is:

- If the selected mode is not CPWM then MOD register is updated after MOD register was written and the FTM counter changes from MOD to CNTIN. If the FTM counter is at free-running counter mode then this update occurs when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM then MOD register is updated after MOD register was written and the FTM counter changes from MOD to (MOD – 0x0001).

If (CLKS[1:0] ≠ 0:0 and FTMEN = 1) then MOD register is updated by the MOD register synchronization (MOD Register Synchronization).

39.4.10.3 CnV Register Update

If (CLKS[1:0] = 0:0) then CnV register is updated when CnV register is written (independent of FTMEN bit).

If (CLKS[1:0] ≠ 0:0 and FTMEN = 0), then CnV register is updated according to the selected mode, that is:

- If the selected mode is output compare then CnV register is updated on the next FTM counter change (end of the prescaler counting) after CnV register was written.
- If the selected mode is EPWM then CnV register is updated after CnV register was written and the FTM counter changes from MOD to CNTIN. If the FTM counter is at free-running counter mode then this update occurs when the FTM counter changes from 0xFFFF to 0x0000.
- If the selected mode is CPWM then CnV register is updated after CnV register was written and the FTM counter changes from MOD to (MOD – 0x0001).

If (CLKS[1:0] ≠ 0:0 and FTMEN = 1) then CnV register is updated according to the selected mode, that is:.

41.4.3.4 Glitch filter bypassed

In pulse counter mode when the glitch filter is bypassed, the selected input source increments the LPTMR counter register every time it asserts. Before the LPTMR is first enabled, the selected input source is forced to asserted. This is to prevent the LPTMR counter register from incrementing if the selected input source is already asserted when the LPTMR is first enabled.

41.4.4 LPTMR compare

When the LPTMR counter register equals the value of the LPTMR compare register and increments, the following events occur:

- Timer compare flag is set
- LPTMR interrupt is generated if Timer Interrupt Enable is also set
- LPTMR hardware trigger is generated
- LPTMR counter register is reset if the free running counter bit is clear

When the LPTMR is enabled, the LPTMR compare register can only be altered when the timer compare flag is set. When updating the LPTMR compare register, the LPTMR compare register must be written and the timer compare flag must be cleared before the LPTMR counter has incremented past the new LPTMR compare value.

41.4.5 LPTMR counter

The LPTMR counter register increments by one on every:

- prescaler clock (time counter mode with prescaler bypassed)
- prescaler output (time counter mode with prescaler enabled)
- input source assertion (pulse counter mode with glitch filter bypassed)
- glitch filter output (pulse counter mode with glitch filter enabled).

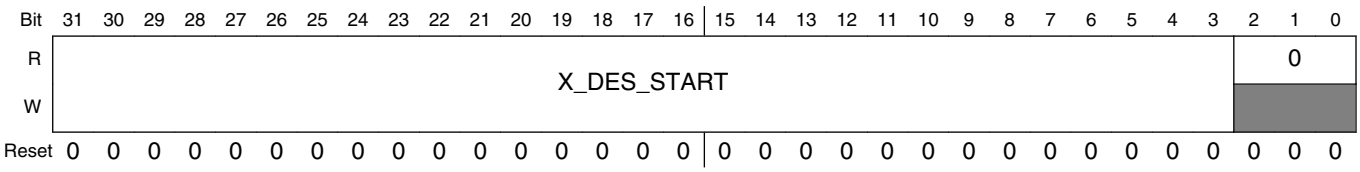
The LPTMR counter register is reset when the LPTMR is disabled or if the counter register overflows. If the CSR[TFC] control bit is set then the LPTMR counter register is also reset whenever the CSR[TCF] status flag is set.

The LPTMR counter register continues incrementing when the core is halted in debug mode.

44.3.20 Transmit Buffer Descriptor Ring Start Register (ENET_TDSR)

TDSR provides a pointer to the start of the circular transmit buffer descriptor queue in external memory. This pointer must be 64-bit aligned (bits 2–0 must be zero); however, it is recommended to be 128-bit aligned (evenly divisible by 16). This register is undefined at reset and must be initialized prior to operation.

Address: ENET_TDSR is 400C_0000h base + 184h offset = 400C_0184h



ENET_TDSR field descriptions

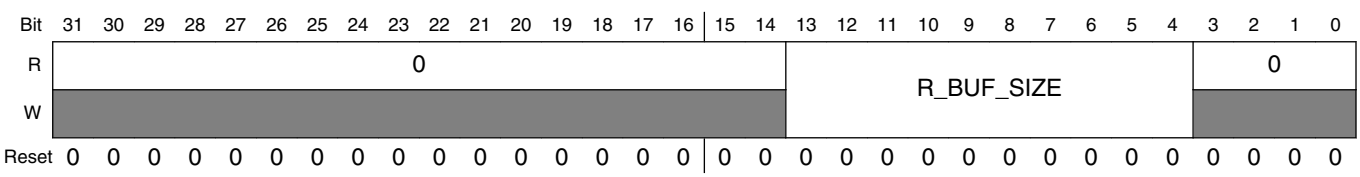
Field	Description
31–3 X_DES_START	Pointer to the start of the transmit buffer descriptor queue.
2–0 Reserved	This read-only field is reserved and always has the value zero.

44.3.21 Maximum Receive Buffer Size Register (ENET_MRBR)

The MRBR is a user-programmable register that dictates the maximum size of all receive buffers. This value should take into consideration that the receive CRC is always written into the last receive buffer. To allow one maximum size frame per buffer, MRBR must be set to RCR[MAX_FL] or larger. To properly align the buffer, MRBR must be evenly divisible by 16. To ensure this, bits 3–0 are forced low.

To minimize bus utilization (descriptor fetches), set MRBR greater than or equal to 256 bytes. The MRBR register is undefined at reset and must be initialized by the user.

Address: ENET_MRBR is 400C_0000h base + 188h offset = 400C_0188h



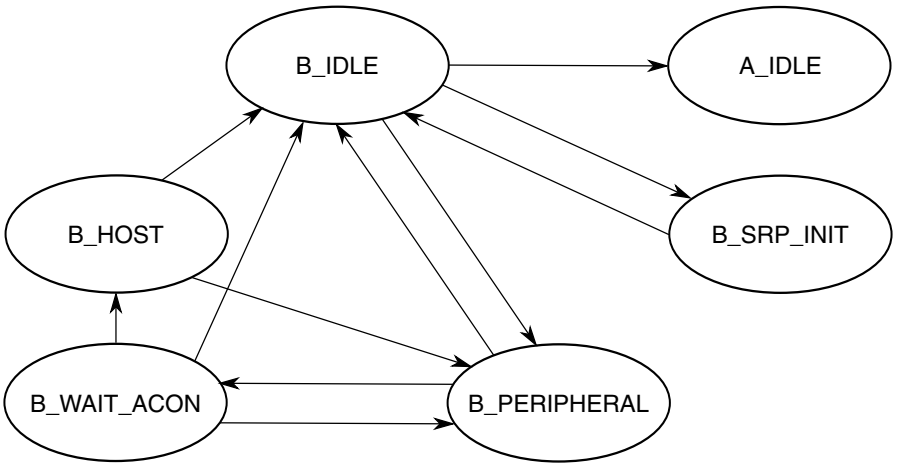


Figure 45-92. Dual Role B Device Flow Diagram

Table 45-95. State Descriptions for the Dual Role B Device Flow

State	Action	Response
B_IDLE	If ID\ Interrupt. A Type A cable has been plugged in and the device should now respond as a Type A device.	Go to A_IDLE
	If B_SESS_VLD Interrupt. The A device has turned on VBUS and begins a session.	Go to B_PERIPHERAL Turn on DP_HIGH
	If B application wants the bus and Bus is Idle for 2 ms and the B_SESS_END bit is set, the B device can perform an SRP.	Go to B_SRP_INIT Pulse CHRG_VBUS Pulse DP_HIGH 5-10 ms
B_SRP_INIT	If ID\ Interrupt or SRP Done (SRP must be done in less than 100 msecs.)	Go to B_IDLE
B_PERIPHERAL	If HNP enabled and the bus is suspended and B wants the bus, the B device can become the host.	Go to B_WAIT_ACON Turn off DP_HIGH
B_WAIT_ACON	If A connects, an attach interrupt is received	Go to B_HOST Turn on Host Mode
	If ID\ Interrupt or B_SESS_VLD/ Interrupt If the cable changes or if VBUS goes away, the host doesn't support us. Go to B_IDLE	Go to B_IDLE
	If 3.125 ms expires or if a Resume occurs	Go to B_PERIPHERAL
B_HOST	If ID\ Interrupt or B_SESS_VLD\ Interrupt If the cable changes or if VBUS goes away, the host doesn't support us.	Go to B_IDLE
	If B application is done or A disconnects	Go to B_PERIPHERAL

48.1.2 FlexCAN Module Features

The FlexCAN module includes these distinctive legacy features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mb/sec
  - Content-related addressing
- Flexible Mailboxes of zero to eight bytes data length
- Each Mailbox configurable as Rx or Tx, all supporting standard and extended messages
- Individual Rx Mask Registers per Mailbox
- Full featured Rx FIFO with storage capacity for up to 6 frames and automatic internal pointer handling
- Transmission abort capability
- Programmable clock source to the CAN Protocol Interface, either bus clock or crystal oscillator
- Unused structures space can be used as general purpose RAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)

Chapter 50
Inter-Integrated Circuit (I2C)

50.1 Introduction

NOTE

For the chip-specific implementation details of this module's instances see the chip configuration chapter.

The inter-integrated circuit (I^2C, I2C, or IIC) module provides a method of communication between a number of devices. The interface is designed to operate up to 100 kbit/s with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF. The I2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

50.1.1 Features

The I2C module has the following features:

- Compatible with *The I^2C-Bus Specification*
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation and detection
- Repeated START signal generation and detection
- Acknowledge bit generation and detection
- Bus busy detection
- General call recognition

I2Cx_S field descriptions (continued)

Field	Description
	0 Not addressed 1 Addressed as a slave
5 BUSY	Bus busy Indicates the status of the bus regardless of slave or master mode. This bit is set when a START signal is detected and cleared when a STOP signal is detected. 0 Bus is idle 1 Bus is busy
4 ARBL	Arbitration lost This bit is set by hardware when the arbitration procedure is lost. The ARBL bit must be cleared by software, by writing a one to it. 0 Standard bus operation. 1 Loss of arbitration.
3 RAM	Range address match This bit is set by any of the following conditions: • Any nonzero calling address is received that matches the address in the RA register. • The RMEN bit is set and the calling address is within the range of values of the A1 and RA registers. Writing the C1 register with any value clears this bit. 0 Not addressed 1 Addressed as a slave
2 SRW	Slave read/write When addressed as a slave, SRW indicates the value of the R/$\overline{W}$ command bit of the calling address sent to the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IICIF	Interrupt flag This bit sets when an interrupt is pending. This bit must be cleared by software or by writing a 1 to it in the interrupt routine. One of the following events can set this bit: • One byte transfer including ACK/NACK bit completes if FACK = 0 • One byte transfer excluding ACK/NACK bit completes if FACK = 1. An ACK or NACK is sent on the bus by writing 0 or 1 to TXAK after this bit is set in receive mode • Match of slave address to calling address including primary slave address, range slave address, alert response address, second slave address, or general call address. • Arbitration lost • In SMBus mode, any timeouts except SCL and SDA high timeouts 0 No interrupt pending 1 Interrupt pending
0 RXAK	Receive acknowledge

Table continues on the next page...

If receive FIFO 0 is enabled and receive interrupt enable (IER[RIE]) and received FIFO 0 full enable (IER[RDR0EN]) bits are set, receive interrupt 0 occurs when the received data word is transferred to the receive FIFO 0 and receive FIFO 0 reaches the selected threshold. This results in receive FIFO full 0 (RFF0) flag to set.

The core has to read the data from the receive data register 0 (RX0) (if receive FIFO 0 is disabled) before a new data word is transferred from the receive shift register (RXSR). Otherwise, the receive overrun error 0 (IER[ROE0EN]) bit is set. If receive FIFO 0 is enabled, the receive overrun error 0 (ROE0) bit sets when the receive FIFO 0 data level reaches the selected threshold and a new data word is ready to transfer to the receive FIFO 0.

The following figure shows transmitter and receiver timing for an 8-bit word in the first time slot in normal mode and continuous clock with a late word length frame sync. The transmit data register is loaded with the data to be transmitted. On arrival of the clock, this data is transferred to the transmit shift register which is transmitted on arrival of the frame-sync on the STXD output. Simultaneously, the receive shift register shifts in the received data available on the SRXD input. At the end of the time slot, this data is transferred to the receive data register.

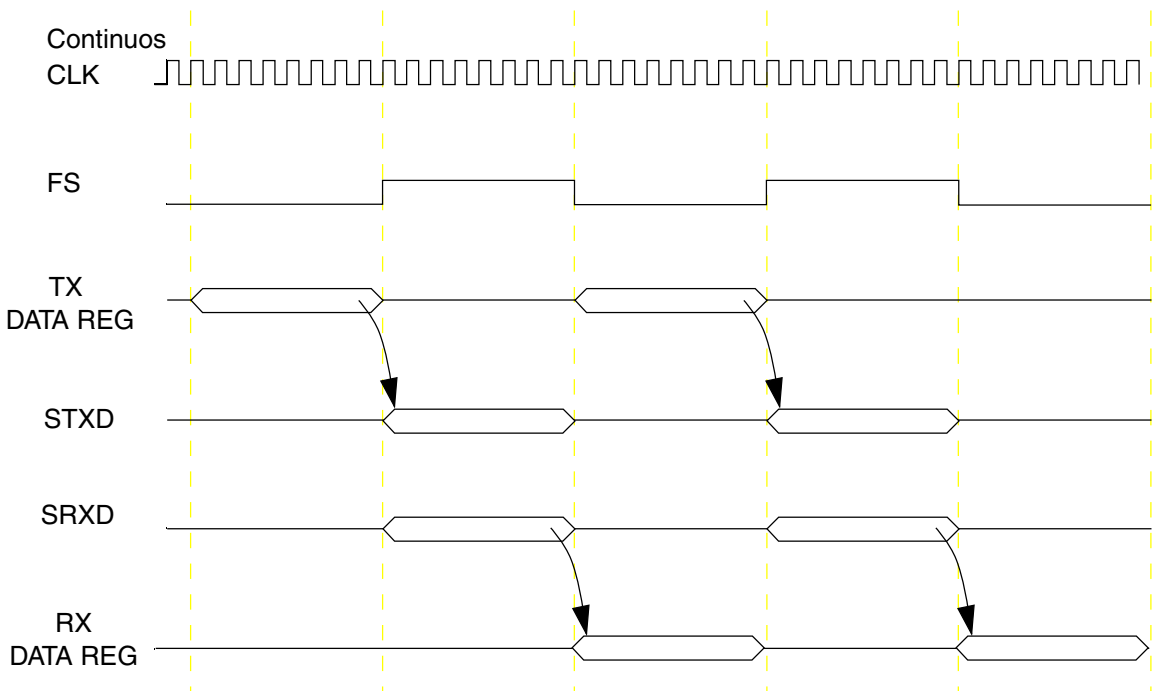
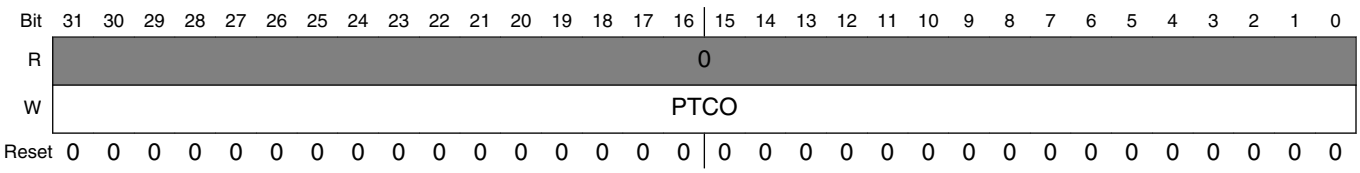


Figure 53-46. Normal mode timing - continuous clock

The following figure shows a similar case for internal (I^2S generates clock) gated clock mode.

54.2.3 Port Clear Output Register (GPIOx_PCOR)

Addresses: GPIOA_PCOR is 400F_F000h base + 8h offset = 400F_F008h
GPIOB_PCOR is 400F_F040h base + 8h offset = 400F_F048h
GPIOC_PCOR is 400F_F080h base + 8h offset = 400F_F088h
GPIOD_PCOR is 400F_F0C0h base + 8h offset = 400F_F0C8h
GPIOE_PCOR is 400F_F100h base + 8h offset = 400F_F108h

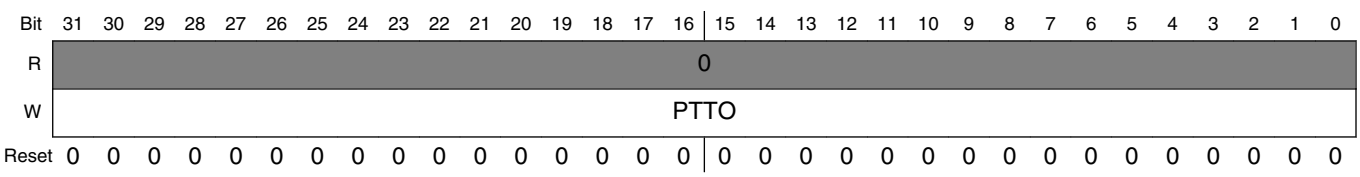


GPIOx_PCOR field descriptions

Field	Description
31–0 PTCO	Port Clear Output Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows: 0 Corresponding bit in PDORn does not change. 1 Corresponding bit in PDORn is set to logic zero.

54.2.4 Port Toggle Output Register (GPIOx_PTOR)

Addresses: GPIOA_PTOR is 400F_F000h base + Ch offset = 400F_F00Ch
GPIOB_PTOR is 400F_F040h base + Ch offset = 400F_F04Ch
GPIOC_PTOR is 400F_F080h base + Ch offset = 400F_F08Ch
GPIOD_PTOR is 400F_F0C0h base + Ch offset = 400F_F0CCh
GPIOE_PTOR is 400F_F100h base + Ch offset = 400F_F10Ch

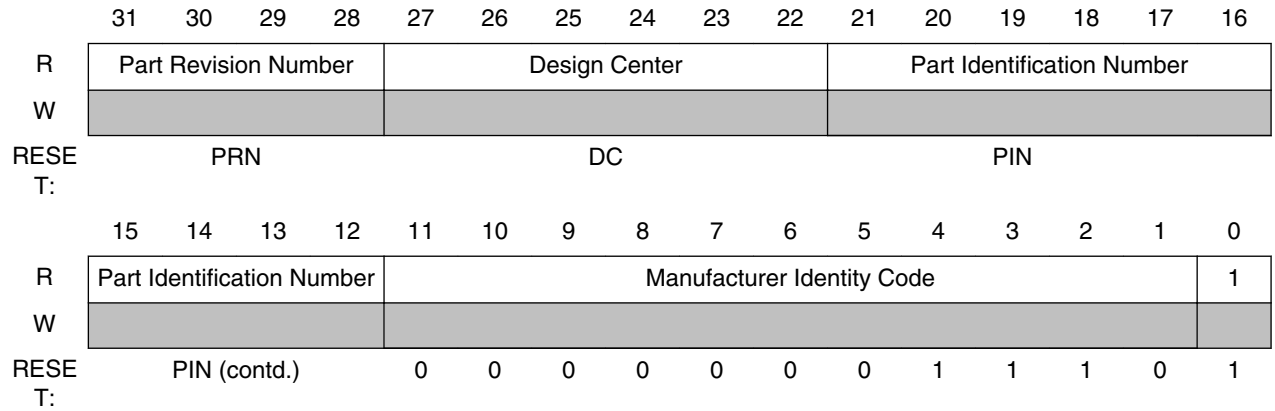


GPIOx_PTOR field descriptions

Field	Description
31–0 PTTO	Port Toggle Output Writing to this register will update the contents of the corresponding bit in the Port Data Output Register (PDOR) as follows:

56.3.3 Device identification register

The device identification (JTAG ID) register, shown in the following figure, allows the revision number, part number, manufacturer, and design center responsible for the design of the part to be determined through the TAP. The device identification register is selected for serial data transfer between TDI and TDO when the IDCODE instruction is active. Entry into the Capture-DR state while the device identification register is selected loads the IDCODE into the shift register to be shifted out on TDO in the Shift-DR state. No action occurs in the Update-DR state.



The following table describes the device identification register functions.

Table 56-2. Device identification register field descriptions

Field	Description
PRN	Part Revision Number. Contains the revision number of the part. Value is 0x0.
DC	Design Center. Indicates the design center. Value is 0x2C.
PIN	Part Identification Number. Contains the part number of the device. Value is TBD.
MIC	Manufacturer Identity Code. Contains the reduced Joint Electron Device Engineering Council (JEDEC) ID. Value is 0x00E .
IDCODE ID	IDCODE Register ID. Identifies this register as the device identification register and not the bypass register. Always set to 1.

56.3.4 Boundary scan register

The boundary scan register is connected between TDI and TDO when the EXTEST, SAMPLE or SAMPLE/PRELOAD instructions are active. It is used to capture input pin data, force fixed values on output pins, and select a logic value and direction for bidirectional pins. Each bit of the boundary scan register represents a separate boundary

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