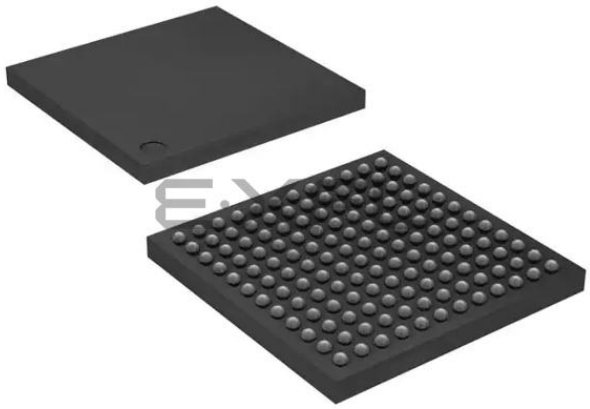

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	104
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 46x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx128zvmd10r

Table 40. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2)} + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2)$ Ø 4	É	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2)$ Ø 4	É	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	É	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	É	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	É	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	É	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

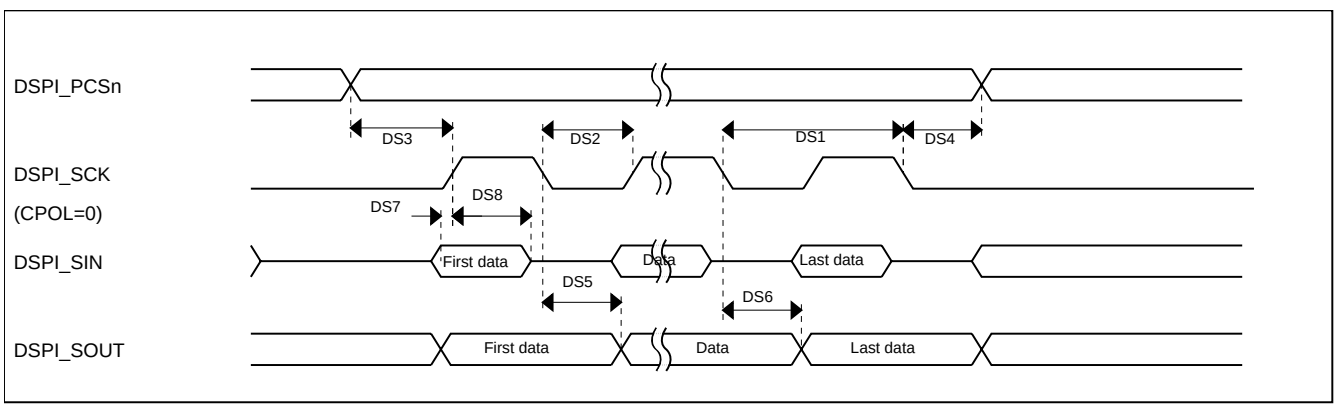

Figure 21. DSPI classic SPI timing ° master mode

Table 41. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	É	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	É	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2)} + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	É	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	É	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	É	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	É	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	É	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	É	19	ns

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
35	K3	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	ADC1_SE16/ CMP2_IN2/ ADC0_SE22								
36	J3	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	ADC0_SE16/ CMP1_IN2/ ADC0_SE21								
37	M3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
38	L3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
39	L4	DAC1_OUT/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP2_IN3/ ADC1_SE23	DAC1_OUT/ CMP2_IN3/ ADC1_SE23								
40	M7	XTAL32	XTAL32	XTAL32								
41	M6	EXTAL32	EXTAL32	EXTAL32								
42	L6	VBAT	VBAT	VBAT								
43	É	VDD	VDD	VDD								
44	É	VSS	VSS	VSS								
45	M4	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_b		
46	K5	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX			EWM_IN		
47	K4	PTE26	DISABLED		PTE26		UART4_CTS_ b			RTC_CLKOUT		
48	J4	PTE27	DISABLED		PTE27		UART4_RTS_ b					
49	H4	PTE28	DISABLED		PTE28							
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_ BCLK	JTAG_TRST	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3				TRACE_ CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4				TRACE_D3	

144 LQFP	144 MAP BGA	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
117	A7	PTC12			PTC12		UART4_RTS_b		FB_AD27			
118	D6	PTC13			PTC13		UART4_CTS_b		FB_AD26			
119	C6	PTC14			PTC14		UART4_RX		FB_AD25			
120	B6	PTC15			PTC15		UART4_TX		FB_AD24			
121	É	VSS	VSS	VSS								
122	É	VDD	VDD	VDD								
123	A6	PTC16			PTC16	CAN1_RX	UART3_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b			
124	D5	PTC17			PTC17	CAN1_TX	UART3_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b			
125	C5	PTC18			PTC18		UART3_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b			
126	B5	PTC19			PTC19		UART3_CTS_b		FB_CS3_b/ FB_BE7_0_b	FB_TA_b		
127	A5	PTD0/ LLWU_P12			PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b		FB_ALE/ FB_CS1_b/ FB_TS_b			
128	D4	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b		FB_CS0_b			
129	C4	PTD2/ LLWU_P13			PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX		FB_AD4			
130	B4	PTD3			PTD3	SPI0_SIN	UART2_TX		FB_AD3			
131	A4	PTD4/ LLWU_P14			PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN		
132	A3	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b		
133	A2	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
134	M10	VSS	VSS	VSS								
135	F8	VDD	VDD	VDD								
136	A1	PTD7			PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
137	C9	PTD8	DISABLED		PTD8	I2C0_SCL	UART5_RX			FB_A16		
138	B9	PTD9	DISABLED		PTD9	I2C0_SDA	UART5_TX			FB_A17		
139	B3	PTD10	DISABLED		PTD10		UART5_RTS_b			FB_A18		
140	B2	PTD11	DISABLED		PTD11	SPI2_PCS0	UART5_CTS_b	SDHC0_ CLKIN		FB_A19		
141	B1	PTD12	DISABLED		PTD12	SPI2_SCK		SDHC0_D4		FB_A20		
142	C3	PTD13	DISABLED		PTD13	SPI2_SOUT		SDHC0_D5		FB_A21		

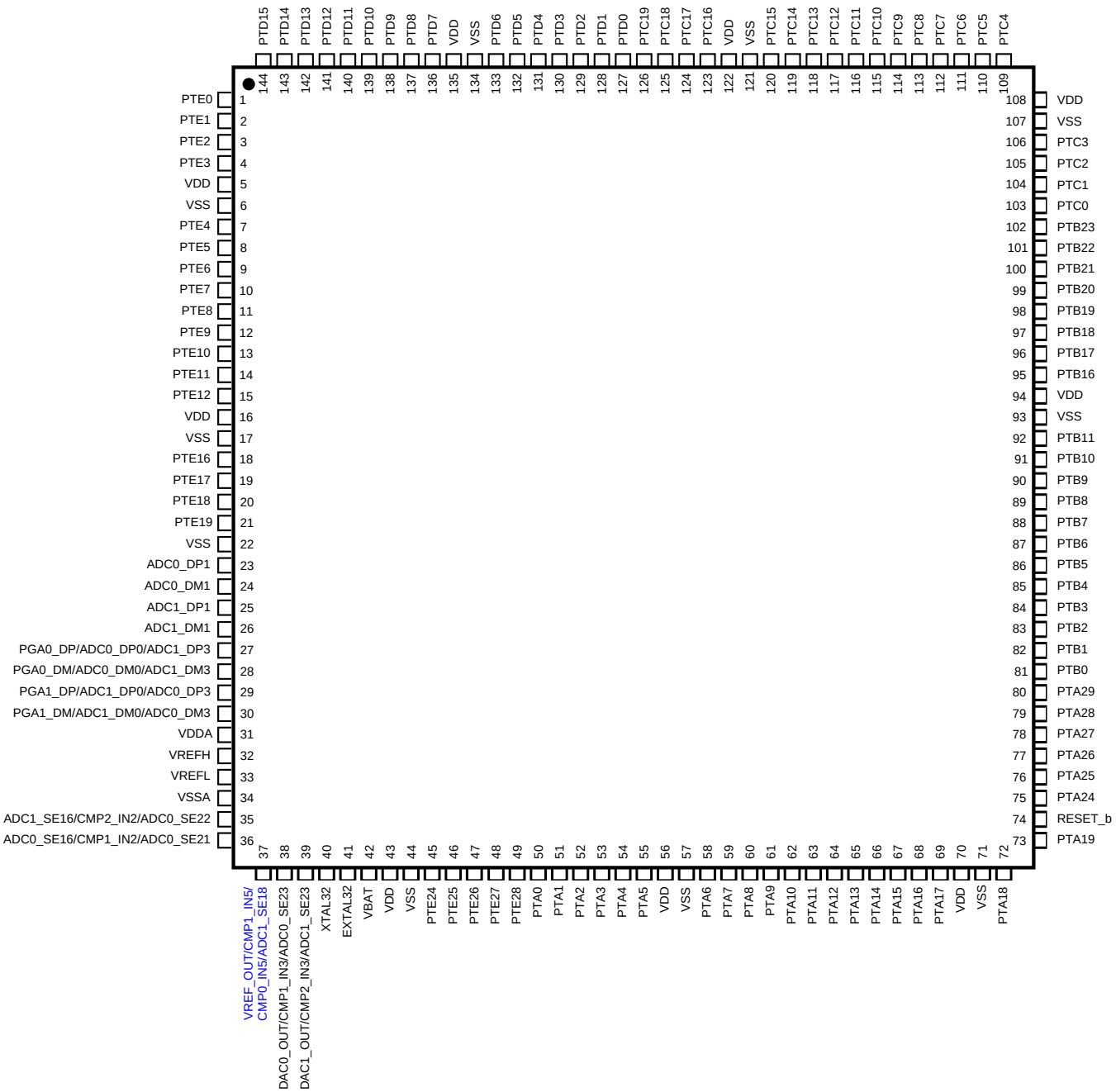

Figure 27. K10 144 LQFP Pinout Diagram

Table 49. Revision History (continued)

Rev. No.	Date	Substantial Changes
6	01/2012	µ Added AC electrical specifications. µ Replaced TBDs with silicon data throughout. µ In "Power mode transition operating behaviors" table, removed entry times. µ Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. µ Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". µ Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. µ Updated I_{DD_RUN} numbers in ×Power consumption operating behaviors× section. µ Clarified ×Diagram: Typical IDD_RUN operating behavior× section and updated ×Run mode supply current vs. core frequency É all peripheral clocks disabled× figure. µ In ×Voltage reference electrical specifications× section, updated I_L, C, V_{tdrift}, and V_{vdrift} values.
7	02/2013	µ In "ESD handling ratings", added a note for I_{LAT}. µ Updated "Voltage and current operating requirements". µ Updated "Voltage and current operating behaviors". µ Updated "Power mode transition operating behaviors". µ Updated "EMC radiated emissions operating behaviors" to add MAPBGA data. µ In "MCG specifications", updated the description of f_{ints_t}. µ In "16-bit ADC operating conditions", updated the max spec of V_{ADIN}. µ In "16-bit ADC electrical characteristics", updated the temp sensor slope and voltage specs. µ Updated "I2C switching specifications". µ In "SDHC specifications", removed the operating voltage limits and updated the SD1 and SD6 specs. µ In "I2S switching specifications", added separate specification tables for the full operating voltage range.

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Document Number: K10P144M100SF2
Rev. 7, 02/2013

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