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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54605j256et100e

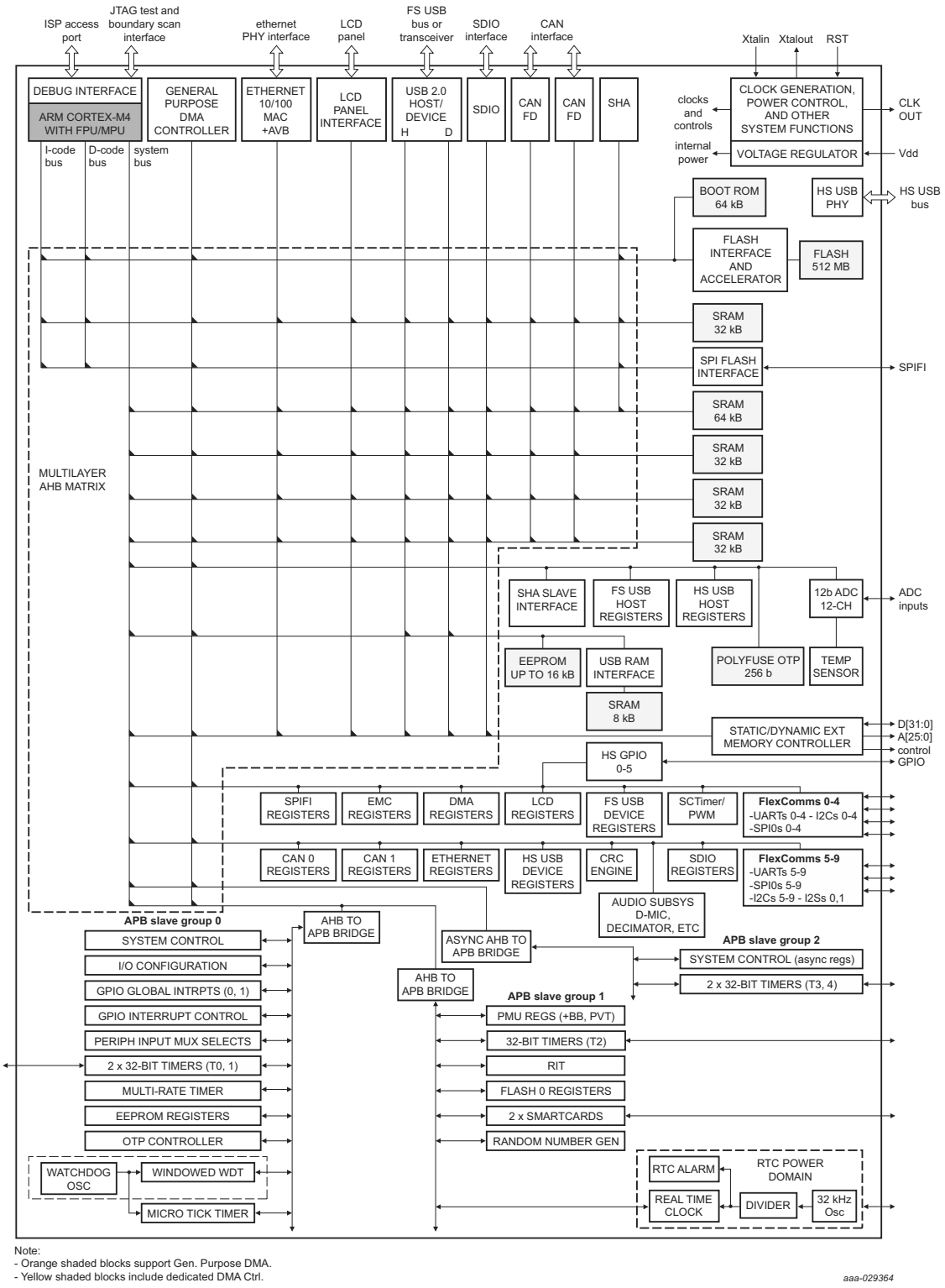

Fig 4. LPC546xx Block diagram

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_14	A9	C12	160	78	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B5	B7	187	88	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
								R — Reserved.
							O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	H8	N12	98	47	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_18	D2	D1	15	5	[2]	PU	I/O	**PIO1_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							I	**CAN1_RD —** Receiver input for CAN 1.
							O	**EMC_BLSN[1] —** External memory interface byte lane select 1 (active low).
PIO1_19	F3	L1	33	16	[2]	PU	I/O	**PIO1_19 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I/O	**EMC_D[8] —** External Memory interface data [8].
PIO1_20	G2	M1	35	17	[2]	PU	I/O	**PIO1_20 —** General-purpose digital input/output pin.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**CT3_CAP2 —** Capture 2 input to Timer 3.
								R — Reserved.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	K6	N8	74	37	[2]	PU	I/O	**PIO1_21 —** General-purpose digital input/output pin.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
								R — Reserved.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**EMC_D[10] —** External Memory interface data [10].

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_29	-	L13	112	-	[2]	PU	I/O	**PIO3_29 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[18] —** External memory interface address 18.
PIO3_30	-	K13	116	-	[2]	PU	I/O	**PIO3_30 —** General-purpose digital input/output pin.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[19] —** External memory interface address 19.
PIO3_31	-	J14	123	-	[2]	PU	I/O	**PIO3_31 —** General-purpose digital input/output pin.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
								R — Reserved.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**EMC_A[20] —** External memory interface address 20.
PIO4_0	-	H13	127	-	[2]	PU	I/O	**PIO4_0 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
								R — Reserved.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							O	**EMC_CSN[1] —** External memory interface static chip select 1(active low).

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_31	-	-	114	-	[2]	PU	I/O	**PIO4_31 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
							I/O	**EMC_D[26] —** External Memory interface data [26].
PIO5_0	-	-	122	-	[2]	PU	I/O	**PIO5_0 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I/O	**EMC_D[27] —** External Memory interface data [27].
PIO5_1	-	-	126	-	[2]	PU	I/O	**PIO5_1 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**EMC_D[28] —** External Memory interface data [28].
PIO5_2	-	-	202	-	[2]	PU	I/O	**PIO5_2 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I/O	**EMC_D[29] —** External Memory interface data [29].

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO5_3	-	-	129	-	[2]	PU	I/O	**PIO5_3 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I/O	**EMC_D[30] —** External Memory interface data [30].
PIO5_4	-	-	135	-	[2]	PU	I/O	**PIO5_4 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							I	**CT3_CAP2 —** Capture input 2 to Timer 3.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
							I/O	**EMC_D[31] —** External Memory interface data [31].
PIO5_5	-	-	145	-	[2]	PU	I/O	**PIO5_5 —** General-purpose digital input/output pin.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**TRACECLK —** Trace clock.
							O	**EMC_A[21] —** External memory interface address 21.
PIO5_6	-	-	152	-	[2]	PU	I/O	**PIO5_6 —** General-purpose digital input/output pin.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**TRACEDATA[0] —** Trace data bit 0.
							O	**EMC_A[22] —** External memory interface address 22.

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO5_7	-	-	171	-	[2]	PU	I/O	**PIO5_7 —** General-purpose digital input/output pin.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**TRACEDATA[1] —** Trace data bit 1.
							O	**EMC_A[23] —** External memory interface address 23.
PIO5_8	-	-	175	-	[2]	PU	I/O	**PIO5_8 —** General-purpose digital input/output pin.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**TRACEDATA[2] —** Trace data bit 2.
							O	**EMC_A[24] —** External memory interface address 24.
PIO5_9	-	-	179	-	[2]	PU	I/O	**PIO5_9 —** General-purpose digital input/output pin.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
							O	**TRACEDATA[3] —** Trace data bit 3.
							O	**EMC_A[25] —** External memory interface address 25.
PIO5_10	-	-	168	-	[2]	PU	I/O	**PIO5_10 —** General-purpose digital input/output pin.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
USB1_AVSSC	D1	F2	20	6				USB1 analog 3.3 V ground.
USB1_REXT	B1	F1	21	7				USB1 analog signal for reference resistor, 12.4 kΩ +/-1%
USB1_ID	C1	G1	22	8				Indicates to the transceiver whether connected as an A-device (USB1_ID LOW) or B-device (USB1_ID HIGH).
USB1_VBUS	D3	G2	23	9	[6][8]		I/O	VBUS pin (power on USB cable).

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Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
USB1_AVDDC3V3	E1	G3	24	10				USB1 analog 3.3 V supply.
USB1_AVDDTX3V3	E2	H1	25	11				USB1 analog 3.3 V supply for line drivers.
USB1_DP	F2	H3	27	13	[6]		I/O	USB1 bidirectional D+ line.
USB1_DM	E3	H2	26	12	[6]		I/O	USB1 bidirectional D- line.
USB1_AVSSTX3V3	G1	J1	28	14				USB1 analog ground for line drivers.
USB0_DP	B3	E5	204	97	[6]		I/O	USB0 bidirectional D+ line.
USB0_DM	B2	D5	205	98	[6]		I/O	USB0 bidirectional D- line.
RESETN	J8	N13	101	48	[5]			External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.
VDD	D5; D7; E4; E6; F5; F7; G4; G6	E6; E8; F5; G5; J12; L6; L11	1; 48; 65; 104; 108; 156; 157; 206	1; 21; 33; 50; 54; 75; 76; 99		-	-	Single 1.71 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	D4; D6; E5; E7; F4; F6; G5; G7	B3; D7; D8; E11; H5; J5; K7	2; 49; 66; 103; 107; 148; 162; 201	2; 22; 34; 49; 53; 71; 79; 96		-	-	Ground.
VDDA	J4	N6	64	32		-	-	Analog supply voltage.
VREFN	-	N4	59	-		-	-	ADC negative reference voltage. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
VREFP	K4	P6	63	31		-	-	ADC positive reference voltage.
VSSA	H4	L5	60	30		-	-	Analog ground. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
XTALIN	H2	K4	41	20	[7]	-	-	Main oscillator input.
XTALOUT	G3	J4	40	19	[7]	-	-	Main oscillator output.
VBAT	K9	N11	94	45		-	-	Battery supply voltage. If no battery is used, tie VBAT to VDD or to ground.
RTCXIN	J9	L12	105	51		-	-	RTC oscillator input.
RTCXOUT	H9	K11	106	52		-	-	RTC oscillator output.

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Table 9 shows wake-up sources for reduced power modes.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.
Deep-sleep	Pin interrupts	Enable pin interrupts in NVIC and STARTER0 and/or STARTER1 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTER0 registers. • Enable interrupt in BODCTRL register. • Configure the BOD to keep running in this mode with the power API.
	BOD reset	Enable reset in BODCTRL register.
	Watchdog interrupt	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog interrupt in NVIC and STARTER0 registers. • Enable the watchdog in the WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • Configure the WDTOSC to keep running in this mode with the power API.
	Watchdog reset	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog and watchdog reset in the WWDT MOD register and feed.
	Reset pin	Always available.
	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register. • Enable the RTCALARM interrupt in the STARTER0 register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTC CTRL register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC. • Enable the RTC wake-up interrupt in the STARTER0 register.
	Micro-tick timer (intended for ultra-low power wake-up from deep-sleep mode	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the Micro-tick timer clock by writing to the AHBCLKCTRL1 register. • Start the Micro-tick timer by writing UTICK CTRL register. • Enable the Micro-tick timer interrupt in the STARTER0 register.
	I2C interrupt	Interrupt from I2C in slave mode.
	SPI interrupt	Interrupt from SPI in slave mode.
	USART interrupt	Interrupt from USART in slave or 32 kHz mode.
	USB0 need clock interrupt	Interrupt from USB0 when activity is detected that requires a clock.
	USB1 need clock interrupt	Interrupt from USB1 when activity is detected that requires a clock.
	Ethernet interrupt	Interrupt from ethernet.
	DMA interrupt	Interrupt from DMA.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.

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10. Static characteristics

10.1 General operating conditions

Table 12. General operating conditions

T_{amb} = –40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	CPU clock frequency		[3]	-	-	220	MHz
	CPU clock frequency	For USB high-speed device and host operations	[3]	60	-	220	MHz
	CPU clock frequency	For USB full-speed device and host operations	[3]	12	-	220	MHz
		For OTP programming only		-	-	12	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For OTP programming only	[2]	2.7	-	3.6	V
		For USB operation only		3.0	-	3.6	V
V_{DDA}	analog supply voltage			1.71	-	3.6	V
V_{BAT}	battery supply voltage			1.71	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
T_{amb}	Temperature	For EEPROM operation		–40.0	-	+85	°C
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		-0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		-0.5	-	+3.6	V
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		–0.5	-	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		–0.5	-	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Attempting to program below 2.7 V will result in unpredictable results and the part might enter an unrecoverable state.

[3] The LPC5460x/61x operates at CPU frequencies of up to 180 MHz. The LPC54628 operates at CPU frequencies of up to 220 MHz.

10.2 Power-up ramp conditions

Table 13. Power-up characteristics[1]

T_{amb} = –40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1<V_{DD}<V_2$)		-	-	170	μs
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.62	V

[1] Assert the external reset pin until V_{DD} is > 1.62 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

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Table 20. Typical AHB/APB peripheral power consumption [3][4][5]
T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz[2]**	**CPU: 96 MHz, Async APB bus: 12 MHz[2]**	**CPU: 180 MHz, Async APB bus: 12 MHz[2]**	**CPU: 220 MHz, Async APB bus: 12 MHz[2]**
Timer3		0.9	0.9	0.9	0.9	1.2
Timer4		0.9	0.9	0.9	0.9	1.2

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz, 180 MHz, and 220 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.5 Pin characteristics

Table 21. Static characteristics: pin characteristics
T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$\overline{\text{RESET}}$ pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} > 1.8 V	[3]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V
Output characteristics							

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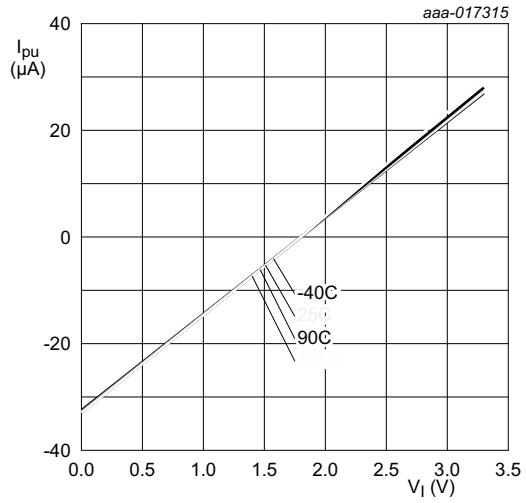
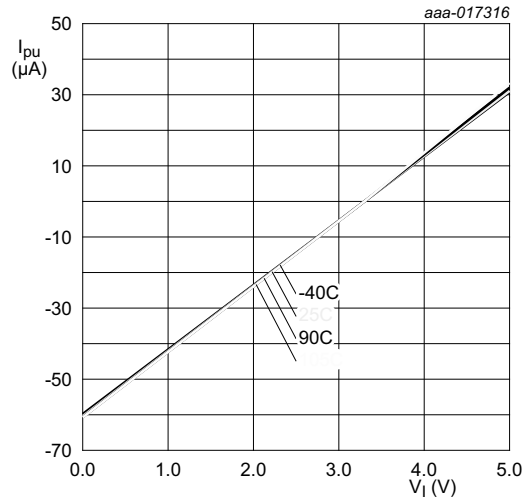
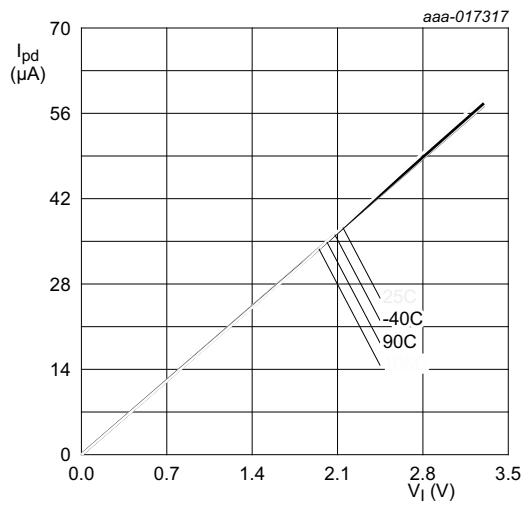


Conditions: V_{DD} = 1.8 V; on standard port pins.

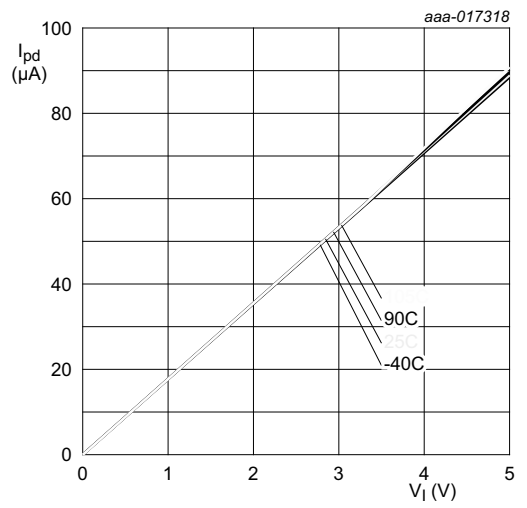


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 22. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 23. Typical pull-down current I_{PD} versus input voltage V_I

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11.3 I/O pins

Table 24. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (Fast-mode);	[2][3]				
		2.7 V ≤ V_{DD} <= 3.6 V		1.0	-	2.5	ns
		1.71 V ≤ V_{DD} <= 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (Fast-mode);	[2][3]				
		2.7 V ≤ V_{DD} <= 3.6 V		0.9	-	2.5	ns
		1.71 V ≤ V_{DD} <= 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.71 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.71 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data, not tested in production.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC546xx user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

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11.5 External memory interface

Table 26. Dynamic characteristics: Static external memory interface

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.4+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−1.6	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−6.7 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−4.8	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.8	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1.0	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.6	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.2	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	2.5	-	5.5	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6	-	2.9	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.6	-	0.9	ns

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[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM10912* LPC546xx *manual*).

[3] Latest of address valid, $\overline{\text{EMC_CSx}}$ LOW, $\overline{\text{EMC_OE}}$ LOW, $\overline{\text{EMC_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC_CSx}}$ HIGH, $\overline{\text{EMC_OE}}$ HIGH, $\overline{\text{EMC_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC_CSx}}$ HIGH, $\overline{\text{EMC_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM10912* LPC546xx *manual*).

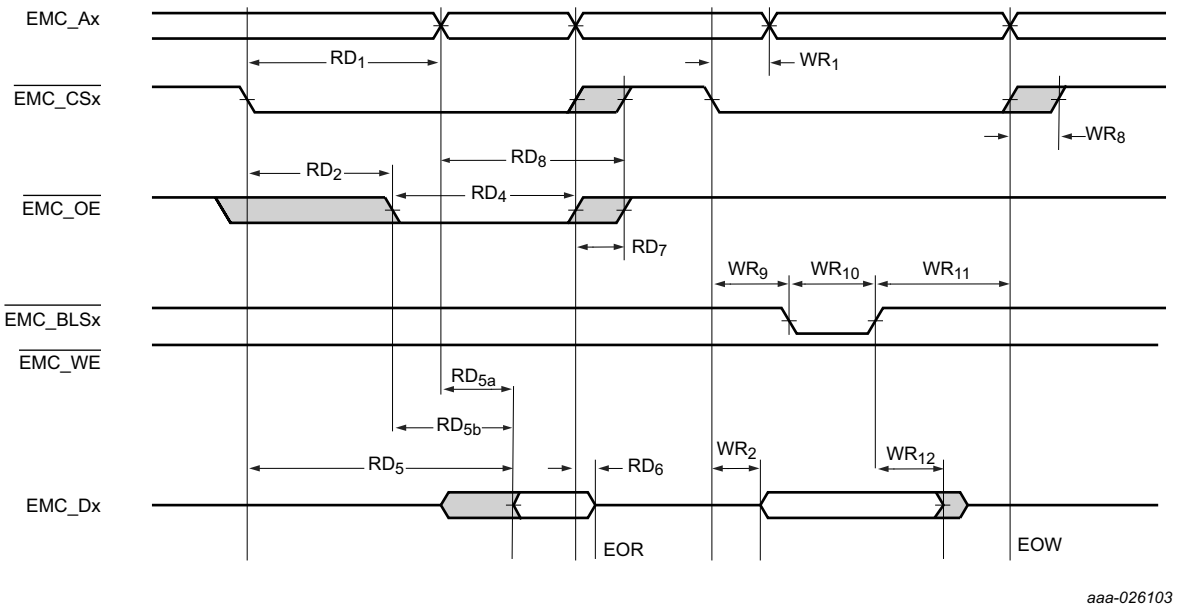

Fig 24. External static memory read/write access (PB = 0)

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11.13 I²C-bus

Table 41. Dynamic characteristic: I²C-bus pins[1]

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	Both SDA and SCL signals Standard-mode	-	300	ns
			Fast-mode	20 + 0.1 × C_b	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	μs
			Fast-mode	1.3	-	μs
			Fast-mode Plus	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	μs
			Fast-mode	0.6	-	μs
			Fast-mode Plus	0.26	-	μs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	μs
			Fast-mode	0	-	μs
			Fast-mode Plus	0	-	μs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] Guaranteed by design. Not tested in production.

[2] Parameters are valid over operating temperature range unless otherwise specified. See the I²C-bus specification *UM10204* for details.

[3] tHD;DAT is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF. If mixed with Hs-mode devices, faster fall times are allowed.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] tSU;DAT is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

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13.5 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See Figure 46.

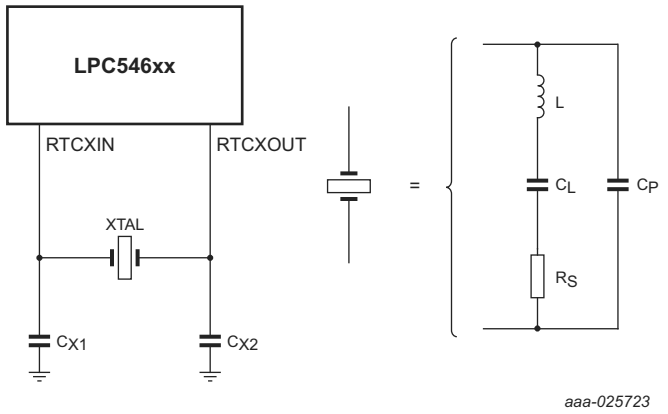

Fig 46. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

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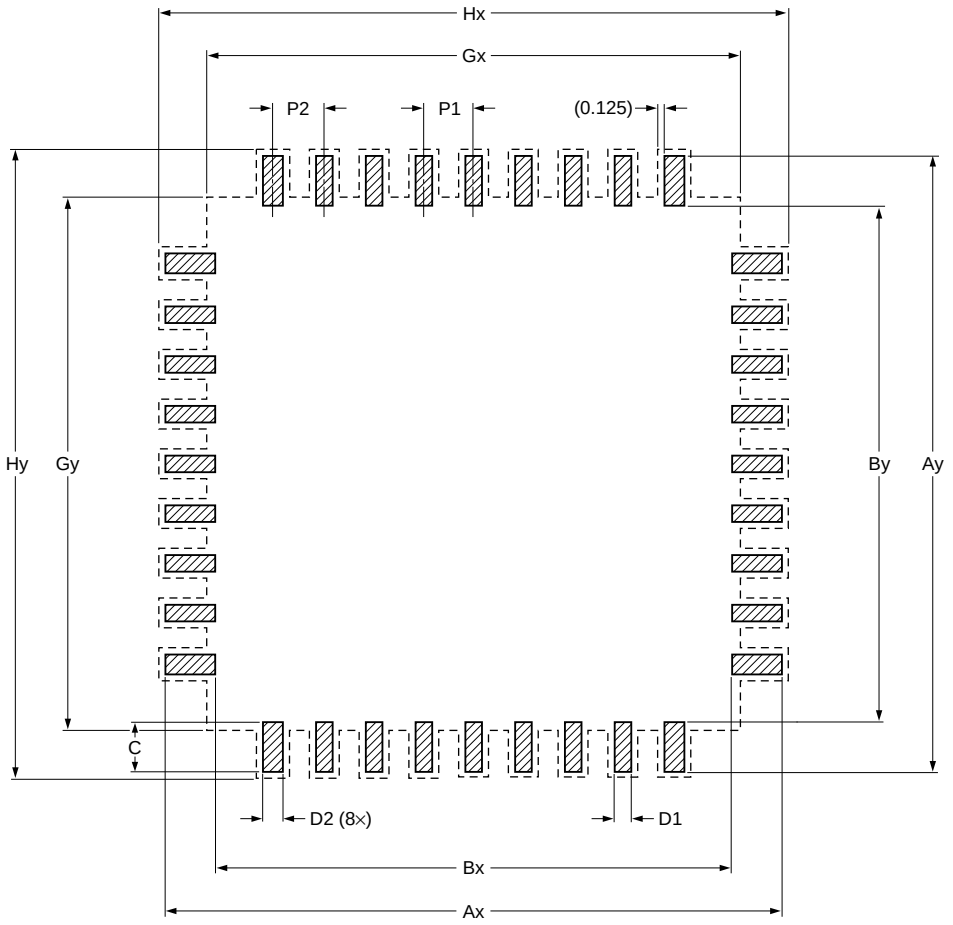
15. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 54. Reflow soldering of the LQFP208 package

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18. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC546xx v.2.5	20180620	Product data sheet		LPC546xx v.2.4
Modifications:	• Updated Figure 14 “Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX” • Updated Table 14 “CoreMark score[1]”. • Updated Table 4 “Pin description”: Description of VREFN and VSSA. • Updated Table 5 “Termination of unused pins”: Added USB1_ID pin.			
LPC546xx v.2.4	20180524	Product data sheet	201805030I	LPC546xx v.2.3
Modifications:	• Added text to serial interfaces to Section 2 “Features and benefits”: USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00032 for more details. • Added table note 2 of Section 6.2.2 “Pin states in different power modes”: If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage. • Added table note 3 to Table 18 “Static characteristics: Power consumption in deep power-down mode”: If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage. • Added remark to Figure 16 “Deep-sleep mode: Typical supply current IDD versus temperature for different supply voltages VDD”: At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage. • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: I_{DD} supply current, Deep-sleep mode; Flash is powered down for SRAMX (32 KB) powered T_{amb} = 25 °C and T_{amb} = 105 °C; Max values: 69 μA and 1150 μA. Updated table note 3: Tested in production. VDD = 1.71 V. At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage. • Updated Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: I_{DD} supply current, Deep-sleep mode; Flash is powered down for SRAMX (32 KB) powered T_{amb} = 25 °C; Max value: 69 μA.			
LPC546xx v.2.3	20180426	Product data sheet	-	LPC546xx v.2.2
Modifications:	• Updated Table 4 “Pin description”: VREFN and VSSA.			
LPC546xx v.2.2	20180417	Product data sheet	-	LPC546xx v.2.1
Modifications:	• Updated Table 25 “Dynamic characteristic: Typical wake-up times from low power modes”: Changed t_{wake} at typical for deep-sleep mode to 150 μs. Was 19 μs.			
LPC546xx v.2.1	20180206	Product data sheet	-	LPC546xx v.2.0
Modifications:	• Updated Figure 3 “LQFP100 package marking”. • Fixed Figure 4 “LPC546xx Block diagram” figure number identifier. • Fixed Figure 9 “LPC546xx Memory mapping” figure number identifier.			
LPC546xx v.2.0	20180126	Product data sheet	-	LPC546xx v.1.9

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