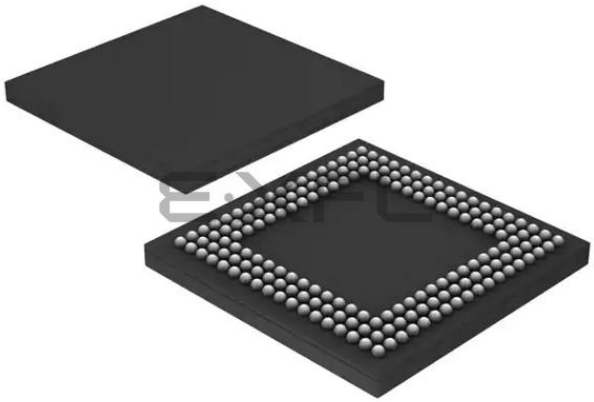

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	145
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54605j256et180e

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_9	E10	G12	136	65	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
							I/O	**EMC_D[7] —** External Memory interface data [7].
PIO0_10/ ADC0_0	J1	P2	50	23	[4]	PU	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	K1	L3	51	24	[4]	PU	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
								R — Reserved.
								R — Reserved.
							I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.

Table 4. Pin description *…continued*

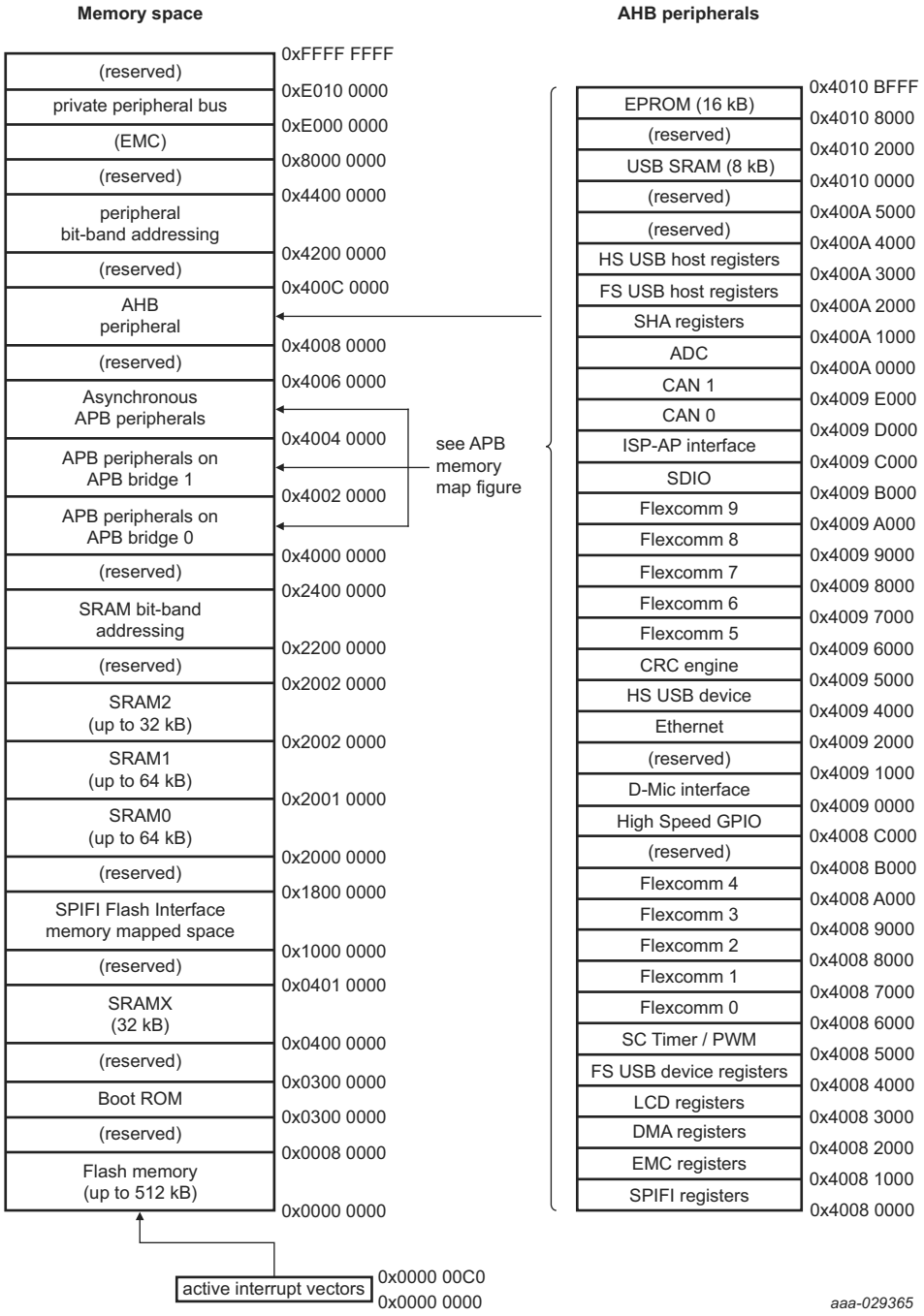
Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_19	-	P12	93	-	[2]	PU	I/O	**PIO2_19 —** General-purpose digital input/output pin.
							O	**LCD_VD[1] —** LCD Data [1].
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
PIO2_20	-	P13	95	-	[2]	PU	I/O	**PIO2_20 —** General-purpose digital input/output pin.
							O	**LCD_VD[2] —** LCD Data [2].
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
PIO2_21	-	L10	99	-	[2]	PU	I/O	**PIO2_21 —** General-purpose digital input/output pin.
							O	**LCD_VD[3] —** LCD Data [3].
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	-	K10	113	-	[2]	PU	I/O	**PIO2_22 —** General-purpose digital input/output pin.
							O	**LCD_VD[4] —** LCD Data [4].
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
								R — Reserved.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
PIO2_23	-	M14	115	-	[2]	PU	I/O	**PIO2_23 —** General-purpose digital input/output pin.
							O	**LCD_VD[5] —** LCD Data [5].
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
PIO2_24	-	K14	118	-	[2]	PU	I/O	**PIO2_24 —** General-purpose digital input/output pin.
							O	**LCD_VD[6] —** LCD Data [6].
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
PIO2_25	-	J11	121	-	[2][8]	PU	I/O	**PIO2_25 —** General-purpose digital input/output pin.
							O	**LCD_VD[7] —** LCD Data [7].
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_26	-	H11	124	-	[2]	PU	I/O	**PIO2_26 —** General-purpose digital input/output pin.
							O	**LCD_VD[8] —** LCD Data [8].
								R — Reserved.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
PIO2_27	-	H14	130	-	[2]	PU	I/O	**PIO2_27 —** General-purpose digital input/output pin.
							O	**LCD_VD[9] —** LCD Data [9].
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
PIO2_28	-	G13	134	-	[2]	PU	I/O	**PIO2_28 —** General-purpose digital input/output pin.
							O	**LCD_VD[10]) —** LCD Data [10].
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
PIO2_29	-	G11	137	-	[2]	PU	I/O	**PIO2_29 —** General-purpose digital input/output pin.
							O	**LCD_VD[11] —** LCD Data [11].
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT2_CAP3 —** Capture 3 input to Timer 2.
							O	**CLKOUT —** Output of the CLKOUT function.
PIO2_30	-	F12	143	-	[2]	PU	I/O	**PIO2_30 —** General-purpose digital input/output pin.
							O	**LCD_VD[12] —** LCD Data [12].
								R — Reserved.
								R — Reserved.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
PIO2_31	-	D14	149	-	[2]	PU	I/O	**PIO2_31 —** General-purpose digital input/output pin.
							O	**LCD_VD[13] —** LCD Data [13].
PIO3_0	-	D12	155	-	[2]	PU	I/O	**PIO3_0 —** General-purpose digital input/output pin.
							O	**LCD_VD[14] —** LCD Data [14].
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.



The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

Fig 9. LPC546xx Memory mapping

7.19.6 Repetitive Interrupt Timer (RIT)

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.19.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Can be used for ETM debug time stamping.

7.20 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.20.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz[2]**	**CPU: 96 MHz, Async APB bus: 12 MHz[2]**	**CPU: 180 MHz, Async APB bus: 12 MHz[2]**	**CPU: 220 MHz, Async APB bus: 12 MHz[2]**
Timer3		0.9	0.9	0.9	0.9	1.2
Timer4		0.9	0.9	0.9	0.9	1.2

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz, 180 MHz, and 220 MHz.

[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.5 Pin characteristics

Table 21. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} > 1.8 V	[3]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V
Output characteristics							

Table 28. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 3.7	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.7	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 4.1	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.8	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 4.4	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.9	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 5.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 4.8	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.7	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	8.1	ns
$t_{h(Q)}$	data output hold time		−1.7	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 30 for internal programmable delay.

11.14 I²S-bus interface

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
Master; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		26.0	-	40.3	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.0	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		26.0	-	41.0	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.6	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		6.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		6.4	-	-	ns
Slave; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		18.8	-	37.1	ns
		100 MHz < CCLK ≤ 180 MHz		18.0	-	35.5	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.8	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.4	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		3.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.2	-	-	ns

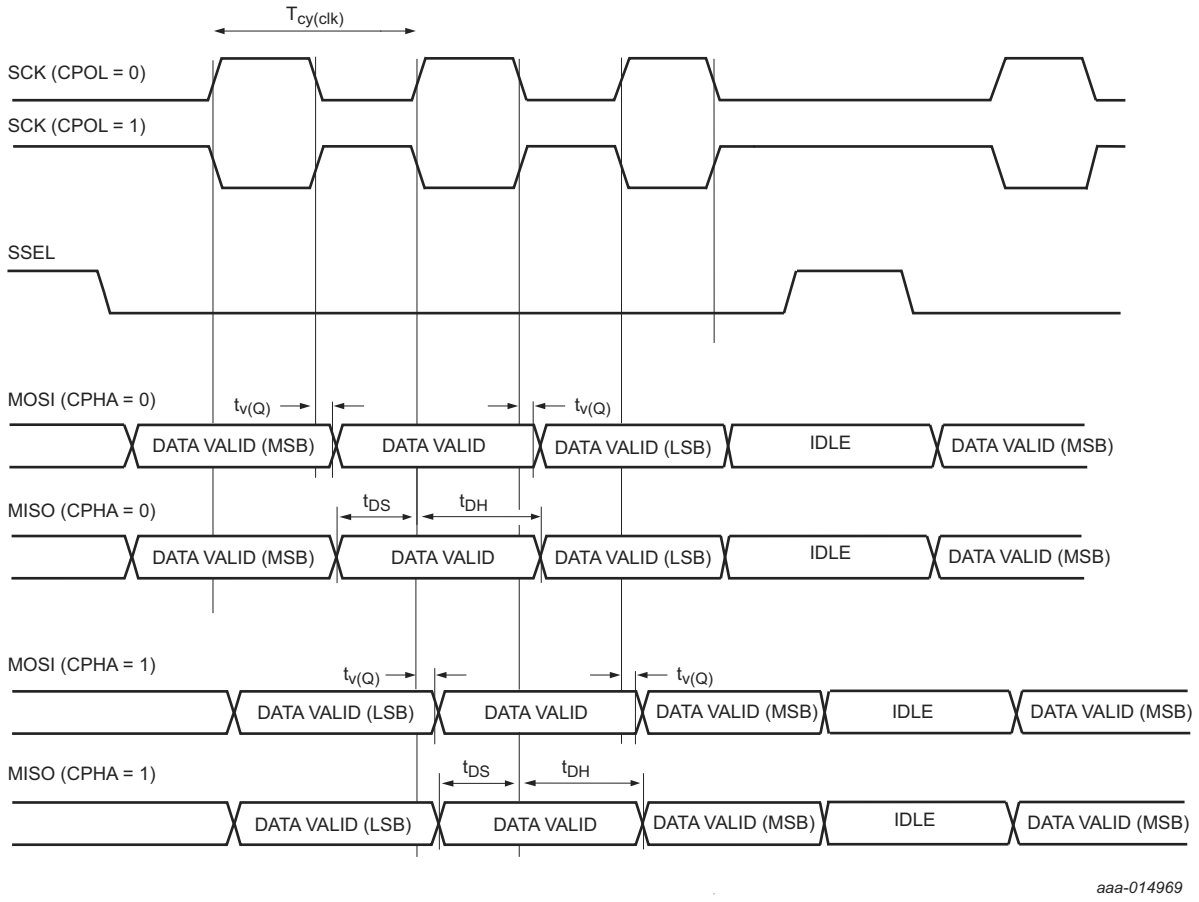


Fig 31. SPI master timing

11.19 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 47. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	21.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	19.7	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	0	-	4.9	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	4.5	ns
USART slave (in synchronous mode)1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.4	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	20.2	-	39.5	ns
		100 MHz < CCLK ≤ 180 MHz	19.3	-	37.7	ns
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		100 MHz < CCLK ≤ 180 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		100 MHz < CCLK ≤ 180 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

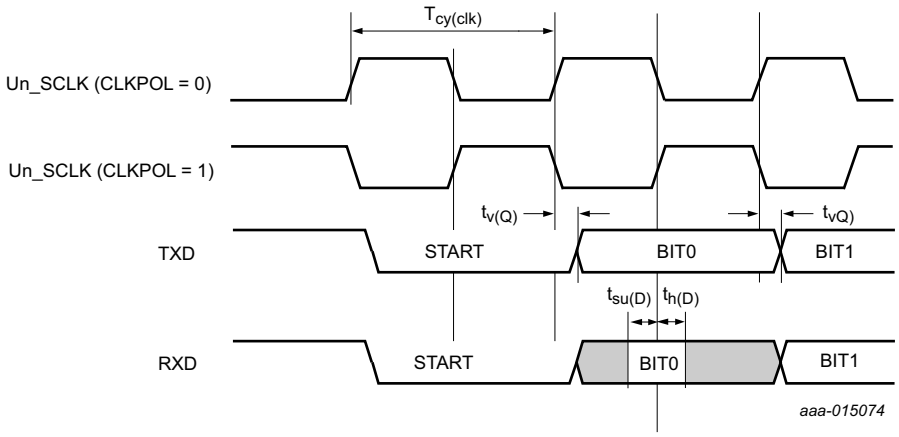


Fig 35. USART timing

11.20 SCTimer/PWM output timing

Table 48. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 90 % and 10 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	3.4	-	4.5	ns

11.21 USB interface characteristics

Table 49. Dynamic characteristics: USB0 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0		20	ns
t_f	fall time	10 % to 90 %		4.0		20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90		111.11	%
V_{CRS}	output signal crossover voltage			1.3		2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 36		160		175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 36		−2		+5	ns
t_{JR1}	receiver jitter to next transition			−18.5		+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 36	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 36	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 50. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Based on simulation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.2	-	0	ns
		100 MHz < CCLK ≤ 180 MHz		−1.2	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN, ENET_TX_ER	[1][2]				
		CCLK ≤ 100 MHz		10.0	-	18.2	ns
		100 MHz < CCLK ≤ 180 MHz		10.0	-	18.2	ns

[1] Output drivers can drive a load ≥ 25 pF accommodating over 12 inch of PCB trace and the input capacitance of the receiving device.

[2] Timing values are given from the point at which the clock signal waveform crosses 1.4 V to the valid input or output level.

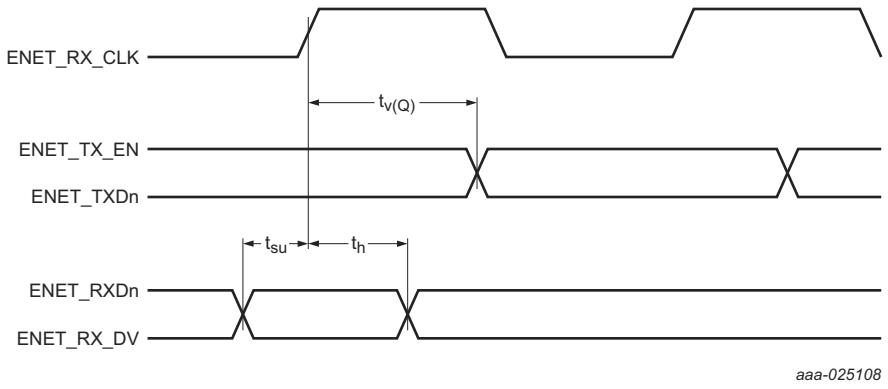


Fig 37. Ethernet RMII timing

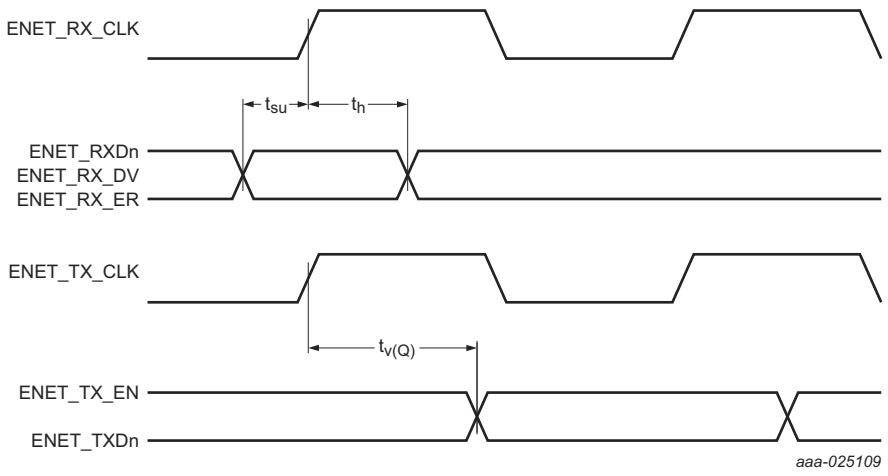


Fig 38. Ethernet MII timing

12.2 12-bit ADC characteristics

Table 54. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±4.5	-	LSB
			[1][5]	-		-	LSB
$E_{L(adj)}$	integral non-linearity	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±7.5	-	LSB
			[1][6]	-		-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz		-	< ±2.5	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

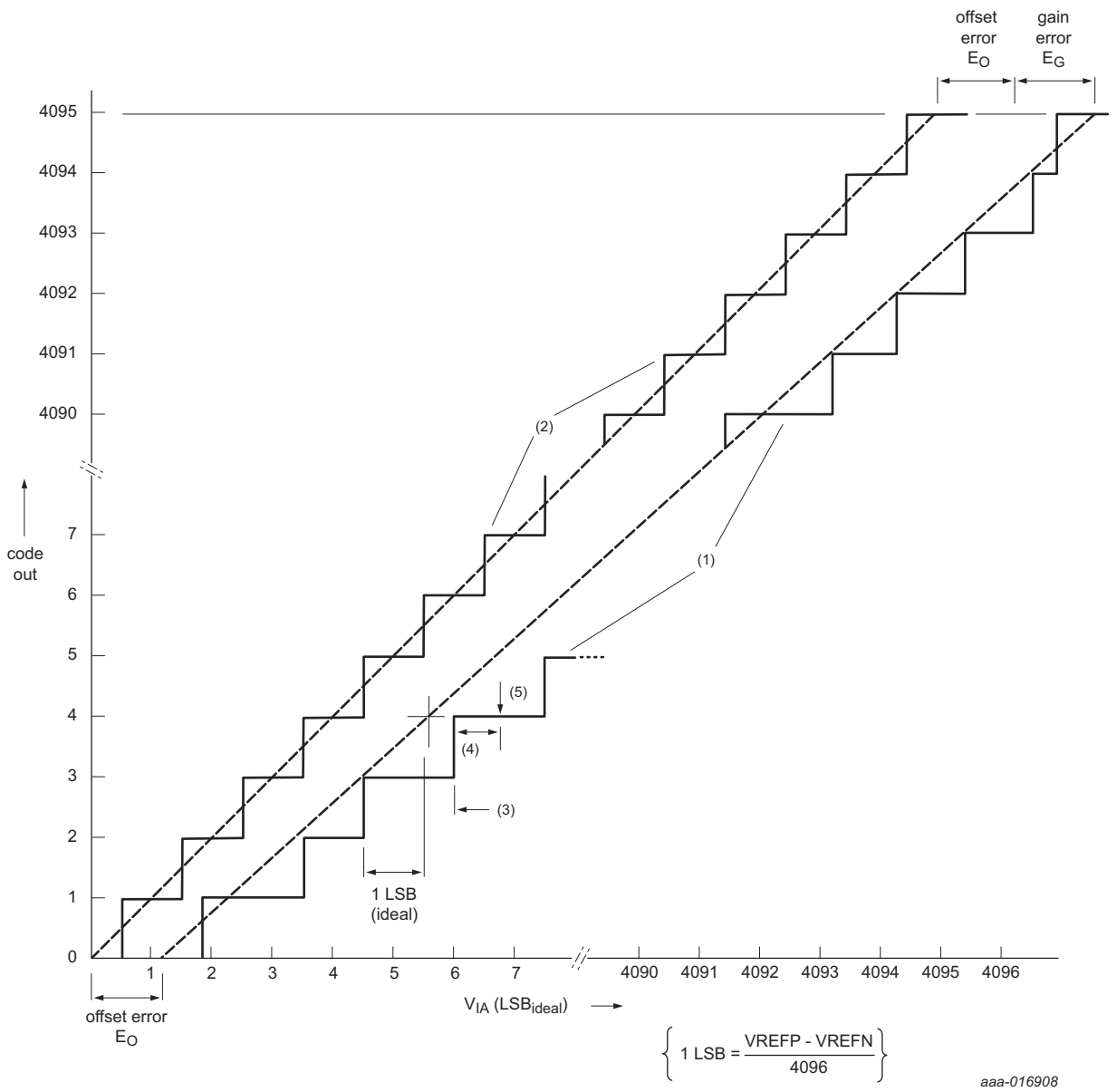
[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 40.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 21 for C_{io}. See Figure 41.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 40. 12-bit ADC characteristics

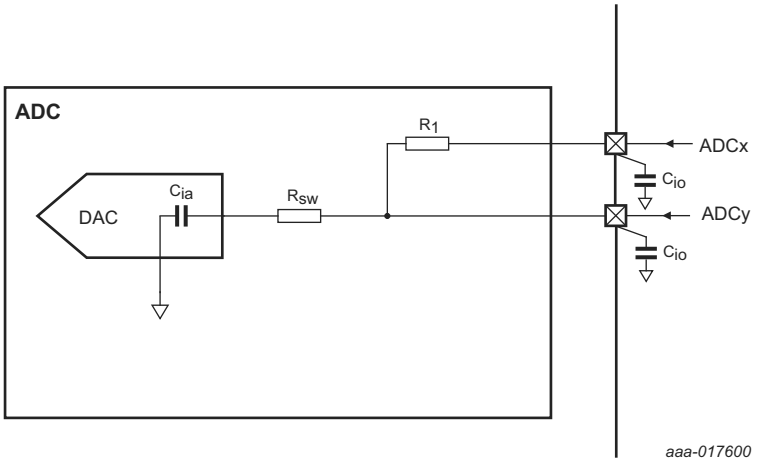


Fig 41. ADC input impedance

12.3 Temperature sensor

Table 56. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-		3.7	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	3.7	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

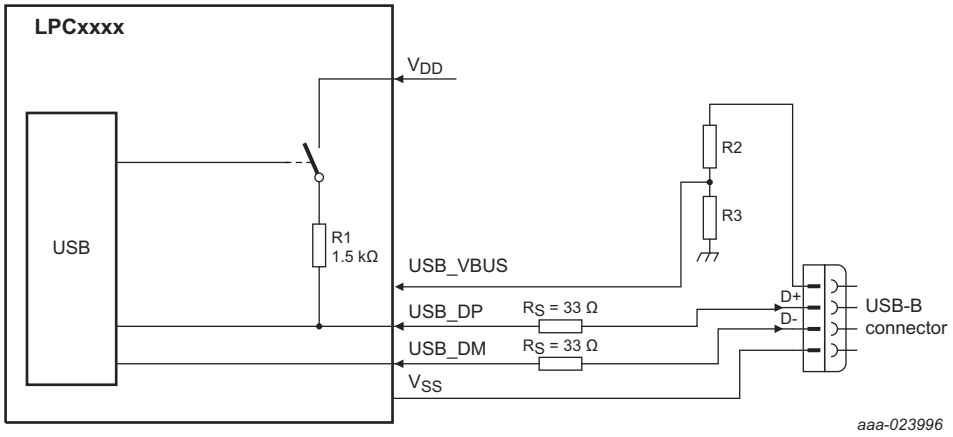
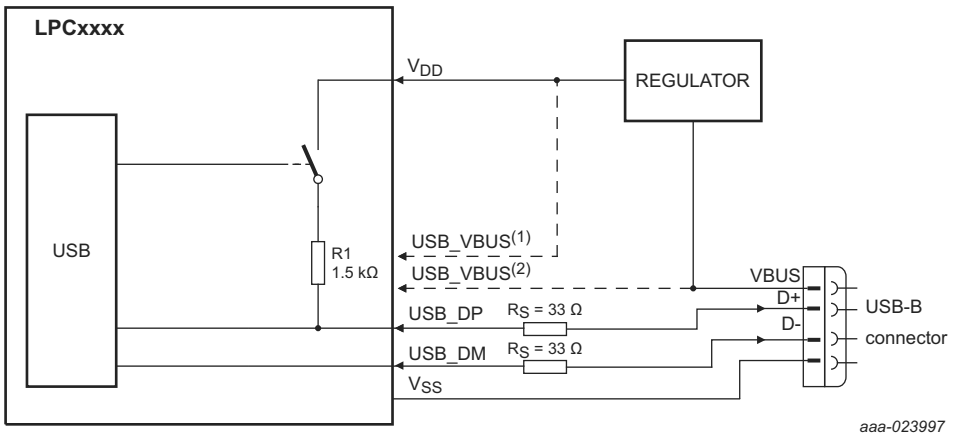


Fig 48. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



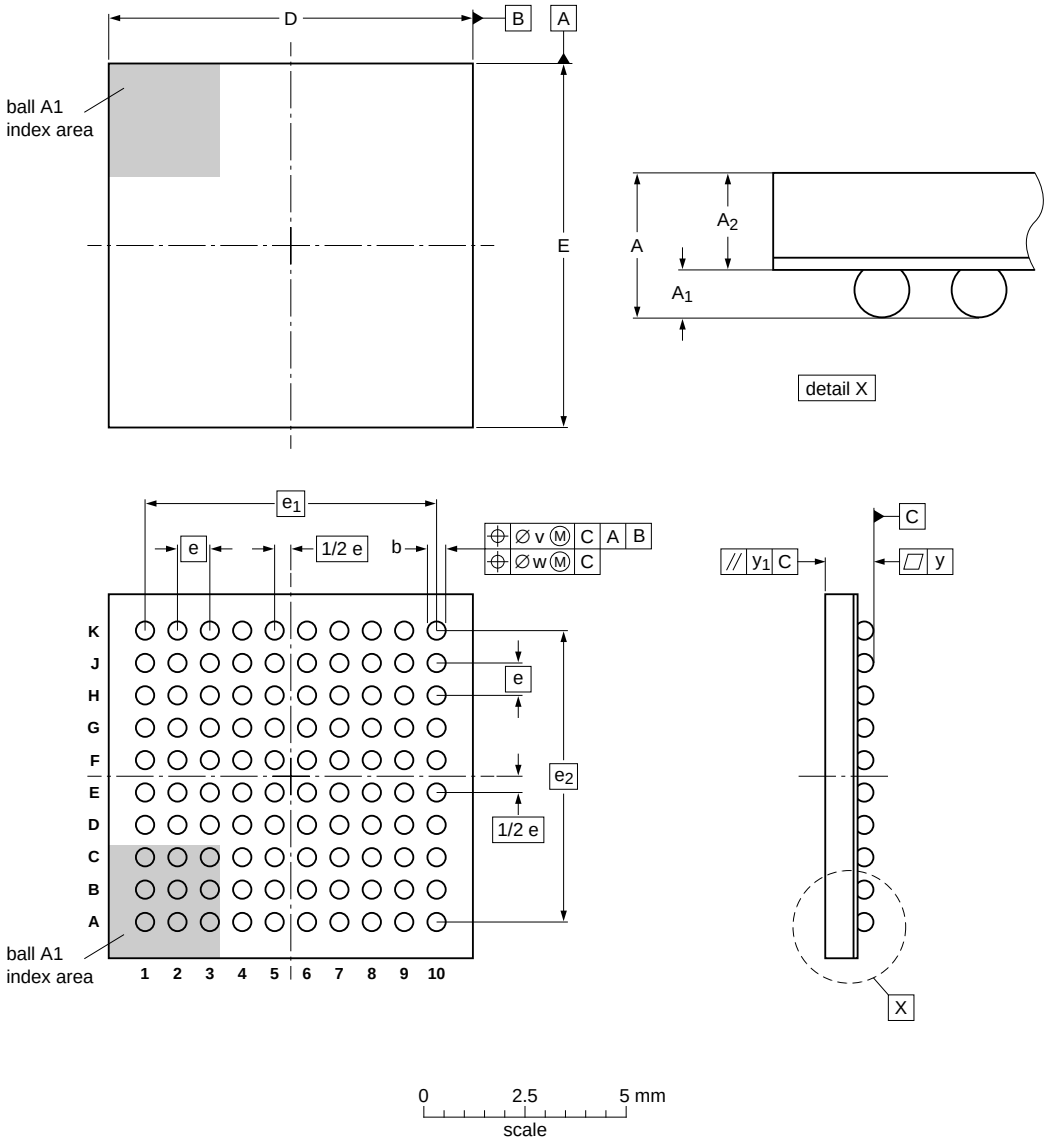
Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 49. USB interface on a bus-powered device

TFBGA100: plastic thin fine-pitch ball grid array package; 100 balls; body 9 x 9 x 0.7 mm **SOT926-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.8 0.65	0.5 0.4	9.1 8.9	9.1 8.9	0.8	7.2	7.2	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT926-1	- - -	- - -	- - -			~~05-12-09~~ 05-12-22

Fig 53. TFBGA100 package

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Regrouped Table 2 “Ordering options”. • Added text to Section 7.15.3.1 “Features”: Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details. • Removed Table note 2: fclk = cclk/CLKDIV +1. See LPC5460x UM10912 and updated Table note 1 “See the LPC5460x user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).”of Section 11.2 “EEPROM”. • Updated Table 50 “Dynamic characteristics: SD/MMC and SDIO”: changed the maximum clock frequency to 52 MHz. • Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”:			
LPC5460x v.1	20161215	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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