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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54605j512bd100e

- CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - SCTimer/PWM with 8 input and 10 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 10 match/captures, 10 events, and 10 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - enhanced Code Read Protection (eCRP) to protect user code.
  - OTP memory for ECRP settings, and user application specific data.
  - Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ± 1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_15/ ADC0_3	K2	L4	53	26	[4]	PU	I/O; AI	**PIO0_15/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_WEN —** External memory interface Write Enable (active low).
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
PIO0_16/ ADC0_4	H3	M4	54	27	[4]	PU	I/O; AI	**PIO0_16/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.ws
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CLKOUT —** Output of the CLKOUT function.
							I	**CT1_CAP0 —** Capture input 0 to Timer 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_CSN[0] —** External memory interface static chip select 0 (active low).
							O	**ENET_TXD0 —** Ethernet transmit data 0.
PIO0_17	B10	E14	146	70	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							O	**EMC_OEN —** External memory interface output enable (active low)
							O	**ENET_TXD1 —** Ethernet transmit data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_14	A9	C12	160	78	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B5	B7	187	88	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
								R — Reserved.
							O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	H8	N12	98	47	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_18	D2	D1	15	5	[2]	PU	I/O	**PIO1_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							I	**CAN1_RD —** Receiver input for CAN 1.
							O	**EMC_BLSN[1] —** External memory interface byte lane select 1 (active low).
PIO1_19	F3	L1	33	16	[2]	PU	I/O	**PIO1_19 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I/O	**EMC_D[8] —** External Memory interface data [8].
PIO1_20	G2	M1	35	17	[2]	PU	I/O	**PIO1_20 —** General-purpose digital input/output pin.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**CT3_CAP2 —** Capture 2 input to Timer 3.
								R — Reserved.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	K6	N8	74	37	[2]	PU	I/O	**PIO1_21 —** General-purpose digital input/output pin.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
								R — Reserved.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**EMC_D[10] —** External Memory interface data [10].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_19	-	P12	93	-	[2]	PU	I/O	**PIO2_19 —** General-purpose digital input/output pin.
							O	**LCD_VD[1] —** LCD Data [1].
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
PIO2_20	-	P13	95	-	[2]	PU	I/O	**PIO2_20 —** General-purpose digital input/output pin.
							O	**LCD_VD[2] —** LCD Data [2].
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
PIO2_21	-	L10	99	-	[2]	PU	I/O	**PIO2_21 —** General-purpose digital input/output pin.
							O	**LCD_VD[3] —** LCD Data [3].
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	-	K10	113	-	[2]	PU	I/O	**PIO2_22 —** General-purpose digital input/output pin.
							O	**LCD_VD[4] —** LCD Data [4].
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
								R — Reserved.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
PIO2_23	-	M14	115	-	[2]	PU	I/O	**PIO2_23 —** General-purpose digital input/output pin.
							O	**LCD_VD[5] —** LCD Data [5].
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
PIO2_24	-	K14	118	-	[2]	PU	I/O	**PIO2_24 —** General-purpose digital input/output pin.
							O	**LCD_VD[6] —** LCD Data [6].
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
PIO2_25	-	J11	121	-	[2][8]	PU	I/O	**PIO2_25 —** General-purpose digital input/output pin.
							O	**LCD_VD[7] —** LCD Data [7].
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

- Toggle on match.
- Do nothing on match.

- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins may vary by device.)

7.19.2 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

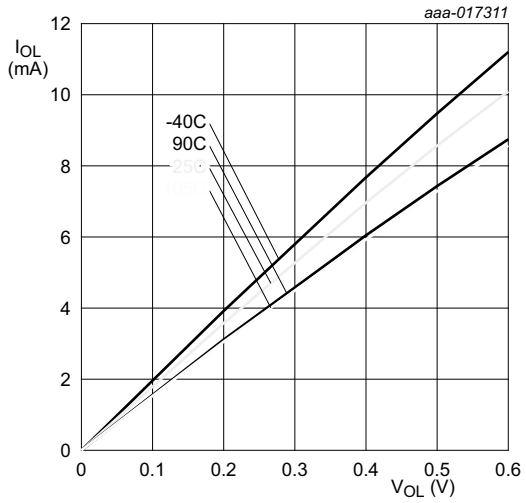
- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

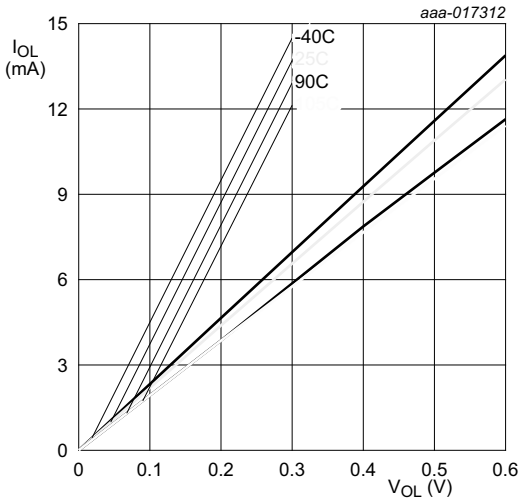
- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.19.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCTimer/PWM states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:

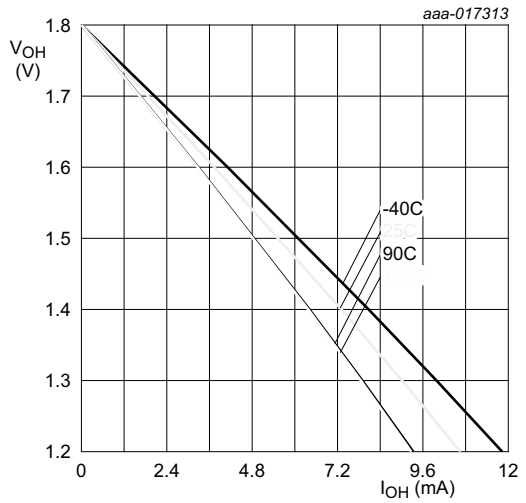


Conditions: V_{DD} = 1.8 V; on standard port pins.

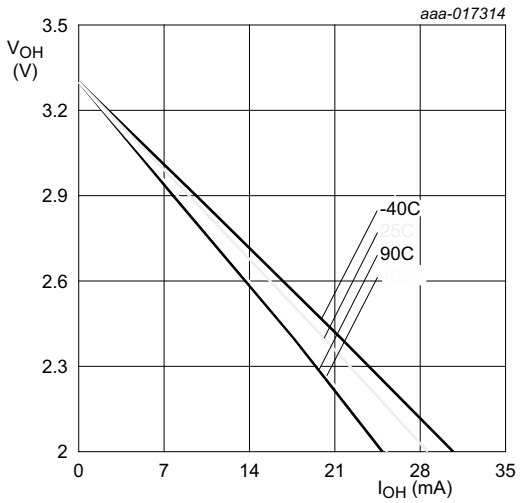


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 20. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 21. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

11.4 Wake-up process

Table 25. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.0	-	µs
		from deep-sleep mode; SRAMx powered. SRAM0, SRAM1, SRAM2, SRAM3, and USB SRAM powered down.	[2][5]	-	150	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

11.5 External memory interface

Table 26. Dynamic characteristics: Static external memory interface

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.4+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−1.6	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−6.7 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−4.8	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.8	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1.0	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.6	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.2	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	2.5	-	5.5	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6	-	2.9	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.6	-	0.9	ns

Table 26. Dynamic characteristics: Static external memory interface *…continued*

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1	[6]	−0.8	-	0	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[6]	0.6	-	0.9	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[2][6]	−0.8	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[2][6]	−1.2 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[2][6]	2.5 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	5.5 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[2][5][6]	−0.8 + $T_{cy(clk)}$	-	$T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[2][6]	0.2 + $T_{cy(clk)}$	-	0.5 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 24 as indicated in the Conditions column.

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM10912* LPC546xx *manual*).

[3] Latest of address valid, $\overline{EMC\_CSx}$ LOW, $\overline{EMC\_OE}$ LOW, $\overline{EMC\_BLSx}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_OE}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{EMC\_CSx}$ HIGH, $\overline{EMC\_BLSx}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM10912* LPC546xx *manual*).

Table 27. Dynamic characteristics: Static external memory interface

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.5+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−2.3	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−7.9 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns

Table 27. Dynamic characteristics: Static external memory interface *…continued*

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−5.5	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.7	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time	RD_8	[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters[2]							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.5 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.9	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	−0.1 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	3.1	-	6.7	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6 + $T_{cy(clk)}$	-	2.8 + $T_{cy(clk)}$	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.5 +$T_{cy(clk)}$	-	0.8 + $T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	PB = 1	[6]	−0.8	-	0	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	PB = 1	[6]	0.5	-	0.8	ns
t_{deact}	deactivation time	WR_8; PB = 0; PB = 1	[2][6]	−0.8	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW	WR_9; PB = 0	[2][6]	−1.9 + (WAITWEN + 1) × $T_{cy(clk)}$	-	(WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	WR_{10}; PB = 0	[2][6]	3.1+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	6.7+ (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSHEOW}$	$\overline{BLS}$ HIGH to end of write time	WR_{11}; PB = 0	[2][5][6]	−0.8 + $T_{cy(clk)}$	-	$T_{cy(clk)}$	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	WR12; PB = 0	[2][6]	0.2 + $T_{cy(clk)}$	-	0.5 + $T_{cy(clk)}$	ns

[1] Parameters are shown as RD_n or WD_n in Figure 24 as indicated in the Conditions column.

Table 28. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 3.7	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.7	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 4.1	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.8	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 4.4	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.9	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 5.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 4.8	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.7	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	8.1	ns
$t_{h(Q)}$	data output hold time		−1.7	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 30 for internal programmable delay.

11.18 Smart card interface

Table 46. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		100 MHz < CCLK ≤ 180 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

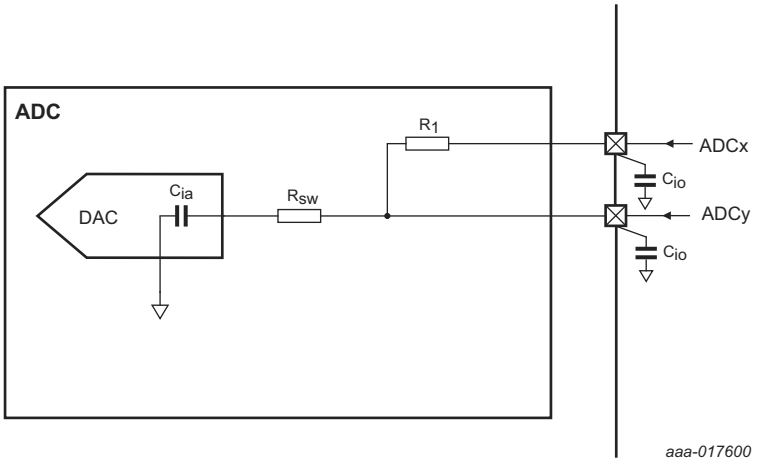


Fig 41. ADC input impedance

12.3 Temperature sensor

Table 56. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-		3.7	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	3.7	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.

13.3 Connecting power, clocks, and debug functions

Figure 45 shows the basic board connections used to power the LPC546xx. devices, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Updated a feature in Section 7.17.8.2 “SPI serial I/O controller”: Maximum data rate of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. Was 71 Mbit/s in master mode. • Updated Section 11.15 “SPI interfaces”: the maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s. • Updated Table 4 “Pin description”: Changed restate state of PIO3_23 and PIO0_24 to Z. Added footnote True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin to PIO3_23 and PIO0_24.			
LPC546xx v.1.9	20171109	Product data sheet	-	LPC546xx v.1.8
Modifications:	• Updated Table 1 “Ordering information” and Table 2 “Ordering options”. Added the part numbers: LPC54605J256BD100, LPC54605J512BD100, LPC54605J256ET100, LPC54605J512ET100.			
LPC546xx v.1.8	20170614	Product data sheet	-	LPC546xx v.1.7
Modifications:	• Updated Section 13.7 “Suggested USB interface solutions”. Removed the remark. • Added LPC5462x device to the data sheet. • Updated Timer and digital peripherals of Section 2 “Features and benefits”. • Updated Section 7.19.2 “SCTimer/PWM”, Section 7.19.2.1 “Features” and Section 7.18.3 “External memory controller”. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”. • Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”, Table 43 “SPI dynamic characteristics[1]”, Table 44 “Dynamic characteristics: SPIFI[1]”, Table 45 “Dynamic characteristics[1]”, Table 46 “Dynamic characteristics[1]”, Table 47 “USART dynamic characteristics[1]”, Table 50 “Dynamic characteristics: Ethernet”, Table 51 “Dynamic characteristics: SD/MMC and SDIO”, and Table 52 “Dynamic characteristics: LCD”: replaced the condition, CCLK > 100 MHz with 100 MHz <CCLK ≤ 180 MHz • Updated Table 12 “General operating conditions”. Added the condition, For OTP programming only to f_{clk}. • Added Remark to Section 7.24 “Code security (enhanced Code Read Protection - eCRP)”. • Updated Table 19 “Typical peripheral power consumption[1][2]”: added SYSOSC value. • Updated Table 14 “CoreMark score[1]”. • Updated Table 15 “Static characteristics: Power consumption in active and sleep mode”: I_{DD} supply current in Active mode: CoreMark code executed from flash. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”.			
LPC546xx v.1.7	20170428	Product data sheet	-	LPC546xx v.1.6
Modifications:	• Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”. • Updated Table 11 “Thermal resistance”.			
LPC546xx v.1.6		Product data sheet	-	LPC546xx v.1.5
Modifications:	• Added TFBGA100 and LQFP100 packages.			

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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