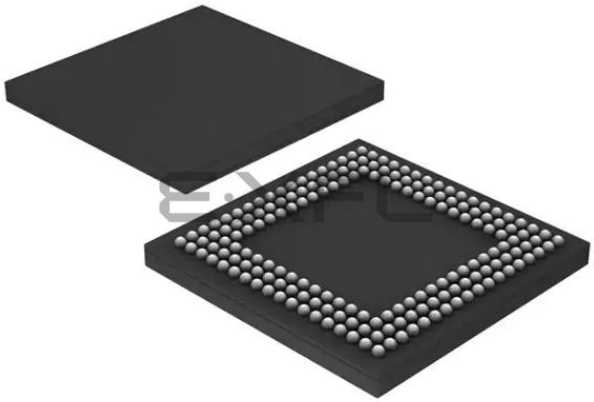

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	145
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54605j512et180e

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_30	A2	A2	200	95	[2]	PU	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.
PIO1_1	J10	K12	109	55	[2]	PU	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_18	D2	D1	15	5	[2]	PU	I/O	**PIO1_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							I	**CAN1_RD —** Receiver input for CAN 1.
							O	**EMC_BLSN[1] —** External memory interface byte lane select 1 (active low).
PIO1_19	F3	L1	33	16	[2]	PU	I/O	**PIO1_19 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I/O	**EMC_D[8] —** External Memory interface data [8].
PIO1_20	G2	M1	35	17	[2]	PU	I/O	**PIO1_20 —** General-purpose digital input/output pin.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**CT3_CAP2 —** Capture 2 input to Timer 3.
								R — Reserved.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	K6	N8	74	37	[2]	PU	I/O	**PIO1_21 —** General-purpose digital input/output pin.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
								R — Reserved.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**EMC_D[10] —** External Memory interface data [10].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_8	-	F4	32	-	[2]	PU	I/O	**PIO2_8 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[2] —** SD/MMC data 2.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
PIO2_9	-	K2	36	-	[2]	PU	I/O	**PIO2_9 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[3] —** SD/MMC data 3.
								R — Reserved.
							O	**CT0_MAT1 —** Match output 0 from Timer 1.
PIO2_10	-	P1	39	-	[2]	PU	I/O	**PIO2_10 —** General-purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
PIO2_11	-	K3	43	-	[2]	PU	I/O	**PIO2_11 —** General-purpose digital input/output pin.
							O	**LCD_PWR —** LCD panel power enable.
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
								R — Reserved.
								R — Reserved.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
PIO2_12	-	M2	45	-	[2]	PU	I/O	**PIO2_12 —** General-purpose digital input/output pin.
							O	**LCD_LE —** LCD line end signal.
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
								R — Reserved.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_13	-	P7	70	-	[2]	PU	I/O	**PIO2_13 —** General-purpose digital input/output pin.
							O	**LCD_DCLK —** LCD panel clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
								R — Reserved.
								R — Reserved.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_19	-	J3	44	-	[2]	PU	I/O	**PIO3_19 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I	**CAN0_RD —** Receiver input for CAN 0.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
PIO3_20	-	N2	46	-	[2]	PU	I/O	**PIO3_20 —** General-purpose digital input/output pin.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I	**SD_CARD_INT_N —** Card interrupt line.
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
PIO3_21/ ADC0_9	-	P5	61	-	[4]	PU	I/O; AI	**PIO3_21/ADC0_9 —** General-purpose digital input/output pin. ADC input channel 9 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
PIO3_22/ ADC0_10	-	N5	62	-	[4]	PU	I/O; AI	**PIO3_22/ADC0_10 —** General-purpose digital input/output pin. ADC input channel 10 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_23	-	C2	8	-	[3]	Z	I/O	**PIO3_23 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
PIO3_24	-	E2	16	-	[3]	Z	I/O	**PIO3_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_31	-	-	114	-	[2]	PU	I/O	**PIO4_31 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
							I/O	**EMC_D[26] —** External Memory interface data [26].
PIO5_0	-	-	122	-	[2]	PU	I/O	**PIO5_0 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I/O	**EMC_D[27] —** External Memory interface data [27].
PIO5_1	-	-	126	-	[2]	PU	I/O	**PIO5_1 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**EMC_D[28] —** External Memory interface data [28].
PIO5_2	-	-	202	-	[2]	PU	I/O	**PIO5_2 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I/O	**EMC_D[29] —** External Memory interface data [29].

7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- Supports up to 54 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M4 core clock.

7.7 On-chip static RAM

The LPC546xx support 200 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.8 On-chip flash

The LPC546xx supports up to 512 kB of on-chip flash memory.

7.9 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- Flash In-Application Programming (IAP) and In-System Programming (ISP).
- ROM-based USB drivers (HID, CDC, MSC, and DFU). Supports flash updates via USB.
- Supports booting from valid user code in flash, USART, SPI, and I2C.
- Legacy, Single, and Dual image boot.
- OTP API for programming OTP memory.
- Random Number Generator (RNG) API.

7.12.1.3 Crystal oscillator

The LPC546xx include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC546xx will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 11 and Figure 12 for an overview of the LPC546xx clock generation.

7.12.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

GPIO Pin Interrupts, GPIO Group Interrupts, and selected peripherals such as USB0, USB1, DMIC, SPI, I2C, USART, WWDT, RTC, Micro-tick Timer, and BOD can be left running in deep sleep mode The FRO, RTC oscillator, and the watchdog oscillator can be left running.In some cases, DMA can operate in deep-sleep mode. For more details, see UM10912, LPC546xx. user manual.

7.14.3 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the RESET pin. The LPC546xx can wake up from deep power-down mode via the RESET pin and the RTC alarm. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
Flash	Software configured	Standby	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations. For more details, see UM10912, LPC546xx. user manual.	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB0	Software configured	Software configured	Off
USB1	Software configured	Software configured	Off
Ethernet	Software configured	Off	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

7.17.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.17.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC546xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

7.19.6 Repetitive Interrupt Timer (RIT)

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.19.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Can be used for ETM debug time stamping.

7.20 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

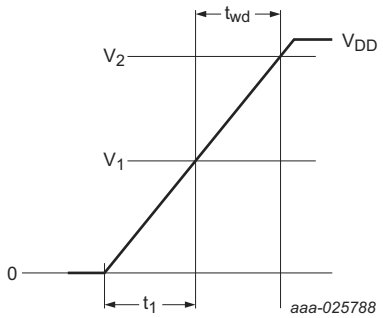
The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.20.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

[3] V_{DD} to stay below V_2 for the minimum duration of t_{wd}.



t_1: The time when there is no restriction on the ramp rate.

Fig 13. Power-up ramp

10.3 CoreMark data

Table 14. CoreMark score[1]

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[2][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 96 MHz	[2][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 180 MHz	[3][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 220 MHz	[3][4][5][7][8]	3.38	Iterations/s/MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][5][6][8]	3.38	Iterations/s/MHz
	CCLK = 96 MHz; 5 system clock flash access time.	[2][4][5][6][8]	2.59	Iterations/s/MHz
	CCLK = 180 MHz; 9 system clock flash access time.	[3][4][5][6][8]	1.99	Iterations/s/MHz
	CCLK = 220 MHz; 8 system clock flash access time.	[3][4][5][6][8][9]	2.11	Iterations/s/MHz
	CCLK = 220 MHz; 9 system clock flash access time.	[3][4][5][6][8]	1.99	Iterations/s/MHz

[1] Based on the power API library from the SDK software package available on nxp.com.

[2] Clock source FRO. PLL disabled.

[3] Clock source 12 MHz FRO. PLL enabled.

[4] Characterized through bench measurements using typical samples.

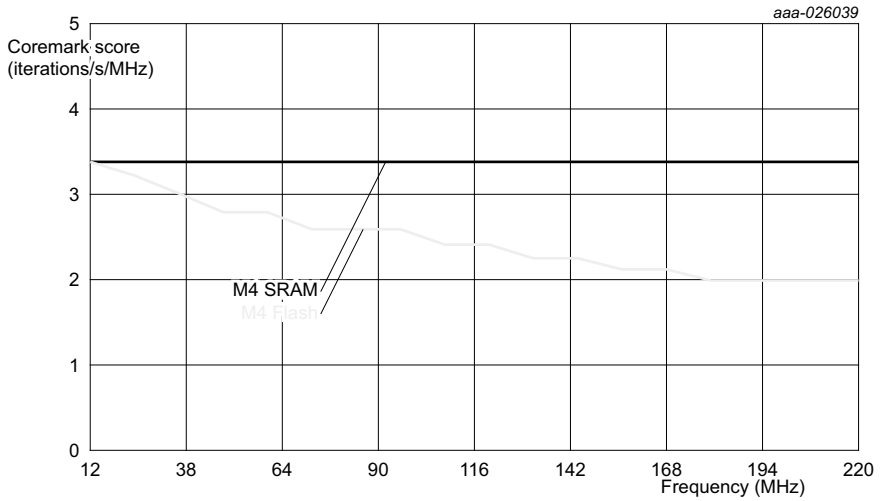
[5] Compiler settings: IAR C/C++ Compiler for Arm ver 8.22.2, optimization level 3, optimized for time on.

[6] See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASHCFG register is set to 1.

[7] Flash is powered down

[8] SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.

[9] At 220 MHz the minimum system clock/access time can be lower when compared to 180 MHz because the power library optimizes the on-chip voltage regulator.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASCFG register is set to 1. Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON. Coremark score is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark score from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark score from SRAMX: SRAM0 is powered; flash is powered down.

Fig 14. Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Async APB peripheral		**CPU: 12 MHz, Async APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 12 MHz[2]**	**CPU: 96 MHz, Async APB bus: 12 MHz[2]**	**CPU: 180 MHz, Async APB bus: 12 MHz[2]**	**CPU: 220 MHz, Async APB bus: 12 MHz[2]**
Timer3		0.9	0.9	0.9	0.9	1.2
Timer4		0.9	0.9	0.9	0.9	1.2

[1] Turn off the peripheral when the configuration is done.

[2] For optimal system power consumption, use fixed low frequency Async APB bus when the CPU is at a higher frequency.

[3] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1, and PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[4] The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz, 180 MHz, and 220 MHz.

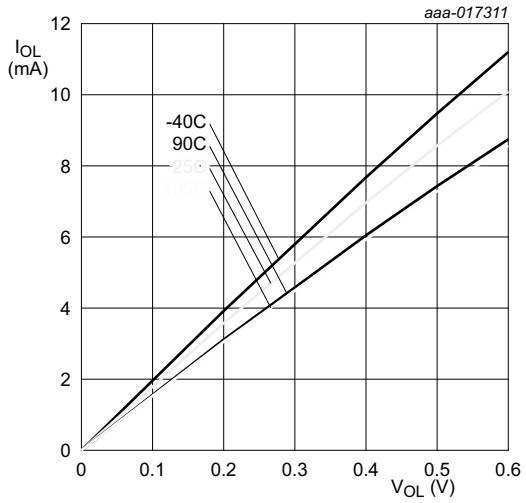
[5] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

10.5 Pin characteristics

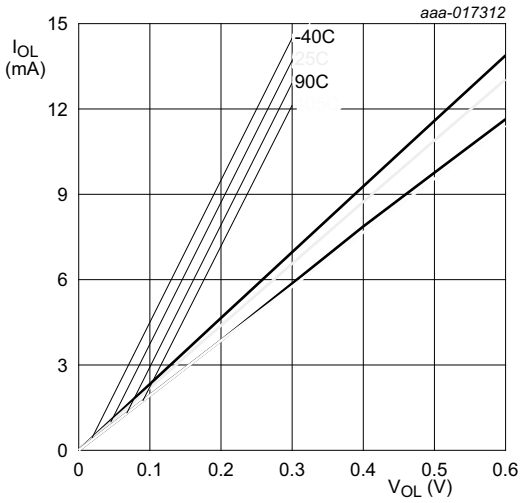
Table 21. Static characteristics: pin characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
RESET pin							
V_{IH}	HIGH-level input voltage			0.8 × V_{DD}	-	5.0	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage		[14]	0.05 × V_{DD}	-	-	V
Standard I/O pins							
Input characteristics							
I_{IL}	LOW-level input current	V_I = 0 V; on-chip pull-up resistor disabled.		-	3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; V_{DD} = 3.6 V; for RESETN pin.			3.0	180	nA
I_{IH}	HIGH-level input current	V_I = V_{DD}; on-chip pull-down resistor disabled		-	3.0	180	nA
V_I	input voltage	pin configured to provide a digital function; V_{DD} > 1.8 V	[3]	0	-	5.0	V
		V_{DD} = 0 V		0	-	3.6	V
V_{IH}	HIGH-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		1.5	-	5.0	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		2.0	-	5.0	V
V_{IL}	LOW-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		−0.5	-	+0.4	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		−0.5	-	+0.8	V
V_{hys}	hysteresis voltage		[14]	0.1 × V_{DD}	-	-	V
Output characteristics							

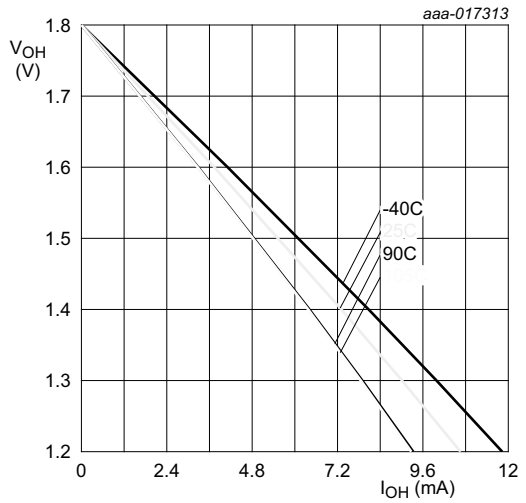


Conditions: V_{DD} = 1.8 V; on standard port pins.

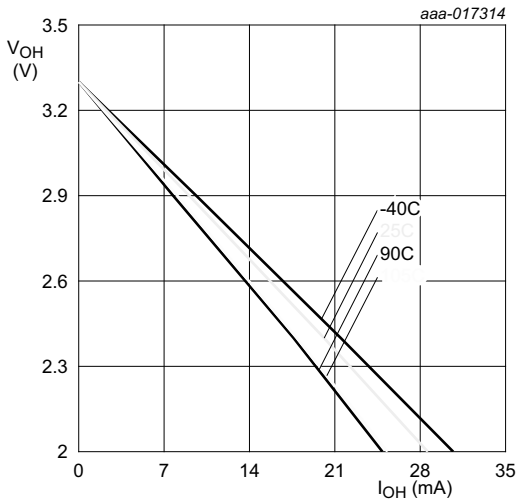


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 20. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 21. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

11.5 External memory interface

Table 26. Dynamic characteristics: Static external memory interface

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.4+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−1.6	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−6.7 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−4.8	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.8	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1.0	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.6	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.2	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	2.5	-	5.5	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6	-	2.9	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.6	-	0.9	ns

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM10912* LPC546xx *manual*).

[3] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM10912* LPC546xx *manual*).

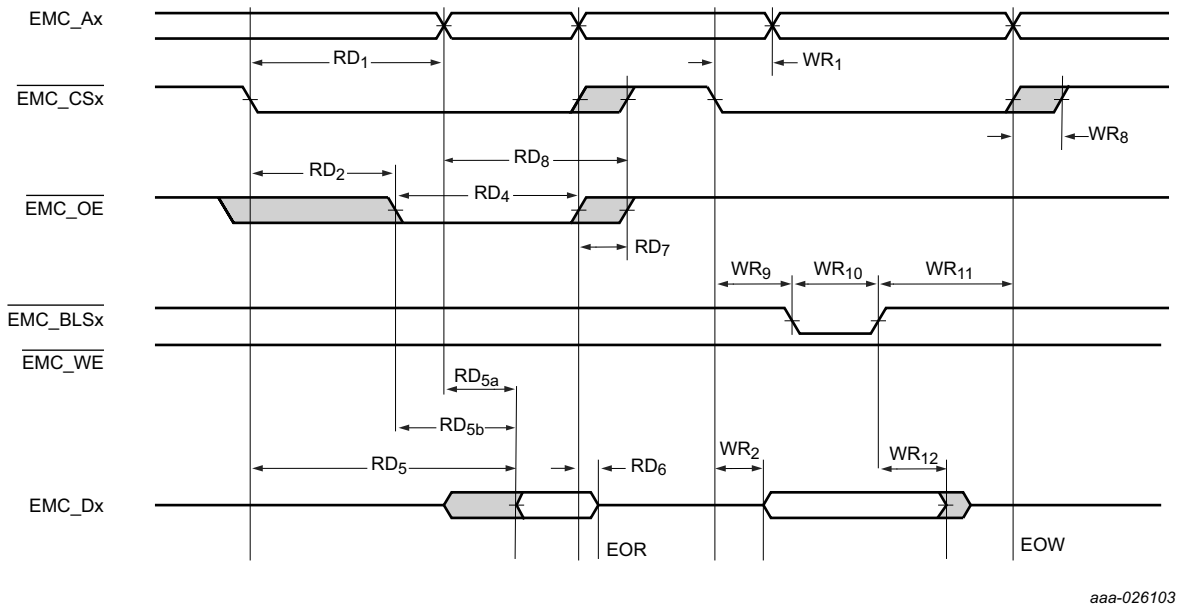


Fig 24. External static memory read/write access (PB = 0)

11.12 Watchdog oscillator

Table 40. Dynamic characteristics: Watchdog oscillator

T_{amb} = −40 °C to +105 °C; 1.71 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency		[2]	200	-	1500	kHz
D_{clkout}	clkout duty cycle			48	-	52	%
J_{PP-CC}	peak-peak period jitter		[3][4]	-	1	20	ns
t_{start}	start-up time		[4]	-	4	-	μs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

11.19 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 47. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	21.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	19.7	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	0	-	4.9	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	4.5	ns
USART slave (in synchronous mode)1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.4	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	20.2	-	39.5	ns
		100 MHz < CCLK ≤ 180 MHz	19.3	-	37.7	ns
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		100 MHz < CCLK ≤ 180 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		100 MHz < CCLK ≤ 180 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

13.3 Connecting power, clocks, and debug functions

Figure 45 shows the basic board connections used to power the LPC546xx. devices, connect the external crystal and the 32 kHz oscillator for the RTC, and provide debug capabilities via the serial wire port.

21. Contents

continued >>