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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j256bd100e

- On-chip memory:
  - Up to 512 KB on-chip flash program memory with flash accelerator and 256 byte page erase and write.
  - Up to 200 KB total SRAM consisting of 160 KB contiguous main SRAM and an additional 32 KB SRAM on the I&D buses. 8 KB of SRAM bank intended for USB traffic.
  - 16 KB of EEPROM.
- ROM API support:
  - Flash In-Application Programming (IAP) and In-System Programming (ISP).
  - ROM-based USB drivers (HID, CDC, MSC, and DFU). Flash updates via USB.
  - Booting from valid user code in flash, USART, SPI, and I^2C.
  - Legacy, Single, and Dual image boot.
  - OTP API for programming OTP memory.
  - Random Number Generator (RNG) API.
- Serial interfaces:
  - Flexcomm Interface contains up to ten serial peripherals. Each Flexcomm Interface can be selected by software to be a USART, SPI, or I^2C interface. Two Flexcomm Interfaces also include an I^2S interface. Each Flexcomm Interface includes a FIFO that supports USART, SPI, and I^2S if supported by that Flexcomm Interface. A variety of clocking options are available to each Flexcomm Interface and include a shared fractional baud-rate generator.
  - I^2C-bus interfaces support Fast-mode and Fast-mode Plus with data rates of up to 1Mbit/s and with multiple address recognition and monitor mode. Two sets of true I^2C pads also support High Speed Mode (3.4 Mbit/s) as a slave.
  - Two ISO 7816 Smart Card Interfaces with DMA support.
  - USB 2.0 high-speed host/device controller with on-chip high-speed PHY.
  - USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00032 for more details.
  - SPIFI with XIP feature uses up to four data lines to access off-chip SPI/DSPI/QSPI flash memory at a much higher rate than standard SPI or SSP interfaces.
  - Ethernet MAC with MII/RMII interface with Audio Video Bridging (AVB) support and dedicated DMA controller.
  - Two CAN FD modules with dedicated DMA controller.
- Digital peripherals:
  - DMA controller with 30 channels and up to 24 programmable triggers, able to access all memories and DMA-capable peripherals.
  - LCD Controller supporting both Super-Twisted Nematic (STN) and Thin-Film Transistor (TFT) displays. It has a dedicated DMA controller, selectable display resolution (up to 1024 x 768 pixels), and supports up to 24-bit true-color mode.
  - External Memory Controller (EMC) provides support for asynchronous static memory devices such as RAM, ROM and flash, in addition to dynamic memories such as single data rate SDRAM with an SDRAM clock of up to 100 MHz. EMC bus width (bit) on TFBGA180, TFBGA100, and LQFP100 and packages supports up to 8/16 data line wide static memory, in addition to dynamic memories, such as, SDRAM (2 banks only) with an SDRAM clock of up to 100 MHz.
  - Secured digital input/output (SD/MMC and SDIO) card interface with DMA support.

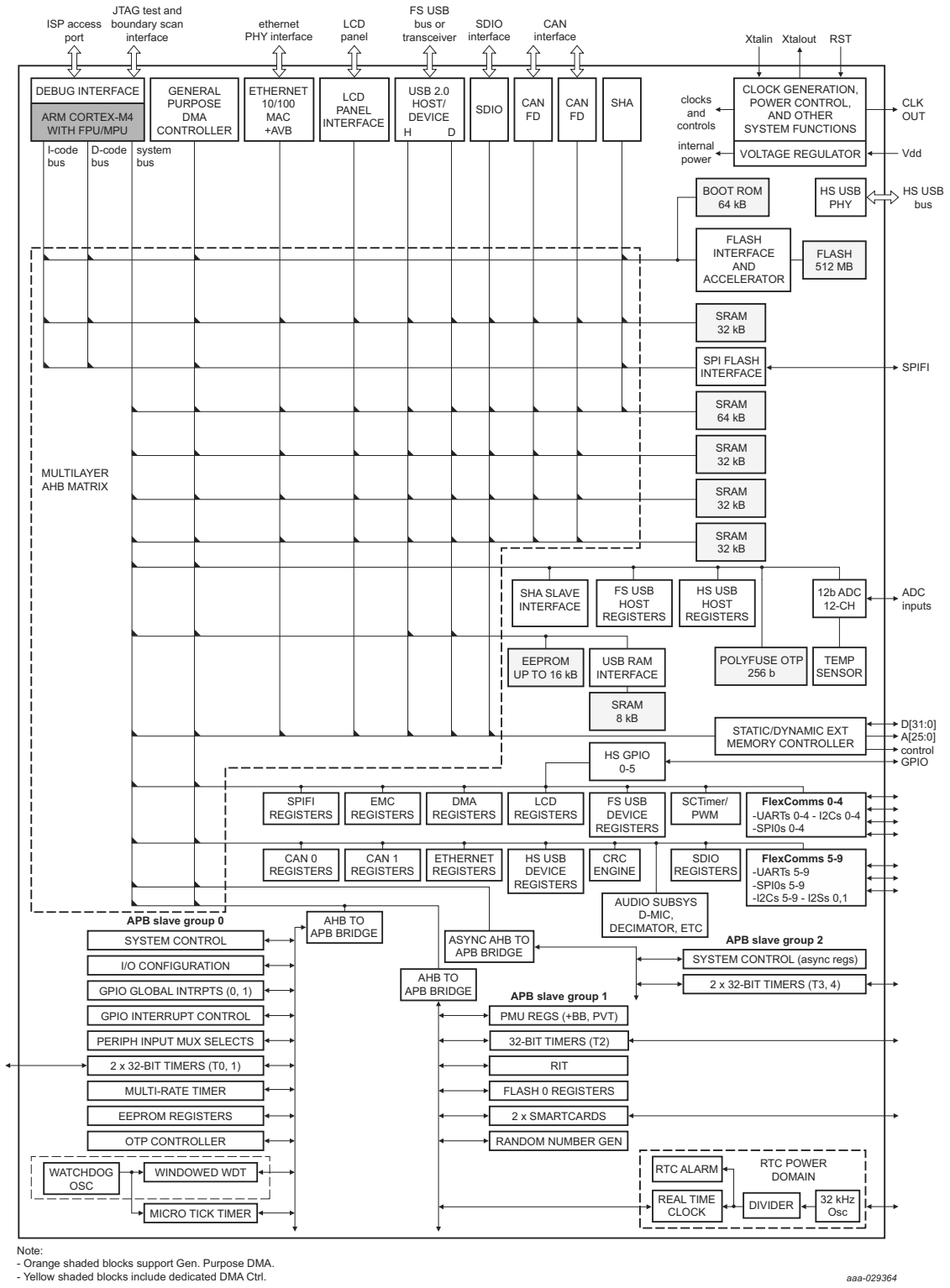

Fig 4. LPC546xx Block diagram

6.2 Pin description

On the LPC546xx, digital pins are grouped into several ports. Each digital pin can support several different digital functions (including General Purpose I/O (GPIO)) and an additional analog function.

Table 4. Pin description

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_0	C4	D6	196	93	[2]	PU	I/O	**PIO0_0 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SCK function.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							O	**CTimer_MAT0 —** Match output 0 from Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
PIO0_1	A1	A1	207	100	[2]	PU	I/O	**PIO0_1 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI SSEL0 function.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
PIO0_2/ TRST	A7	E9	174	83	[2]	PU	I/O	**PIO0_2 —** General-purpose digital input/output pin. In boundary scan mode: TRST (Test Reset). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MISO function.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**SCT0_GPI[2] —** Pin input 2 to SCTimer/PWM.
							I/O	**EMC_D[0] —** External Memory interface data [0].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_25	-	P9	82	-	[2]	PU	I/O	**PIO3_25 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[14] —** External memory interface address 14.
PIO3_26	-	K5	88	-	[2]	PU	I/O	**PIO3_26 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[15] —** External memory interface address 15.
PIO3_27	-	P14	96	-	[2]	PU	I/O	**PIO3_27 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[16] —** External memory interface address 16.
PIO3_28	-	M11	100	-	[2]	PU	I/O	**PIO3_28 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[17] —** External memory interface address 17.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_1	-	G14	132	-	[2]	PU	I/O	**PIO4_1 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	-	F14	138	-	[2]	PU	I/O	**PIO4_2 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	-	F13	140	-	[2]	PU	I/O	**PIO4_3 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	-	D9	147	-	[2]	PU	I/O	**PIO4_4 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_19	-	-	14	-	[2]	PU	I/O	**PIO4_19 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.
								R — Reserved.
							O	**EMC_DQM[2] —** External memory interface data mask 2.
PIO4_20	-	-	18	-	[2]	PU	I/O	**PIO4_20 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I	**CT4_CAP3 —** Capture input 3 to Timer 4.
								R — Reserved.
							O	**EMC_DQM[3] —** External memory interface data mask 3.
PIO4_21	-	-	34	-	[2]	PU	I/O	**PIO4_21 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
								R — Reserved.
							I/O	**EMC_D[16] —** External Memory interface data [16].
PIO4_22	-	-	47	-	[2]	PU	I/O	**PIO4_22 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
								R — Reserved.
							I/O	**EMC_D[17] —** External Memory interface data [17].

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

7.18.4 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.18.4.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.19 Counter/timers

7.19.1 General-purpose 32-bit timers/external event counter

The LPC546xx includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
  - Set LOW on match.
  - Set HIGH on match.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

[13] 8-layer (4.5 in × 3 in); still air.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP208 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	33 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		16 ± 15 %	°C/W
LQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	48 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	65 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		19 ± 15 %	°C/W
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W
TFBGA100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	69 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	60 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		10 ± 15 %	°C/W

10. Static characteristics

10.1 General operating conditions

Table 12. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	CPU clock frequency		[3]	-	-	220	MHz
	CPU clock frequency	For USB high-speed device and host operations	[3]	60	-	220	MHz
	CPU clock frequency	For USB full-speed device and host operations	[3]	12	-	220	MHz
		For OTP programming only		-	-	12	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For OTP programming only	[2]	2.7	-	3.6	V
		For USB operation only		3.0	-	3.6	V
V_{DDA}	analog supply voltage			1.71	-	3.6	V
V_{BAT}	battery supply voltage			1.71	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
T_{amb}	Temperature	For EEPROM operation		−40.0	-	+85	°C
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		-0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		-0.5	-	+3.6	V
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	-	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	-	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Attempting to program below 2.7 V will result in unpredictable results and the part might enter an unrecoverable state.

[3] The LPC5460x/61x operates at CPU frequencies of up to 180 MHz. The LPC54628 operates at CPU frequencies of up to 220 MHz.

10.2 Power-up ramp conditions

Table 13. Power-up characteristics[1]

T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1 < V_{DD} < V_2$)		-	-	170	µs
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.62	V

[1] Assert the external reset pin until V_{DD} is > 1.62 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180MHz.

Table 19. Typical peripheral power consumption[1][2]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO	100
WDT OSC	2.0
Flash	200
BOD	2.0
SYSOSC	247

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
USB0 device		0.3	0.3	0.3	0.4	0.5
USB1 device		4.4	4.4	4.4	5.0	6.5
DMIC		0.2	0.2	0.2	0.2	0.3
GPIO0	[1]	0.9	0.9	0.9	1.0	1.4
GPIO1	[1]	0.8	0.8	0.8	1.0	1.4
GPIO2	[1]	1.0	1.0	1.0	1.1	1.4
GPIO3	[1]	1.1	1.1	1.1	1.3	1.7
GPIO4	[1]	1.0	1.0	1.0	1.2	1.6
GPIO5	[1]	0.7	0.7	0.7	0.8	1.1
DMA		0.7	0.7	0.7	0.8	1.1
CRC		1.0	1.0	1.0	1.0	1.4
ADC0		1.6	1.6	1.6	1.9	2.6
SCTimer/PWM		4.5	4.5	4.5	5.3	7.0
Ethernet AVB		24.0	24.0	24.0	28.0	38.0
LCD		13.0	13.0	13.0	15.0	19.0
EEPROM		1.1	1.1	1.1	1.2	1.6
EMC		39.0	39.0	39.0	45.4	60.1
CAN0		10.8	10.8	10.8	12.6	16.5
CAN1		10.7	10.7	10.7	12.4	16.4
SD/MMC		7.9	7.9	7.9	9.3	12.3
Flexcomm Interface 0 (USART, SPI, I^2C)		1.6	1.6	1.6	1.9	2.5

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Flexcomm Interface1 (USART, SPI, I^2C)		1.6	1.6	1.6	1.8	2.4
Flexcomm Interface 2 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.6
Flexcomm Interface 3 (USART, SPI, I^2C)		1.4	1.4	1.4	1.6	2.2
Flexcomm Interface 4 (USART, SPI, I^2C)		1.4	1.5	1.5	1.7	2.3
Flexcomm Interface 5 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.5
Flexcomm Interface 6 (USART, SPI, I^2C, I^2S)		2.0	2.0	2.0	2.3	3.0
Flexcomm Interface 7 (USART, SPI, I^2C, I^2S)		1.6	1.6	1.6	1.9	2.5
Flexcomm Interface 8 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Flexcomm Interface 9 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
INPUTMUX	[1]	0.83	0.85	0.86	1.0	1.3
IOCON	[1]	2.67	2.65	2.65	3.13	4.2
PINT		1.1	1.1	1.1	1.3	1.8
GINT0 and GINT1		1.33	1.35	1.34	1.52	2.0
WWDT		0.42	0.42	0.42	0.46	0.6
RTC		0.3	0.3	0.3	0.3	0.4
MRT		0.3	0.3	0.3	0.3	0.4
RIT		0.1	0.1	0.1	0.1	0.1
UTICK		0.2	0.2	0.2	0.2	0.3
CTimer0		0.8	0.8	0.8	0.9	1.3
CTimer1		0.8	0.9	0.9	1.0	1.4
CTimer2		0.83	0.85	0.88	0.99	1.3
Smart card0		2.5	2.5	2.5	2.8	3.7
Smart card1		2.5	2.5	2.5	2.8	3.7
RNG		1.4	1.4	1.4	1.5	2.0
OTP controller		4.0	4.0	4.0	4.5	6.0
SHA		1.2	1.2	1.2	1.3	1.7

Table 21. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.71 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.71 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.71 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.71 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.71 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA
I_{OLS}	LOW-level short-circuit output current	1.71 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	µA
		V_I = 5 V	[2]	80		100	µA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	µA
		V_{DD} < V_I < 5 V	[2][7]	6		30	µA
Open-drain I^2C pins							
V_{IH}	HIGH-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	µA
		V_I = 5 V		-	5.5	10	µA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA

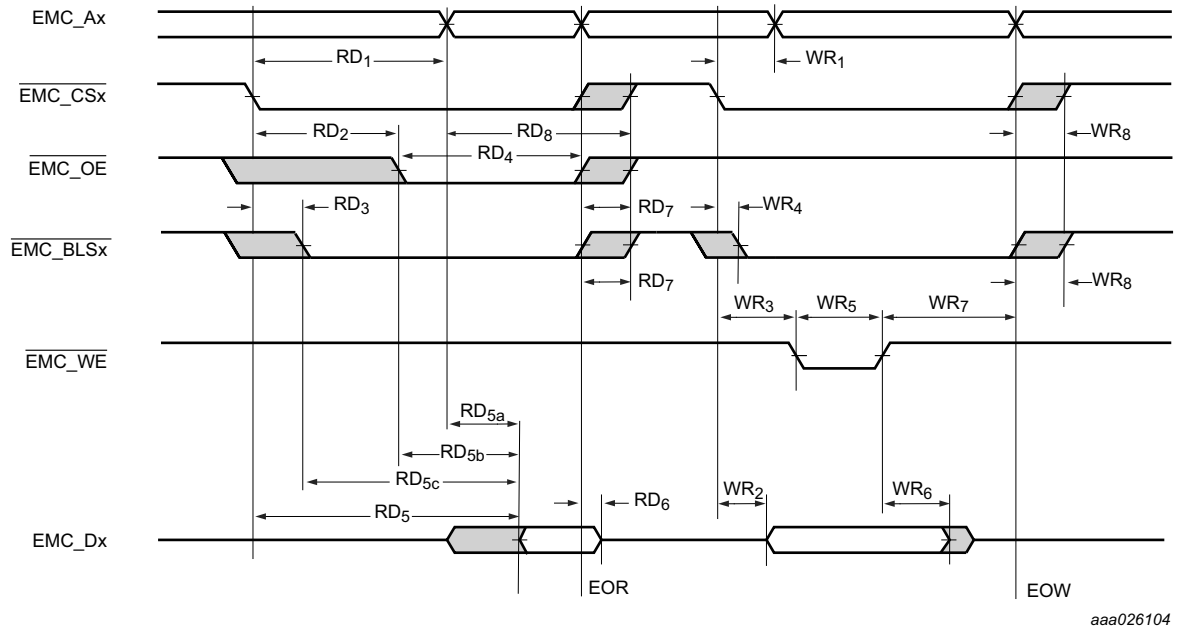

Fig 25. External static memory read/write access (PB =1)

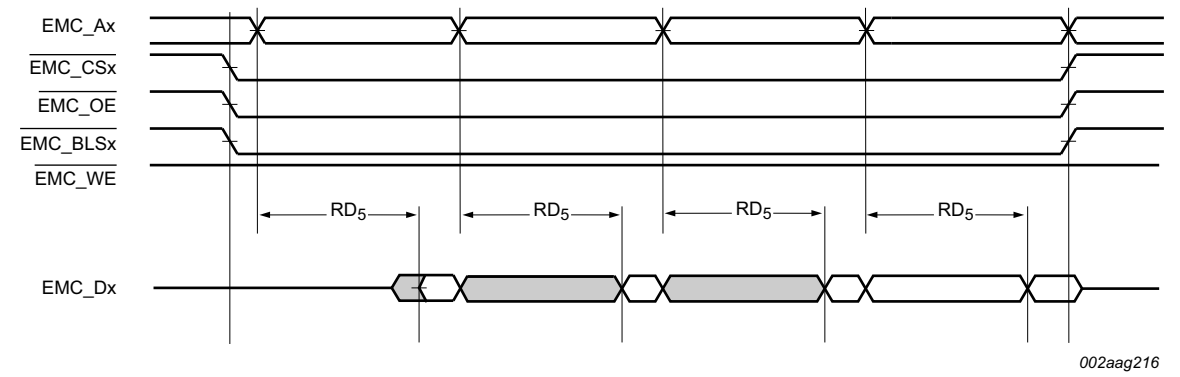

Fig 26. External static memory burst read cycle

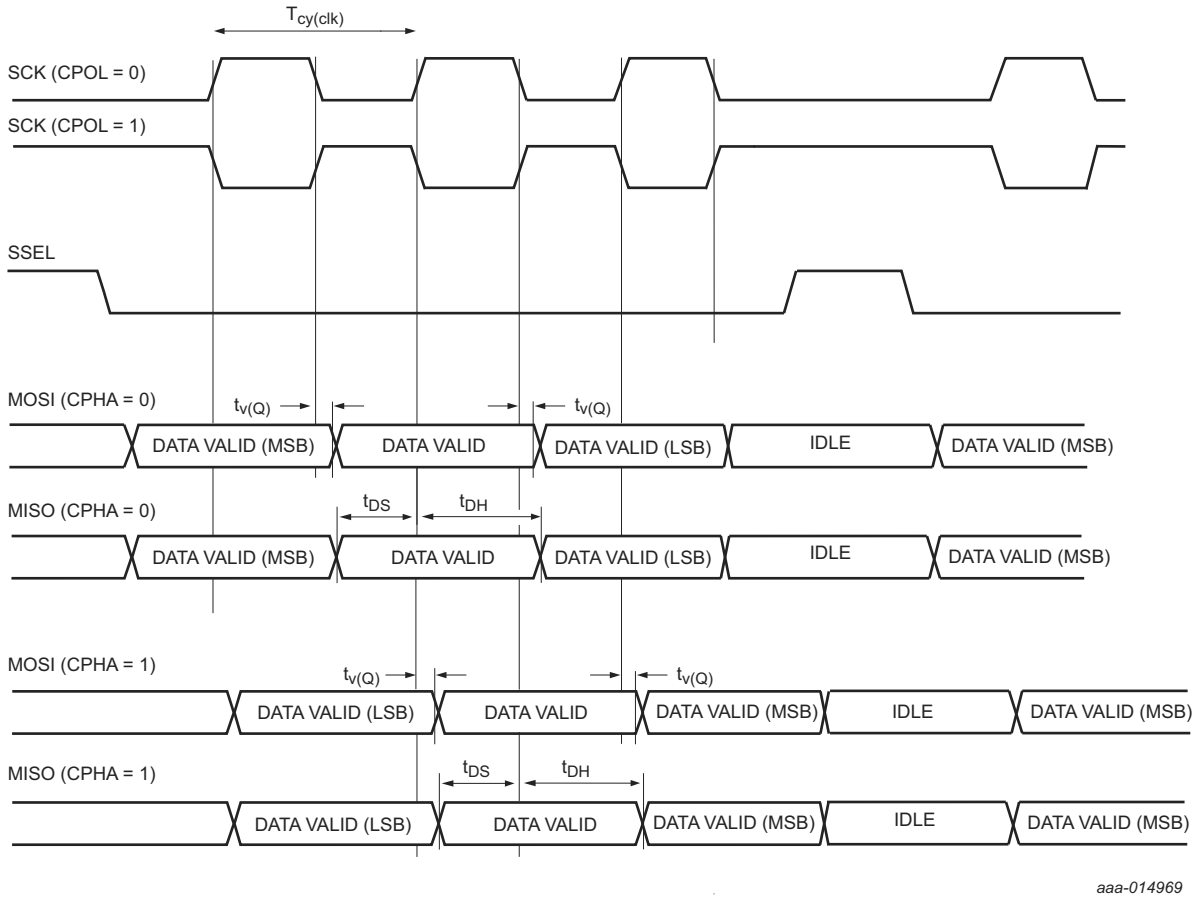

Fig 31. SPI master timing

12.2 12-bit ADC characteristics

Table 54. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±4.5	-	LSB
			[1][5]	-		-	LSB
$E_{L(adj)}$	integral non-linearity	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±7.5	-	LSB
			[1][6]	-		-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz		-	< ±2.5	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Updated a feature in Section 7.17.8.2 “SPI serial I/O controller”: Maximum data rate of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. Was 71 Mbit/s in master mode. • Updated Section 11.15 “SPI interfaces”: the maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s. • Updated Table 4 “Pin description”: Changed restate state of PIO3_23 and PIO0_24 to Z. Added footnote True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin to PIO3_23 and PIO0_24.			
LPC546xx v.1.9	20171109	Product data sheet	-	LPC546xx v.1.8
Modifications:	• Updated Table 1 “Ordering information” and Table 2 “Ordering options”. Added the part numbers: LPC54605J256BD100, LPC54605J512BD100, LPC54605J256ET100, LPC54605J512ET100.			
LPC546xx v.1.8	20170614	Product data sheet	-	LPC546xx v.1.7
Modifications:	• Updated Section 13.7 “Suggested USB interface solutions”. Removed the remark. • Added LPC5462x device to the data sheet. • Updated Timer and digital peripherals of Section 2 “Features and benefits”. • Updated Section 7.19.2 “SCTimer/PWM”, Section 7.19.2.1 “Features” and Section 7.18.3 “External memory controller”. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”. • Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”, Table 43 “SPI dynamic characteristics[1]”, Table 44 “Dynamic characteristics: SPIFI[1]”, Table 45 “Dynamic characteristics[1]”, Table 46 “Dynamic characteristics[1]”, Table 47 “USART dynamic characteristics[1]”, Table 50 “Dynamic characteristics: Ethernet”, Table 51 “Dynamic characteristics: SD/MMC and SDIO”, and Table 52 “Dynamic characteristics: LCD”: replaced the condition, CCLK > 100 MHz with 100 MHz <CCLK ≤ 180 MHz • Updated Table 12 “General operating conditions”. Added the condition, For OTP programming only to f_{clk}. • Added Remark to Section 7.24 “Code security (enhanced Code Read Protection - eCRP)”. • Updated Table 19 “Typical peripheral power consumption[1][2]”: added SYSOSC value. • Updated Table 14 “CoreMark score[1]”. • Updated Table 15 “Static characteristics: Power consumption in active and sleep mode”: I_{DD} supply current in Active mode: CoreMark code executed from flash. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”.			
LPC546xx v.1.7	20170428	Product data sheet	-	LPC546xx v.1.6
Modifications:	• Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”. • Updated Table 11 “Thermal resistance”.			
LPC546xx v.1.6		Product data sheet	-	LPC546xx v.1.5
Modifications:	• Added TFBGA100 and LQFP100 packages.			

21. Contents

continued >>