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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j256et100e

- CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - SCTimer/PWM with 8 input and 10 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 10 match/captures, 10 events, and 10 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - enhanced Code Read Protection (eCRP) to protect user code.
  - OTP memory for ECRP settings, and user application specific data.
  - Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ± 1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.

- yyww: Date code with yy = year and ww = week.
- xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 19.1

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_9	E10	G12	136	65	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
							I/O	**EMC_D[7] —** External Memory interface data [7].
PIO0_10/ ADC0_0	J1	P2	50	23	[4]	PU	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	K1	L3	51	24	[4]	PU	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
								R — Reserved.
								R — Reserved.
							I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_2	-	C3	4	-	[2]	PU	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	-	C1	12	-	[2]	PU	I/O	**PIO2_5 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	-	F3	17	-	[2]	PU	I/O	**PIO2_6 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	-	J2	29	-	[2]	PU	I/O	**PIO2_7 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_D(1) —** SD/MMC data 1.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_1	-	D11	159	-	[2]	PU	I/O	**PIO3_1 —** General-purpose digital input/output pin.
							O	**LCD_VD[15] —** LCD Data [15].
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO3_2	-	C10	164	-	[2]	PU	I/O	**PIO3_2 —** General-purpose digital input/output pin.
							O	**LCD_VD[16] —** LCD Data [16].
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO3_3	-	A13	169	-	[2]	PU	I/O	**PIO3_3 —** General-purpose digital input/output pin.
							O	**LCD_VD[17] —** LCD Data [17].
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_4	-	B11	172	-	[2]	PU	I/O	**PIO3_4 —** General-purpose digital input/output pin.
							O	**LCD_VD[18] —** LCD Data [18].
								R — Reserved.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
PIO3_5	-	B10	177	-	[2]	PU	I/O	**PIO3_5 —** General-purpose digital input/output pin.
							O	**LCD_VD[19] —** LCD Data [19].
								R — Reserved.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
PIO3_6	-	C9	180	-	[2]	PU	I/O	**PIO3_6 —** General-purpose digital input/output pin.
							O	**LCD_VD[20] —** LCD Data [20].
							O	**LCD_VD[0] —** LCD Data [0].
								R — Reserved.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
PIO3_7	-	B8	184	-	[2]	PU	I/O	**PIO3_7 —** General-purpose digital input/output pin.
							O	**LCD_VD[21] —** LCD Data [21].
							O	**LCD_VD[1] —** LCD Data [1].
								R — Reserved.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
USBn_DM	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USB1_AVSCC	F	Tie to VSS.
USB1_VBUS	F	Tie to VDD.
USB1_AVDDC3V3	F	Tie to VDD.
USB1_AVDDTX3V3	F	Tie to VDD.
USB1_AVSSTX3V3	F	Tie to VSS.
USB1_ID	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled, F = Floating

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down[2]
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating
PIO0_13 to PIO0_14 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
PIO3_23 to PIO3_24 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep and deep-sleep.

[2] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

7.13 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

Remark: If the ECRP is set to the most restrictive combination of OTP and the ECRP of the images, no future factory testing can be performed on the device.

7.14 Power control

The LPC546xx support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are three special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode that can be activated using the power API library from the LPCOpen software package.

7.14.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.14.2 Deep-sleep mode

In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled. The FRO is disabled. The flash memory is put in standby mode.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

GPIO Pin Interrupts, GPIO Group Interrupts, and selected peripherals such as USB0, USB1, DMIC, SPI, I2C, USART, WWDT, RTC, Micro-tick Timer, and BOD can be left running in deep sleep mode The FRO, RTC oscillator, and the watchdog oscillator can be left running.In some cases, DMA can operate in deep-sleep mode. For more details, see UM10912, LPC546xx. user manual.

7.14.3 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the RESET pin. The LPC546xx can wake up from deep power-down mode via the RESET pin and the RTC alarm. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
Flash	Software configured	Standby	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations. For more details, see UM10912, LPC546xx. user manual.	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB0	Software configured	Software configured	Off
USB1	Software configured	Software configured	Off
Ethernet	Software configured	Off	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

7.16.1 Features

- Pin interrupts:
  - Up to eight pins can be selected from all GPIO pins on ports 0 and 1 as edge-sensitive or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
  - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Level-sensitive interrupt pins can be HIGH-active or LOW-active.
  - Pin interrupts can wake up the device from sleep mode and deep-sleep mode.
- Pattern match engine:
  - Up to eight pins can be selected from all digital pins on ports 0 and 1 to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
  - Each bit slice minterm (product term) comprising of the specified boolean expression can generate its own, dedicated interrupt request.
  - Any occurrence of a pattern match can also be programmed to generate an RXEV notification to the CPU. The RXEV signal can be connected to a pin.
  - Pattern match can be used in conjunction with software to create complex state machines based on pin inputs.
  - Pattern match engine facilities wake-up only from active and sleep modes.

7.17 Serial peripherals

7.17.1 Full-speed USB Host/Device interface (USB0)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.17.1.1 USB0 device controller

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Supports 10 physical (5 logical) endpoints including two control endpoints.
- Single and double-buffering supported.
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types.
- Supports wake-up from reduced power mode on USB activity and remote wake-up.
- Supports SoftConnect.
- Link Power Management (LPM) supported.

7.17.3 Ethernet AVB

The Ethernet block enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration.

7.17.3.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Supports IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
  - Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.17.4 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the LPC546xx microcontroller with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.17.4.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.

7.18.4 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.18.4.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.19 Counter/timers

7.19.1 General-purpose 32-bit timers/external event counter

The LPC546xx includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
  - Set LOW on match.
  - Set HIGH on match.

7.21 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.21.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.22 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.23 Security features

The OTP memory contains a memory bank of 128 bits each. OTP bank contains 4 words: word 0 for ECRP, word 1 is reserved, words 2 and 3 can be used by user application for storing application specific options.

7.23.1 Features

- OTP memory.
- Random number generator (RNG).

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Master; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		21.4	-	30.4	ns
		100 MHz < CCLK ≤ 180 MHz		20.6	-	28.7	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		21.1	-	29	ns
		100 MHz < CCLK ≤ 180 MHz		20.3	-	28.3	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		1.3	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		2.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.3	-	-	ns
Slave; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		13.8	-	23.6	ns
		100 MHz < CCLK ≤ 180 MHz		13	-	21.9	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.2	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0.7	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		1.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.3	-	-	ns

[1] Based on characterization; not tested in production.

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM10912) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

11.16 SPIFI

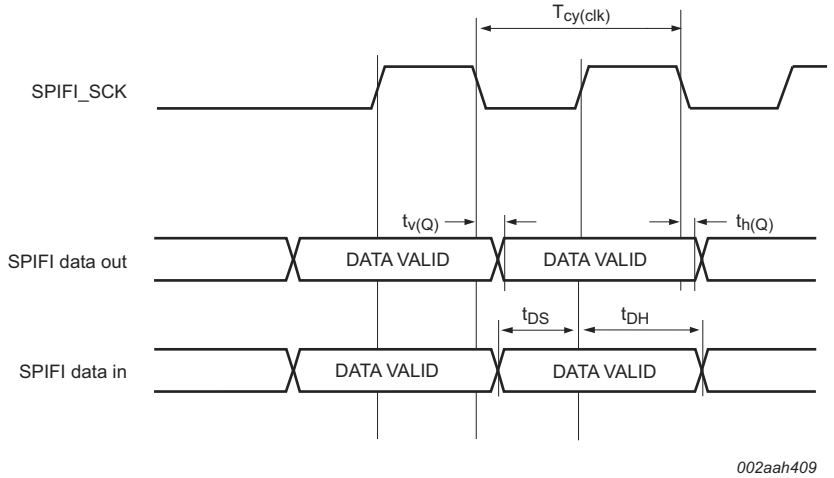
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 44. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge. Maximum SPIFI clock = 100 MHZ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		100 MHz < CCLK ≤ 180 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		100 MHz < CCLK ≤ 180 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 33. SPIFI control register (Mode 0)

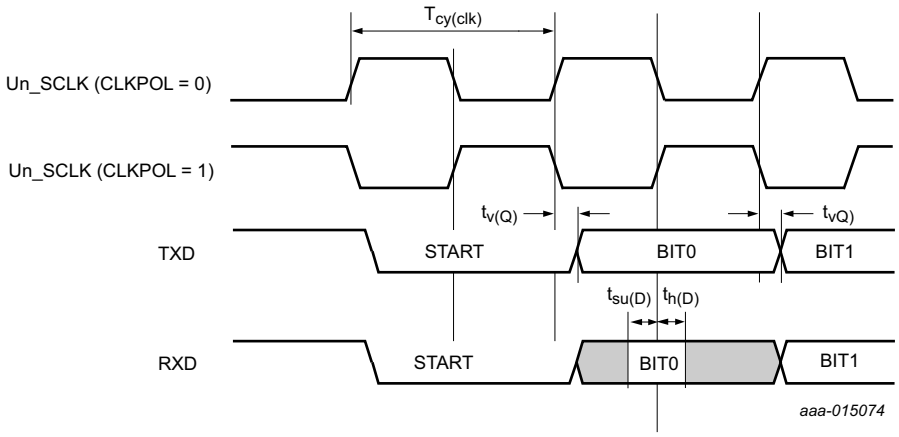


Fig 35. USART timing

11.20 SCTimer/PWM output timing

Table 48. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 90 % and 10 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	3.4	-	4.5	ns

11.21 USB interface characteristics

Table 49. Dynamic characteristics: USB0 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0		20	ns
t_f	fall time	10 % to 90 %		4.0		20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90		111.11	%
V_{CRS}	output signal crossover voltage			1.3		2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 36		160		175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 36		−2		+5	ns
t_{JR1}	receiver jitter to next transition			−18.5		+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 36	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 36	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 55. ADC sampling times[1]

-40 °C ≤ T_{amb} <= 85 °C; 1.71 V ≤ V_{DDA} ≤ 3.6 V; 1.71 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		47	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		38	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		30	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		22	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		74	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		105	-	-	ns

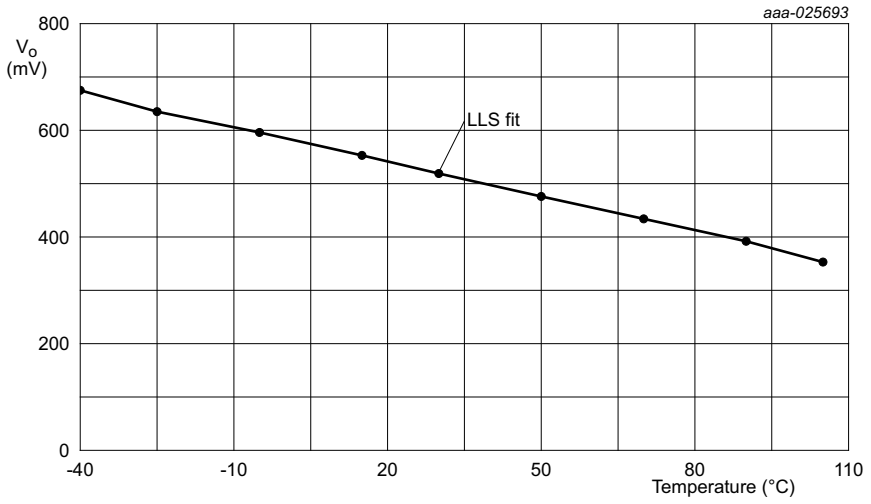
Table 57. Temperature sensor Linear-Least-Square (LLS) fit parameters

$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	[1]	-	−2.04	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C	[1]	-	584.0	-	mV
Value at 30 °C		[2]	515.9	-	531.5	mV

[1] Measured over typical samples.

[2] Measured for samples over process corners.



$V_{DD} = V_{DDA}$ 3.3 V; measured on matrix samples.

Fig 42. LLS fit of the temperature sensor output voltage

13.5 RTC oscillator

In the RTC oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on RTCXIN and RTCXOUT. See Figure 46.

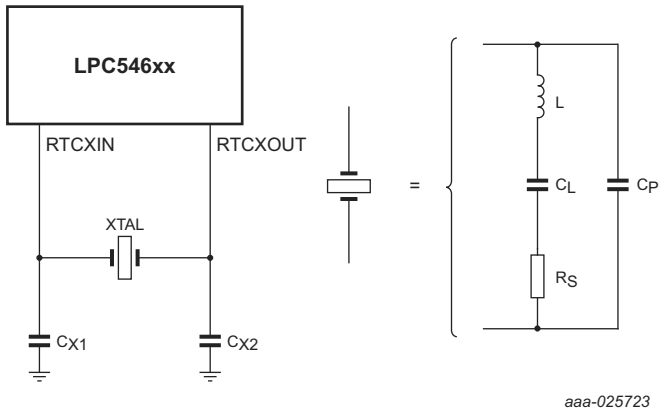


Fig 46. RTC oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the RTCXIN and RTCXOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, output the RTC Clock to the CLOCKOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC546xx v.1.5	20170331	Product data sheet	-	LPC546xx v.1.4
Modifications:	• Updated Table 51 “Dynamic characteristics: SD/MMC and SDIO”. The max clock frequency is 50 MHz. • Updated Section 7.18.2 “SD/MMC card interface”: Supports up to a maximum of 50 MHz of interface frequency. • Updated Table 41 “Dynamic characteristic: I2C-bus pins[1]” • Updated Figure 28 “I2S-bus timing (master)” and Figure 29 “I2S-bus timing (slave)”. • Updated Table 2 “Ordering options”. Parts LPC54618J512ET180 and LPC54618J512BD208 have Classic CAN. • Added Section 11.4 “Wake-up process”.			
LPC546xx v.1.4	20170307	Product data sheet	-	LPC5460x v.1.3
Modifications:	• Changed data sheet title to LPC546xx. • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes” and Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”.			
LPC5460x v.1.3	20170224	Product data sheet	-	LPC5460x v.1.2
Modifications:	• Removed S parts. Data sheet title renamed to LPC5460x. • Removed AES-256 engine and SHA references throughout the document. • Security peripherals renamed to Security features. • Updated Section 4 “Marking”. • Updated Section 5 “Block diagram”. • Updated Figure 6 “LPC546xx Memory mapping”. • Updated Table 20 “Typical AHB/APB peripheral power consumption [3][4][5]”.			
LPC5460x v.1.2	20170206	Product data sheet	-	LPC5460x v.1.1
Modifications:	• Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”: Static memory chip select: was 0x9000 0000 - 0x93 FFFF, now, 0x9000 0000 – 0x93FF FFFF. • Updated Figure 8 “LPC5460x clock generation”. • Updated Power control in Section 2 “Features and benefits”: Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes. • Updated Table 4 “Pin description”: PIO0_26, USB0_IDVALUE, Type is Input (I). • Updated Section 7.18.1.1 “Features”. • Updated Table 31 “Dynamic characteristics of the PLL0[1]”: Input frequency, $F_{in,}$ Max value is 25 MHZ.			
LPC5460x v.1.1	20170124	Product data sheet	-	LPC5460x v.1