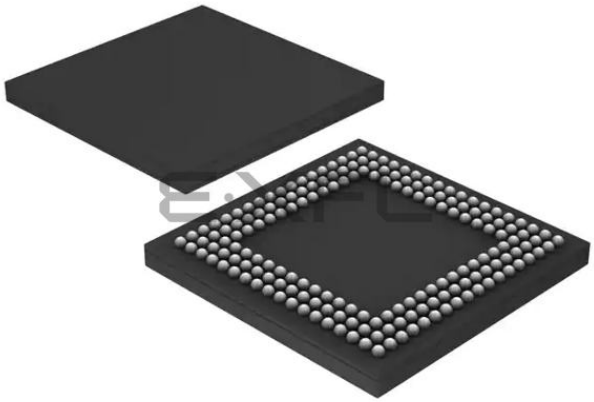

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	145
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j256et180e

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54605J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54605J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54606J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54607J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J256BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54608J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54608J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54616J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54616J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54616J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54616J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54618J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54618J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54628J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_22	K8	P11	89	43	[2]	PU	I/O	**PIO1_22 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**EMC_CKE[1] —** External memory interface SDRAM clock enable 1.
PIO1_23	K10	M10	97	46	[2]	PU	I/O	**PIO1_23 —** General-purpose digital input/output pin.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**EMC_A[11] —** External memory interface address 11.
PIO1_24	G8	N14	111	57	[2]	PU	I/O	**PIO1_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
								R — Reserved.
								R — Reserved.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	G10	M12	119	59	[2]	PU	I/O	**PIO1_25 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_A[13] —** External memory interface address 13.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_30	C6	A8	182	86	[2]	PU	I/O	**PIO1_30 —** General-purpose digital input/output pin.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I/O	**SD_D[7] —** SD/MMC data 7.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
							I/O	**EMC_D[14] —** External Memory interface data [14].
PIO1_31	A3	C5	195	92	[2]	PU	I/O	**PIO1_31 —** General-purpose digital input/output pin.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
								R — Reserved.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**EMC_D[15] —** External Memory interface data [15].
PIO2_0/ ADC0_7	-	P3	57	-	[4]	PU	I/O; AI	**PIO2_0/ADC0_7 —** General-purpose digital input/output pin. ADC input channel 7 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
								R — Reserved.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT1_CAP0 —** Capture input 0 to Timer 1.
PIO2_1/ ADC0_8	-	P4	58	-	[4]	PU	I/O; AI	**PIO2_1/ADC0_8 —** General-purpose digital input/output pin. ADC input channel 8 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
								R — Reserved.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_2	-	C3	4	-	[2]	PU	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	-	C1	12	-	[2]	PU	I/O	**PIO2_5 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	-	F3	17	-	[2]	PU	I/O	**PIO2_6 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	-	J2	29	-	[2]	PU	I/O	**PIO2_7 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_D(1) —** SD/MMC data 1.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_29	-	L13	112	-	[2]	PU	I/O	**PIO3_29 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[18] —** External memory interface address 18.
PIO3_30	-	K13	116	-	[2]	PU	I/O	**PIO3_30 —** General-purpose digital input/output pin.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[19] —** External memory interface address 19.
PIO3_31	-	J14	123	-	[2]	PU	I/O	**PIO3_31 —** General-purpose digital input/output pin.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
								R — Reserved.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**EMC_A[20] —** External memory interface address 20.
PIO4_0	-	H13	127	-	[2]	PU	I/O	**PIO4_0 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
								R — Reserved.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							O	**EMC_CSN[1] —** External memory interface static chip select 1(active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_1	-	G14	132	-	[2]	PU	I/O	**PIO4_1 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	-	F14	138	-	[2]	PU	I/O	**PIO4_2 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	-	F13	140	-	[2]	PU	I/O	**PIO4_3 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	-	D9	147	-	[2]	PU	I/O	**PIO4_4 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_9	-	A12	173	-	[2][8]	PU	I/O	**PIO4_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
PIO4_10	-	B9	181	-	[2]	PU	I/O	**PIO4_10 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
								SCT0_GPI3 — Pin input 3 to SCTimer/PWM.
PIO4_11	-	A9	183	-	[2]	PU	I/O	**PIO4_11 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
PIO4_12	-	A6	188	-	[2]	PU	I/O	**PIO4_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
PIO4_13	-	B6	190	-	[2]	PU	I/O	**PIO4_13 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
								R — Reserved.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO5_3	-	-	129	-	[2]	PU	I/O	**PIO5_3 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I/O	**EMC_D[30] —** External Memory interface data [30].
PIO5_4	-	-	135	-	[2]	PU	I/O	**PIO5_4 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							I	**CT3_CAP2 —** Capture input 2 to Timer 3.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
							I/O	**EMC_D[31] —** External Memory interface data [31].
PIO5_5	-	-	145	-	[2]	PU	I/O	**PIO5_5 —** General-purpose digital input/output pin.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**TRACECLK —** Trace clock.
							O	**EMC_A[21] —** External memory interface address 21.
PIO5_6	-	-	152	-	[2]	PU	I/O	**PIO5_6 —** General-purpose digital input/output pin.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**TRACEDATA[0] —** Trace data bit 0.
							O	**EMC_A[22] —** External memory interface address 22.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
USB1_AVDDC3V3	E1	G3	24	10				USB1 analog 3.3 V supply.
USB1_AVDDTX3V3	E2	H1	25	11				USB1 analog 3.3 V supply for line drivers.
USB1_DP	F2	H3	27	13	[6]		I/O	USB1 bidirectional D+ line.
USB1_DM	E3	H2	26	12	[6]		I/O	USB1 bidirectional D- line.
USB1_AVSSTX3V3	G1	J1	28	14				USB1 analog ground for line drivers.
USB0_DP	B3	E5	204	97	[6]		I/O	USB0 bidirectional D+ line.
USB0_DM	B2	D5	205	98	[6]		I/O	USB0 bidirectional D- line.
RESETN	J8	N13	101	48	[5]			External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.
VDD	D5; D7; E4; E6; F5; F7; G4; G6	E6; E8; F5; G5; J12; L6; L11	1; 48; 65; 104; 108; 156; 157; 206	1; 21; 33; 50; 54; 75; 76; 99		-	-	Single 1.71 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	D4; D6; E5; E7; F4; F6; G5; G7	B3; D7; D8; E11; H5; J5; K7	2; 49; 66; 103; 107; 148; 162; 201	2; 22; 34; 49; 53; 71; 79; 96		-	-	Ground.
VDDA	J4	N6	64	32		-	-	Analog supply voltage.
VREFN	-	N4	59	-		-	-	ADC negative reference voltage. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
VREFP	K4	P6	63	31		-	-	ADC positive reference voltage.
VSSA	H4	L5	60	30		-	-	Analog ground. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
XTALIN	H2	K4	41	20	[7]	-	-	Main oscillator input.
XTALOUT	G3	J4	40	19	[7]	-	-	Main oscillator output.
VBAT	K9	N11	94	45		-	-	Battery supply voltage. If no battery is used, tie VBAT to VDD or to ground.
RTCXIN	J9	L12	105	51		-	-	RTC oscillator input.
RTCXOUT	H9	K11	106	52		-	-	RTC oscillator output.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC546xx uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.

7.13 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

Remark: If the ECRP is set to the most restrictive combination of OTP and the ECRP of the images, no future factory testing can be performed on the device.

7.14 Power control

The LPC546xx support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are three special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode that can be activated using the power API library from the LPCOpen software package.

7.14.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.14.2 Deep-sleep mode

In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled. The FRO is disabled. The flash memory is put in standby mode.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

GPIO Pin Interrupts, GPIO Group Interrupts, and selected peripherals such as USB0, USB1, DMIC, SPI, I2C, USART, WWDT, RTC, Micro-tick Timer, and BOD can be left running in deep sleep mode The FRO, RTC oscillator, and the watchdog oscillator can be left running.In some cases, DMA can operate in deep-sleep mode. For more details, see UM10912, LPC546xx. user manual.

7.14.3 Deep power-down mode

In deep power-down mode, power is shut off to the entire chip except for the RTC power domain and the RESET pin. The LPC546xx can wake up from deep power-down mode via the RESET pin and the RTC alarm. The ALARM1HZ flag in RTC control register generates an RTC wake-up interrupt request, which can wake up the part. During deep power-down mode, the contents of the SRAM and registers are not retained. All functional pins are tri-stated in deep power-down mode.

Table 8 shows the peripheral configuration in reduced power modes.

Table 8. Peripheral configuration in reduced power modes

Peripheral	Reduced power mode		
	Sleep	Deep-sleep	Deep power-down
FRO	Software configured	Software configured	Off
Flash	Software configured	Standby	Off
BOD	Software configured	Software configured	Off
PLL	Software configured	Off	Off
Watchdog osc and WWDT	Software configured	Software configured	Off
Micro-tick Timer	Software configured	Software configured	Off
DMA	Active	Configurable some for operations. For more details, see UM10912, LPC546xx. user manual.	Off
USART	Software configured	Off; but can create a wake-up interrupt in synchronous slave mode or 32 kHz clock mode	Off
SPI	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
I2C	Software configured	Off; but can create a wake-up interrupt in slave mode	Off
USB0	Software configured	Software configured	Off
USB1	Software configured	Software configured	Off
Ethernet	Software configured	Off	Off
DMIC	Software configured	Software configured	Off
Other digital peripherals	Software configured	Off	Off
RTC oscillator	Software configured	Software configured	Software configured

- Supports DMA access.
- Provides XIP (execute in place) feature to execute code directly from serial flash.

7.17.5 CAN Flexible Data (CAN FD) interface

The LPC546xx contains two CAN FD interfaces, CAN FD 1 and CAN FD 2.

7.17.5.1 Features

- Conforms with CAN protocol version 2.0 part A, B and ISO 11898-1.
- CAN FD with up to 64 data bytes supported.
- CAN Error Logging.
- AUTOSAR support.
- SAE J1939 support.
- Improved acceptance filtering.

7.17.6 DMIC subsystem

7.17.6.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

7.17.7 Smart card interface

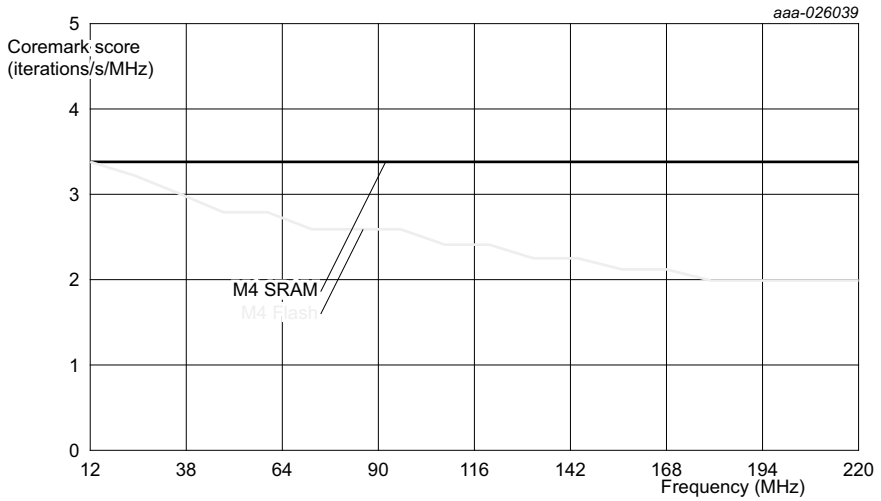
7.17.7.1 Features

- Two DMA supported ISO 7816 Smart Card Interfaces.
- Both asynchronous protocols, T = 0 and T = 1 are supported.

7.17.8 Flexcomm Interface serial communication

7.17.8.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASCFG register is set to 1. Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON. Coremark score is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark score from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark score from SRAMX: SRAM0 is powered; flash is powered down.

Fig 14. Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX

11.14 I²S-bus interface

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
Master; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		26.0	-	40.3	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.0	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		26.0	-	41.0	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.6	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		6.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		6.4	-	-	ns
Slave; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		18.8	-	37.1	ns
		100 MHz < CCLK ≤ 180 MHz		18.0	-	35.5	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.8	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.4	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		3.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.2	-	-	ns

12.2 12-bit ADC characteristics

Table 54. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±4.5	-	LSB
			[1][5]	-		-	LSB
$E_{L(adj)}$	integral non-linearity	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±7.5	-	LSB
			[1][6]	-		-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz		-	< ±2.5	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

Table 55. ADC sampling times[1] *...continued*
-40 °C ≤ T_{amb} <= 85 °C; 1.71 V ≤ V_{DDA} ≤ 3.6 V; 1.71 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	35	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		38	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		40	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		46	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		61	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		86	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	27	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		29	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		32	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		36	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		48	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		69	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		22	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		23	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		26	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		36	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		51	-	-	ns

[1] Characterized through simulation. Not tested in production.

[2] The ADC default sampling time is 2.5 ADC clock cycles. To match a given analog source output impedance, the sampling time can be extended by adding up to seven ADC clock cycles for a maximum sampling time of 9.5 ADC clock cycles. See the TSAMP bits in the ADC CTRL register.

[3] Z_o = analog source output impedance.

[4] For VDD ≤ 2.5 V, add one additional clock cycle to the values in Table 55.

12.2.1 ADC input impedance

Figure 41 shows the ADC input impedance. In this figure:

- ADCx represents slow ADC input channels 6 to 11.
- ADCy represents fast ADC input channels 0 to 5.
- R_1 and R_{sw} are the switch-on resistance on the ADC input channel.
- If fast channels (ADC inputs 0 to 5) are selected, the ADC input signal goes through R_{sw} to the sampling capacitor (C_{ia}).
- If slow channels (ADC inputs 6 to 11) are selected, the ADC input signal goes through R_1 + R_{sw} to the sampling capacitor (C_{ia}).
- Typical values, R_1 = 487 Ω, R_{sw} = 278 Ω
- See Table 21 for C_{io}.
- See Table 54 for C_{ia}.

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Regrouped Table 2 “Ordering options”. • Added text to Section 7.15.3.1 “Features”: Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details. • Removed Table note 2: fclk = cclk/CLKDIV +1. See LPC5460x UM10912 and updated Table note 1 “See the LPC5460x user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).”of Section 11.2 “EEPROM”. • Updated Table 50 “Dynamic characteristics: SD/MMC and SDIO”: changed the maximum clock frequency to 52 MHz. • Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”:			
LPC5460x v.1	20161215	Product data sheet	-	-