Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j512bd100e

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_14	A9	C12	160	78	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B5	B7	187	88	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
								R — Reserved.
							O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	H8	N12	98	47	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_8	-	F4	32	-	[2]	PU	I/O	**PIO2_8 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[2] —** SD/MMC data 2.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
PIO2_9	-	K2	36	-	[2]	PU	I/O	**PIO2_9 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[3] —** SD/MMC data 3.
								R — Reserved.
							O	**CT0_MAT1 —** Match output 0 from Timer 1.
PIO2_10	-	P1	39	-	[2]	PU	I/O	**PIO2_10 —** General-purpose digital input/output pin.
							I	**ENET_RX_ER —** Ethernet receive error (RMII/MII interface).
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
PIO2_11	-	K3	43	-	[2]	PU	I/O	**PIO2_11 —** General-purpose digital input/output pin.
							O	**LCD_PWR —** LCD panel power enable.
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
								R — Reserved.
								R — Reserved.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
PIO2_12	-	M2	45	-	[2]	PU	I/O	**PIO2_12 —** General-purpose digital input/output pin.
							O	**LCD_LE —** LCD line end signal.
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**USB0_IDVALUE —** Indicates to the transceiver whether connected as an A-device (USB0_ID LOW) or B-device (USB0_ID HIGH).
								R — Reserved.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_13	-	P7	70	-	[2]	PU	I/O	**PIO2_13 —** General-purpose digital input/output pin.
							O	**LCD_DCLK —** LCD panel clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
								R — Reserved.
								R — Reserved.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

7.12.1.3 Crystal oscillator

The LPC546xx include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC546xx will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 11 and Figure 12 for an overview of the LPC546xx clock generation.

7.12.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.17.3 Ethernet AVB

The Ethernet block enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration.

7.17.3.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Supports IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
  - Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.17.4 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the LPC546xx microcontroller with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.17.4.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.

7.17.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.17.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC546xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

7.18.3.1 Features

- Read and write buffers to reduce latency and to improve performance.
- Low transaction latency.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Dynamic memory interface support including single data rate SDRAM.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- EMC bus width (bit) on LQFP100 and TFBGA100 packages supports up to 8/16 data line wide static memory, in addition to dynamic memories, such as, SDRAM (2 banks only) with an SDRAM clock of up to 100 MHz.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

7.21 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.21.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.22 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.23 Security features

The OTP memory contains a memory bank of 128 bits each. OTP bank contains 4 words: word 0 for ECRP, word 1 is reserved, words 2 and 3 can be used by user application for storing application specific options.

7.23.1 Features

- OTP memory.
- Random number generator (RNG).

registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180MHz.

Table 19. Typical peripheral power consumption[1][2]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO	100
WDT OSC	2.0
Flash	200
BOD	2.0
SYSOSC	247

[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
USB0 device		0.3	0.3	0.3	0.4	0.5
USB1 device		4.4	4.4	4.4	5.0	6.5
DMIC		0.2	0.2	0.2	0.2	0.3
GPIO0	[1]	0.9	0.9	0.9	1.0	1.4
GPIO1	[1]	0.8	0.8	0.8	1.0	1.4
GPIO2	[1]	1.0	1.0	1.0	1.1	1.4
GPIO3	[1]	1.1	1.1	1.1	1.3	1.7
GPIO4	[1]	1.0	1.0	1.0	1.2	1.6
GPIO5	[1]	0.7	0.7	0.7	0.8	1.1
DMA		0.7	0.7	0.7	0.8	1.1
CRC		1.0	1.0	1.0	1.0	1.4
ADC0		1.6	1.6	1.6	1.9	2.6
SCTimer/PWM		4.5	4.5	4.5	5.3	7.0
Ethernet AVB		24.0	24.0	24.0	28.0	38.0
LCD		13.0	13.0	13.0	15.0	19.0
EEPROM		1.1	1.1	1.1	1.2	1.6
EMC		39.0	39.0	39.0	45.4	60.1
CAN0		10.8	10.8	10.8	12.6	16.5
CAN1		10.7	10.7	10.7	12.4	16.4
SD/MMC		7.9	7.9	7.9	9.3	12.3
Flexcomm Interface 0 (USART, SPI, I^2C)		1.6	1.6	1.6	1.9	2.5

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Flexcomm Interface1 (USART, SPI, I^2C)		1.6	1.6	1.6	1.8	2.4
Flexcomm Interface 2 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.6
Flexcomm Interface 3 (USART, SPI, I^2C)		1.4	1.4	1.4	1.6	2.2
Flexcomm Interface 4 (USART, SPI, I^2C)		1.4	1.5	1.5	1.7	2.3
Flexcomm Interface 5 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.5
Flexcomm Interface 6 (USART, SPI, I^2C, I^2S)		2.0	2.0	2.0	2.3	3.0
Flexcomm Interface 7 (USART, SPI, I^2C, I^2S)		1.6	1.6	1.6	1.9	2.5
Flexcomm Interface 8 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Flexcomm Interface 9 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
INPUTMUX	[1]	0.83	0.85	0.86	1.0	1.3
IOCON	[1]	2.67	2.65	2.65	3.13	4.2
PINT		1.1	1.1	1.1	1.3	1.8
GINT0 and GINT1		1.33	1.35	1.34	1.52	2.0
WWDT		0.42	0.42	0.42	0.46	0.6
RTC		0.3	0.3	0.3	0.3	0.4
MRT		0.3	0.3	0.3	0.3	0.4
RIT		0.1	0.1	0.1	0.1	0.1
UTICK		0.2	0.2	0.2	0.2	0.3
CTimer0		0.8	0.8	0.8	0.9	1.3
CTimer1		0.8	0.9	0.9	1.0	1.4
CTimer2		0.83	0.85	0.88	0.99	1.3
Smart card0		2.5	2.5	2.5	2.8	3.7
Smart card1		2.5	2.5	2.5	2.8	3.7
RNG		1.4	1.4	1.4	1.5	2.0
OTP controller		4.0	4.0	4.0	4.5	6.0
SHA		1.2	1.2	1.2	1.3	1.7

11.4 Wake-up process

Table 25. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.0	-	µs
		from deep-sleep mode; SRAMx powered. SRAM0, SRAM1, SRAM2, SRAM3, and USB SRAM powered down.	[2][5]	-	150	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

11.5 External memory interface

Table 26. Dynamic characteristics: Static external memory interface

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB; Values based on simulation.

Symbol	Parameter[1]	Conditions[1]		Min	Typ	Max	Unit
Read cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	RD_1		−1.2	-	1.6	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	RD_2	[2]	0.4+ $T_{cy(clk)}$ × WAITOEN	-	0.8+ $T_{cy(clk)}$ × WAITOEN	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	RD_3; PB = 1	[2][6]	−1.6	-	0	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	RD_4	[2]	(WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	-	0.3 + (WAITRD − WAITOEN + 1) × $T_{cy(clk)}$	ns
t_{am}	memory access time	RD_5	[2][3]	−6.7 + (WAITRD − WAITOEN +1) × $T_{cy(clk)}$	-	-	ns
$t_{h(D)}$	data input hold time	RD_6	[2][4]	−4.8	-	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	PB = 1	[6]	0.8	-	1.5	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		[2]	0.5	-	0.9	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		[2]	−0.4	-	0	ns
t_{deact}	deactivation time	RD_7	[2]	0.5	-	0.9	ns
Write cycle parameters							
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	WR_1		0.1	-	0.5	ns
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	WR_2		1.0	-	2.2	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	WR_3; PB =1	[2][6]	−0.6	-	0	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	WR_4; PB = 1	[2][6]	−1.2	-	0	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	WR_5; PB =1	[2][6]	(WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	-	0.1 + (WAITWR − WAITWEN + 1) × $T_{cy(clk)}$	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	PB = 1	[2][6]	2.5	-	5.5	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	WR_6; PB =1	[2][6]	1.6	-	2.9	ns
t_{WEHEOW}	$\overline{WE}$ HIGH to end of write time	WR_7; PB = 1	[2][5][6]	0.6	-	0.9	ns

11.19 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 47. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	21.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	19.7	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	0	-	4.9	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	4.5	ns
USART slave (in synchronous mode)1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.4	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	20.2	-	39.5	ns
		100 MHz < CCLK ≤ 180 MHz	19.3	-	37.7	ns
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		100 MHz < CCLK ≤ 180 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		100 MHz < CCLK ≤ 180 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

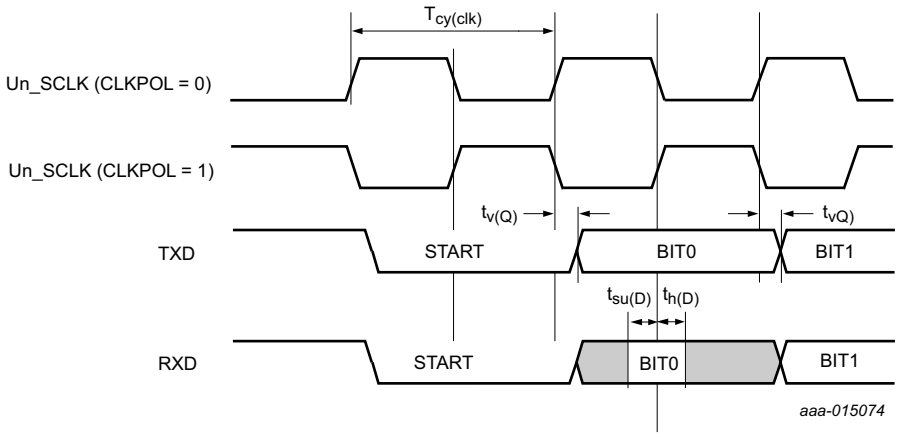


Fig 35. USART timing

11.20 SCTimer/PWM output timing

Table 48. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 90 % and 10 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	3.4	-	4.5	ns

11.21 USB interface characteristics

Table 49. Dynamic characteristics: USB0 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0		20	ns
t_f	fall time	10 % to 90 %		4.0		20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90		111.11	%
V_{CRS}	output signal crossover voltage			1.3		2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 36		160		175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 36		−2		+5	ns
t_{JR1}	receiver jitter to next transition			−18.5		+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 36	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 36	[1]	82	-	-	ns

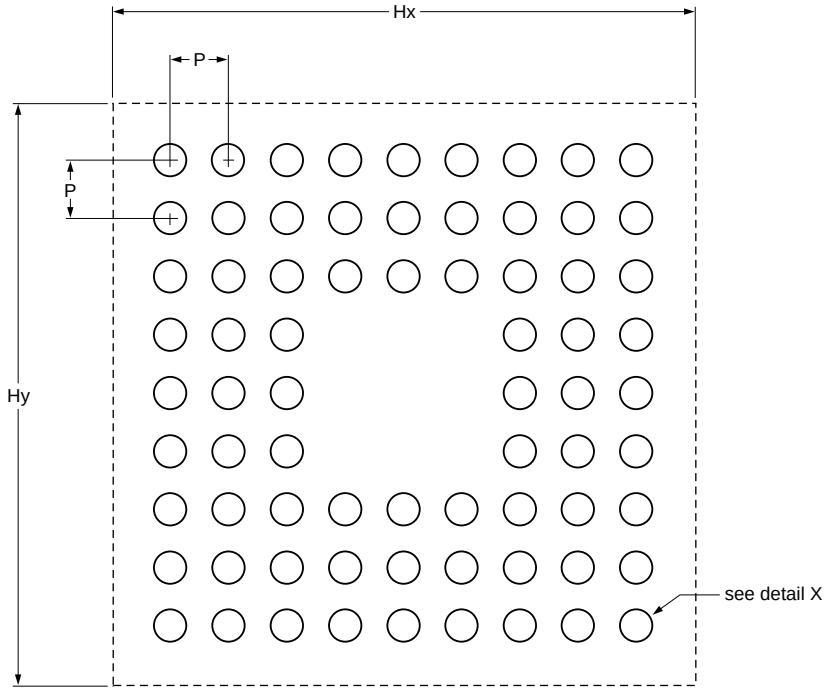
[1] Characterized but not implemented as production test. Guaranteed by design.

Table 55. ADC sampling times[1]

-40 °C ≤ T_{amb} <= 85 °C; 1.71 V ≤ V_{DDA} ≤ 3.6 V; 1.71 V ≤ V_{DD} ≤ 3.6 V

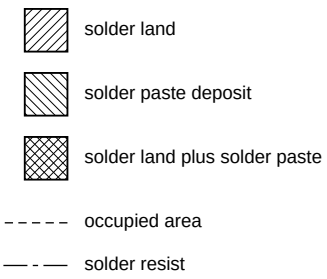
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		47	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		38	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		30	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		22	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		74	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		105	-	-	ns

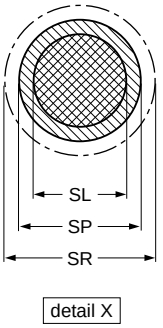
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 57. Reflow soldering of the TFBGA100 package

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Updated a feature in Section 7.17.8.2 “SPI serial I/O controller”: Maximum data rate of 48 Mbit/s in master mode and 14 Mbit/s in slave mode for SPI functions. Was 71 Mbit/s in master mode. • Updated Section 11.15 “SPI interfaces”: the maximum supported bit rate for SPI master mode is 48 Mbit/s. Was 71 Mbit/s. • Updated Table 4 “Pin description”: Changed restate state of PIO3_23 and PIO0_24 to Z. Added footnote True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin to PIO3_23 and PIO0_24.			
LPC546xx v.1.9	20171109	Product data sheet	-	LPC546xx v.1.8
Modifications:	• Updated Table 1 “Ordering information” and Table 2 “Ordering options”. Added the part numbers: LPC54605J256BD100, LPC54605J512BD100, LPC54605J256ET100, LPC54605J512ET100.			
LPC546xx v.1.8	20170614	Product data sheet	-	LPC546xx v.1.7
Modifications:	• Updated Section 13.7 “Suggested USB interface solutions”. Removed the remark. • Added LPC5462x device to the data sheet. • Updated Timer and digital peripherals of Section 2 “Features and benefits”. • Updated Section 7.19.2 “SCTimer/PWM”, Section 7.19.2.1 “Features” and Section 7.18.3 “External memory controller”. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”. • Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”, Table 43 “SPI dynamic characteristics[1]”, Table 44 “Dynamic characteristics: SPIFI[1]”, Table 45 “Dynamic characteristics[1]”, Table 46 “Dynamic characteristics[1]”, Table 47 “USART dynamic characteristics[1]”, Table 50 “Dynamic characteristics: Ethernet”, Table 51 “Dynamic characteristics: SD/MMC and SDIO”, and Table 52 “Dynamic characteristics: LCD”: replaced the condition, CCLK > 100 MHz with 100 MHz <CCLK ≤ 180 MHz • Updated Table 12 “General operating conditions”. Added the condition, For OTP programming only to f_{clk}. • Added Remark to Section 7.24 “Code security (enhanced Code Read Protection - eCRP)”. • Updated Table 19 “Typical peripheral power consumption[1][2]”: added SYSOSC value. • Updated Table 14 “CoreMark score[1]”. • Updated Table 15 “Static characteristics: Power consumption in active and sleep mode”: I_{DD} supply current in Active mode: CoreMark code executed from flash. • Updated Figure 13 “Typical CoreMark score (iterations/s) vs. Frequency (MHz) from flash and SRAMX” and Figure 14 “CoreMark power consumption: typical mA/MHz vs. frequency (MHz) from flash and SRAMX”.			
LPC546xx v.1.7	20170428	Product data sheet	-	LPC546xx v.1.6
Modifications:	• Updated Table 42 “Dynamic characteristics: I2S-bus interface pins [1][4]”. • Updated Table 11 “Thermal resistance”.			
LPC546xx v.1.6		Product data sheet	-	LPC546xx v.1.5
Modifications:	• Added TFBGA100 and LQFP100 packages.			

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Regrouped Table 2 “Ordering options”. • Added text to Section 7.15.3.1 “Features”: Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details. • Removed Table note 2: fclk = cclk/CLKDIV +1. See LPC5460x UM10912 and updated Table note 1 “See the LPC5460x user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).”of Section 11.2 “EEPROM”. • Updated Table 50 “Dynamic characteristics: SD/MMC and SDIO”: changed the maximum clock frequency to 52 MHz. • Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”:			
LPC5460x v.1	20161215	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.