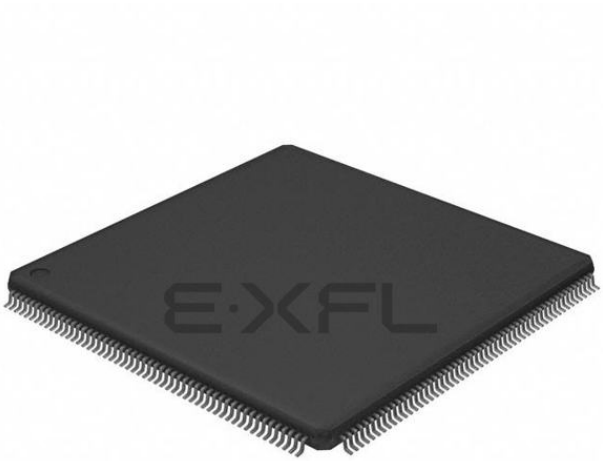

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	171
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j512bd208e

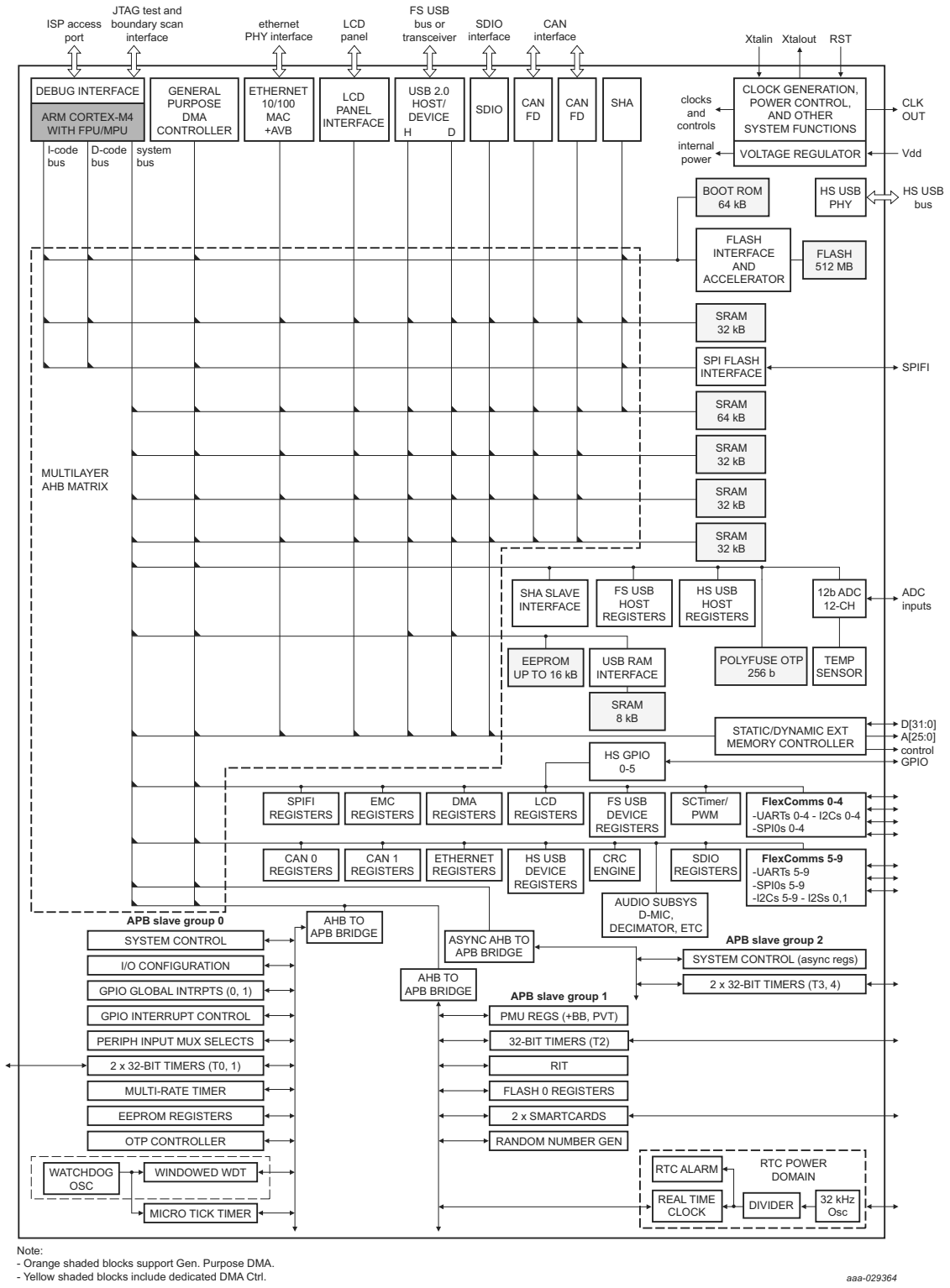


Fig 4. LPC546xx Block diagram

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_15/ ADC0_3	K2	L4	53	26	[4]	PU	I/O; AI	**PIO0_15/ADC0_3 —** General-purpose digital input/output pin. ADC input channel 3 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_CTS_SDA_SSEL0 —** Flexcomm 6: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_WEN —** External memory interface Write Enable (active low).
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
PIO0_16/ ADC0_4	H3	M4	54	27	[4]	PU	I/O; AI	**PIO0_16/ADC0_4 —** General-purpose digital input/output pin. ADC input channel 4 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.ws
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CLKOUT —** Output of the CLKOUT function.
							I	**CT1_CAP0 —** Capture input 0 to Timer 1.
								R — Reserved.
								R — Reserved.
							O	**EMC_CSN[0] —** External memory interface static chip select 0 (active low).
							O	**ENET_TXD0 —** Ethernet transmit data 0.
PIO0_17	B10	E14	146	70	[2]	PU	I/O	**PIO0_17 —** General-purpose digital input/output pin.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							I	**SD_CARD_DET_N —** SD/MMC card detect (active low).
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							O	**EMC_OEN —** External memory interface output enable (active low)
							O	**ENET_TXD1 —** Ethernet transmit data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_2	G9	L14	117	58	[2]	PU	I/O	**PIO1_2 —** General-purpose digital input/output pin.
							O	**CAN0_TD —** Transmitter output for CAN0.
								R — Reserved.
							O	**CT0_MAT3 —** Match output 3 from Timer0.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
								R — Reserved.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_3	F10	J13	120	60	[2]	PU	I/O	**PIO1_3 —** General-purpose digital input/output pin.
							I	**CAN0_RD —** Receiver input for CAN0.
								R — Reserved.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_4	C3	D4	3	3	[2]	PU	I/O	**PIO1_4 —** General-purpose digital input/output pin.
							I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
							I/O	**SD_D[0] —** SD/MMC data 0.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
							I/O	**EMC_D[11]) —** External Memory interface data [11].
PIO1_5	C2	E4	5	4	[2]	PU	I/O	**PIO1_5 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[4] —** External memory interface address 4.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_26	E8	J10	131	63	[2]	PU	I/O	**PIO1_26 —** General-purpose digital input/output pin.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_A[8] —** External memory interface address 8.
PIO1_27	D8	F10	142	68	[2]	PU	I/O	**PIO1_27 —** General-purpose digital input/output pin.
							I/O	**FC2_RTS_SCL_SSEL1 —** Flexcomm 2: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[4] —** SD/MMC data 4.
							O	**CT0_MAT3 —** Match output 3 from Timer 0.
							O	**CLKOUT —** Output of the CLKOUT function.
								R — Reserved.
							O	**EMC_A[9] —** External memory interface address 9.
PIO1_28	A10	E12	151	73	[2]	PU	I/O	**PIO1_28 —** General-purpose digital input/output pin.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
							I/O	**SD_D[5] —** SD/MMC data 5.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
								R — Reserved.
								R — Reserved.
							I/O	**EMC_D[12] —** External Memory interface data [12].
PIO1_29	A8	C11	165	81	[2][8]	PU	I/O	**PIO1_29 —** General-purpose digital input/output pin.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I/O	**SD_D[6] —** SD/MMC data 6.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							I/O	**EMC_D[13] —** External Memory interface data [13].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_1	-	D11	159	-	[2]	PU	I/O	**PIO3_1 —** General-purpose digital input/output pin.
							O	**LCD_VD[15] —** LCD Data [15].
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO3_2	-	C10	164	-	[2]	PU	I/O	**PIO3_2 —** General-purpose digital input/output pin.
							O	**LCD_VD[16] —** LCD Data [16].
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO3_3	-	A13	169	-	[2]	PU	I/O	**PIO3_3 —** General-purpose digital input/output pin.
							O	**LCD_VD[17] —** LCD Data [17].
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_4	-	B11	172	-	[2]	PU	I/O	**PIO3_4 —** General-purpose digital input/output pin.
							O	**LCD_VD[18] —** LCD Data [18].
								R — Reserved.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
PIO3_5	-	B10	177	-	[2]	PU	I/O	**PIO3_5 —** General-purpose digital input/output pin.
							O	**LCD_VD[19] —** LCD Data [19].
								R — Reserved.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
PIO3_6	-	C9	180	-	[2]	PU	I/O	**PIO3_6 —** General-purpose digital input/output pin.
							O	**LCD_VD[20] —** LCD Data [20].
							O	**LCD_VD[0] —** LCD Data [0].
								R — Reserved.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
PIO3_7	-	B8	184	-	[2]	PU	I/O	**PIO3_7 —** General-purpose digital input/output pin.
							O	**LCD_VD[21] —** LCD Data [21].
							O	**LCD_VD[1] —** LCD Data [1].
								R — Reserved.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

7.23.2 SHA-1 and SHA-2

The Hash peripheral is used to perform SHA-1 and SHA-2 (256) based hashing. A hash takes an arbitrarily large message or image and forms a relatively small fixed size “unique” number called a digest. The data is fed by words from the processor, DMA, or hosted access; the words are converted from little-endian (ARM standard) to big-endian (SHA standard) by the block.

7.23.2.1 Features

- Used with an HMAC to support a challenge/response or to validate a message.
- Can be used to verify external memory that has not been compromised.

7.24 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

7.25 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.

Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
Flexcomm Interface1 (USART, SPI, I^2C)		1.6	1.6	1.6	1.8	2.4
Flexcomm Interface 2 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.6
Flexcomm Interface 3 (USART, SPI, I^2C)		1.4	1.4	1.4	1.6	2.2
Flexcomm Interface 4 (USART, SPI, I^2C)		1.4	1.5	1.5	1.7	2.3
Flexcomm Interface 5 (USART, SPI, I^2C)		1.7	1.7	1.7	1.9	2.5
Flexcomm Interface 6 (USART, SPI, I^2C, I^2S)		2.0	2.0	2.0	2.3	3.0
Flexcomm Interface 7 (USART, SPI, I^2C, I^2S)		1.6	1.6	1.6	1.9	2.5
Flexcomm Interface 8 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Flexcomm Interface 9 (USART, SPI, I^2C)		1.5	1.5	1.5	1.8	2.3
Sync APB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
INPUTMUX	[1]	0.83	0.85	0.86	1.0	1.3
IOCON	[1]	2.67	2.65	2.65	3.13	4.2
PINT		1.1	1.1	1.1	1.3	1.8
GINT0 and GINT1		1.33	1.35	1.34	1.52	2.0
WWDT		0.42	0.42	0.42	0.46	0.6
RTC		0.3	0.3	0.3	0.3	0.4
MRT		0.3	0.3	0.3	0.3	0.4
RIT		0.1	0.1	0.1	0.1	0.1
UTICK		0.2	0.2	0.2	0.2	0.3
CTimer0		0.8	0.8	0.8	0.9	1.3
CTimer1		0.8	0.9	0.9	1.0	1.4
CTimer2		0.83	0.85	0.88	0.99	1.3
Smart card0		2.5	2.5	2.5	2.8	3.7
Smart card1		2.5	2.5	2.5	2.8	3.7
RNG		1.4	1.4	1.4	1.5	2.0
OTP controller		4.0	4.0	4.0	4.5	6.0
SHA		1.2	1.2	1.2	1.3	1.7

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM10912* LPC546xx *manual*).

[3] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM10912* LPC546xx *manual*).

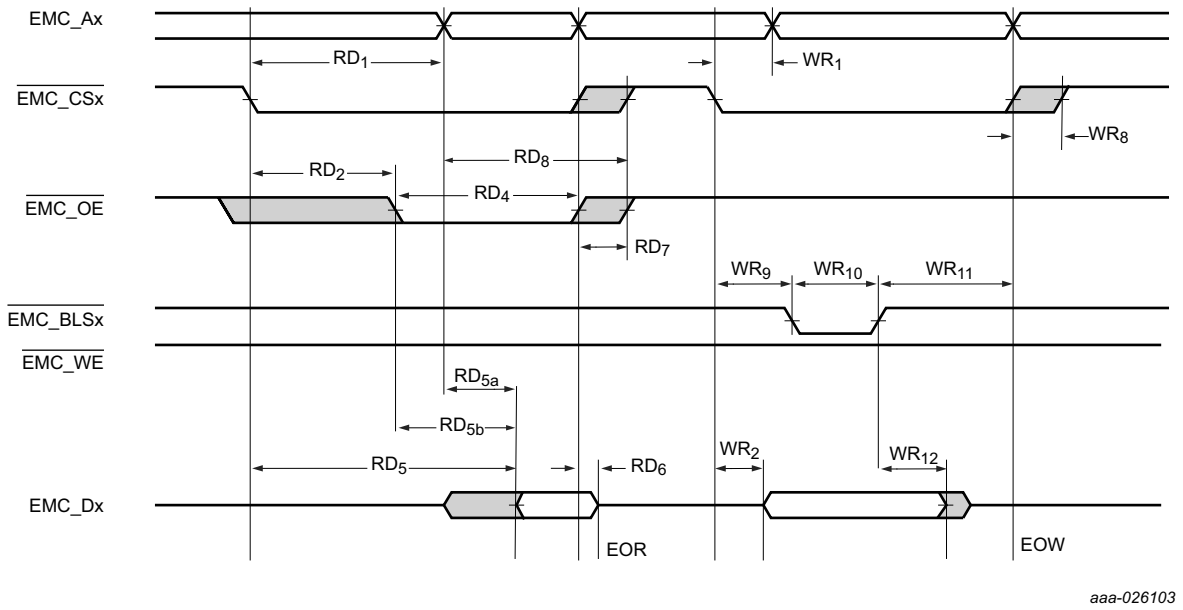


Fig 24. External static memory read/write access (PB = 0)

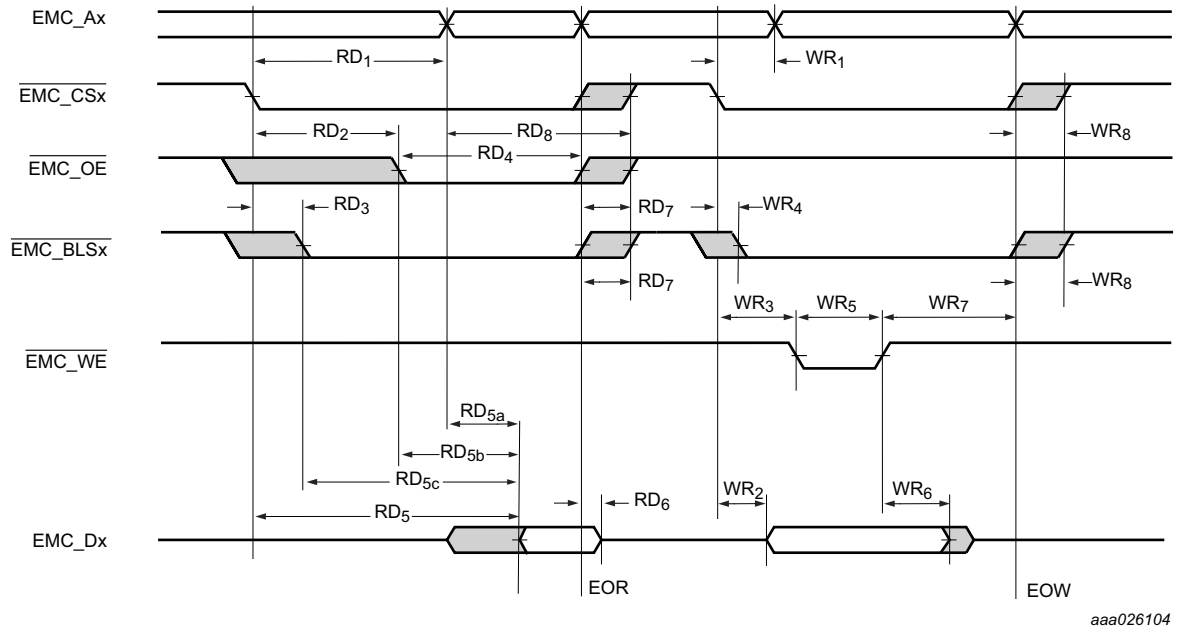


Fig 25. External static memory read/write access (PB =1)

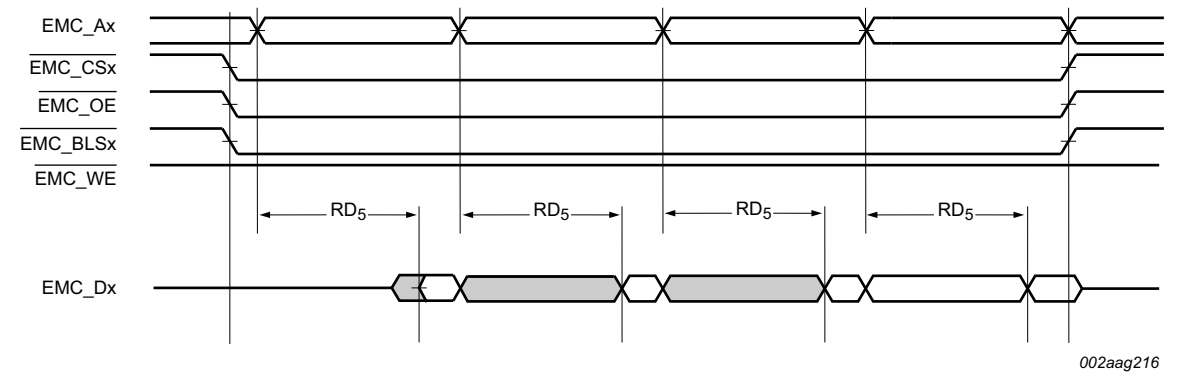


Fig 26. External static memory burst read cycle

Table 36. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 540$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.9 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 37. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.10 Crystal oscillator

Table 38. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

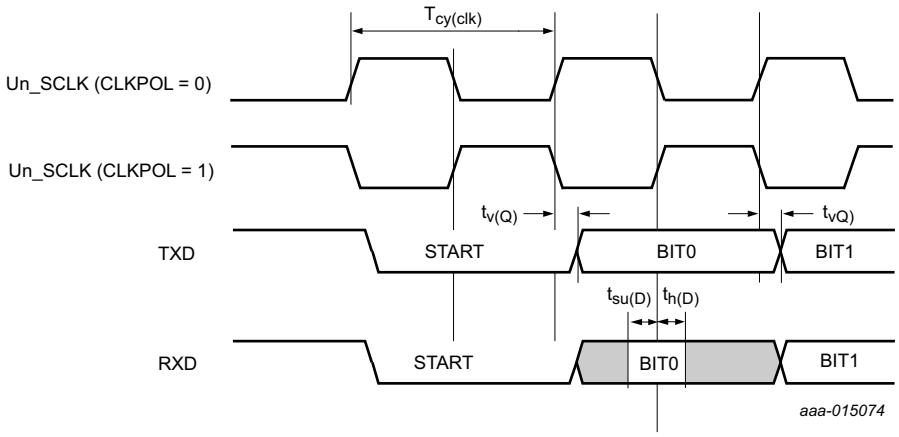


Fig 35. USART timing

11.20 SCTimer/PWM output timing

Table 48. SCTimer/PWM output dynamic characteristics

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V C_L = 30 pF. Simulated skew (over process, voltage, and temperature) of any two SCT fixed-pin output signals; sampled at the 90 % and 10 % level of the rising or falling edge; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(o)}$	output skew time	-	3.4	-	4.5	ns

11.21 USB interface characteristics

Table 49. Dynamic characteristics: USB0 pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		4.0		20	ns
t_f	fall time	10 % to 90 %		4.0		20	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		90		111.11	%
V_{CRS}	output signal crossover voltage			1.3		2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 36		160		175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 36		−2		+5	ns
t_{JR1}	receiver jitter to next transition			−18.5		+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 36	[1]	40	-		ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 36	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

12.2 12-bit ADC characteristics

Table 54. 12-bit ADC static characteristics

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; V_{SSA} = VREFN = GND. ADC calibrated at T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
V_{IA}	analog input voltage		[3]	0	-	V_{DDA}	V
C_{ia}	analog input capacitance		[4]	-	5.0	-	pF
$f_{clk(ADC)}$	ADC clock frequency				-	80	MHz
f_s	sampling frequency			-	-	5.0	Msamples/s
E_D	differential linearity error	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][5]	-	< ±4.5	-	LSB
			[1][5]	-		-	LSB
$E_{L(adj)}$	integral non-linearity	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±4.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz	[1][6]	-	< ±7.5	-	LSB
			[1][6]	-		-	LSB
E_O	offset error	calibration enabled	[1][7]	-	< ±2.2	-	mV
$V_{err(FS)}$	full-scale error voltage	2.0 V < V_{DDA} ≤ 3.6 V 2.0 V < VREFP ≤ 3.6 V $f_{clk(ADC)}$ = 80 MHz	[1][8]	-	< ±3.0	-	LSB
		1.71 V ≤ V_{DDA} ≤ 2.0 V 1.71 V ≤ VREFP ≤ 2.0 V $f_{clk(ADC)}$ = 80 MHz		-	< ±2.5	-	LSB
Z_i	input impedance	f_s = 5.0 Msamples/s	[9][10]	17.0	-	-	kΩ

[1] Based on characterization; not tested in production.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] The input resistance of ADC channels 6 to 11 is higher than ADC channels 0 to 5.

[4] C_{ia} represents the external capacitance on the analog input channel for sampling speeds of 5.0 Msamples/s. No parasitic capacitances included.

[5] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 40.

[6] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 40.

[7] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 40.

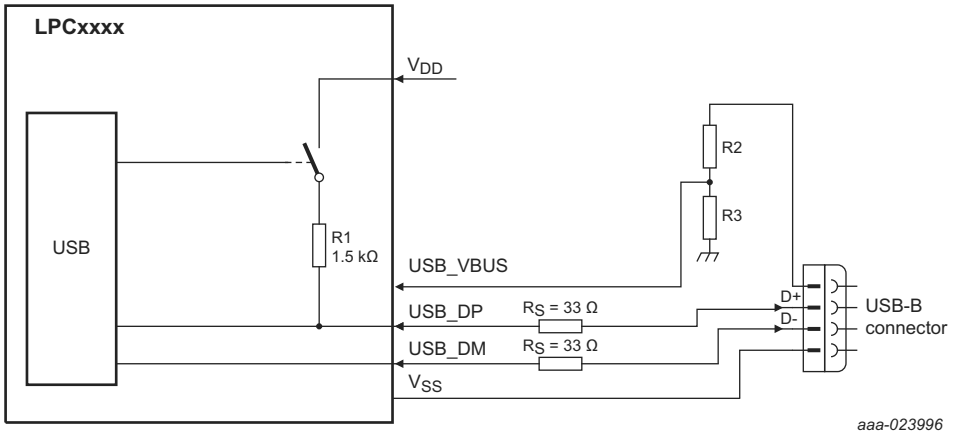
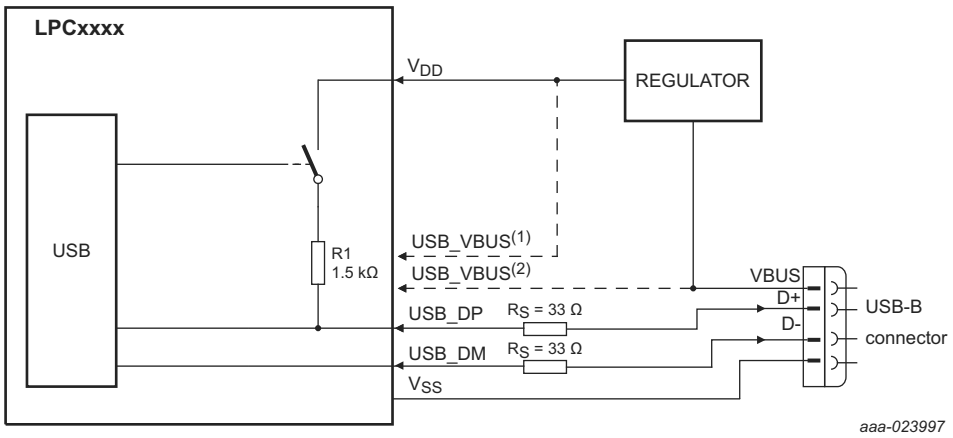


Fig 48. USB interface on a self-powered device where USB_VBUS = 5 V

The internal pull-up (1.5 kΩ) can be enabled by setting the DCON bit in the DEVCMDSTAT register to prevent the USB from timing out when there is a significant delay between power-up and handling USB traffic. External circuitry is not required.



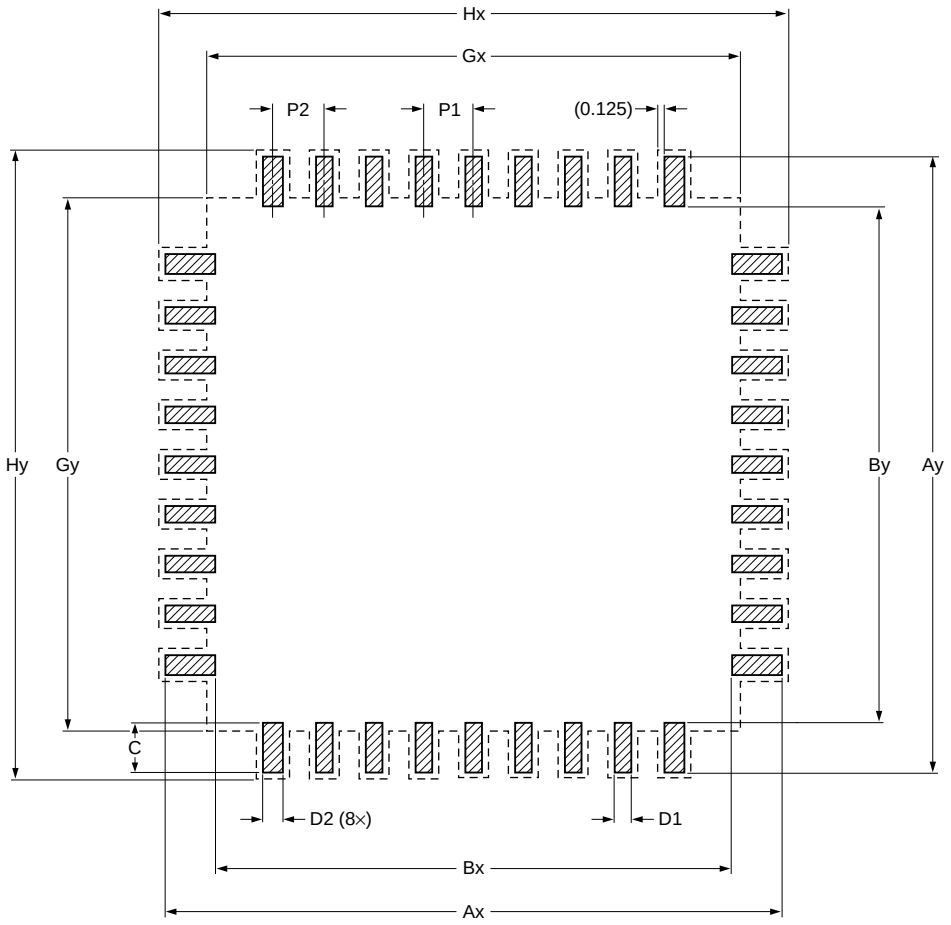
Two options exist for connecting VBUS to the USB_VBUS pin:

(1) Connect the regulator output to USB_VBUS. In this case, the USB_VBUS signal is HIGH whenever the part is powered.

(2) Connect the VBUS signal directly from the connector to the USB_VBUS pin. In this case, 5 V are applied to the USB_VBUS pin while the regulator is ramping up to supply V_{DD}. Since the USB_VBUS pin is only 5 V tolerant when V_{DD} is at operating level, this connection can degrade the performance of the part over its lifetime. Simulation shows that lifetime is reduced to 15 years at T_{amb} = 45 °C and 8 years at T_{amb} = 55 °C assuming that USB_VBUS = 5 V is applied continuously while V_{DD} = 0 V.

Fig 49. USB interface on a bus-powered device

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

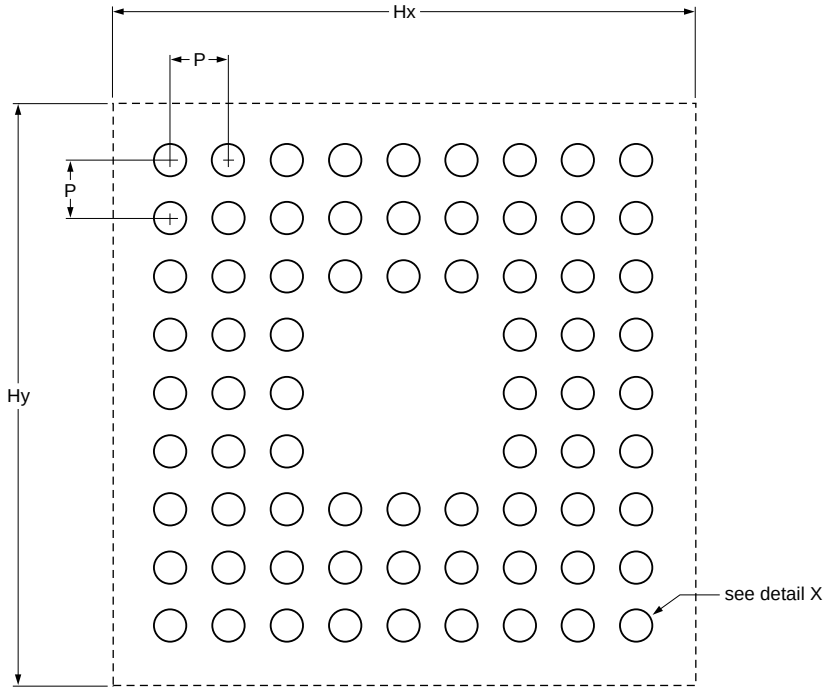
DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

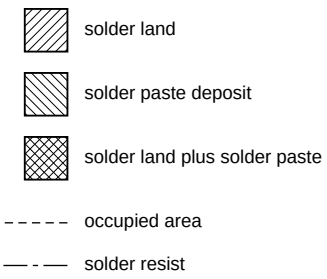
Fig 55. Reflow soldering of the LQFP100 package

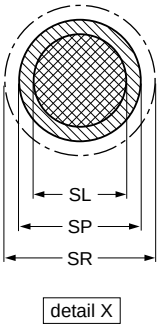
Footprint information for reflow soldering of TFBGA100 package **SOT926-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout





detail X

DIMENSIONS in mm

P	SL	SP	SR	Hx	Hy
0.80	0.330	0.400	0.480	9.400	9.400

sot926-1_fr

Fig 57. Reflow soldering of the TFBGA100 package

For more information, please visit: http://www.nxp.com
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