Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54606j512et100e

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54605J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54605J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54606J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54607J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J256BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54608J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54608J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54616J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54616J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54616J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54616J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54618J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54618J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54628J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3

3.1 Ordering options

Table 2. Ordering options

Type number	Package Name	Frequency/MHz	Flash/kB	SRAM/kB	FS USB	HS USB	Ethernet AVB	Classic CAN	CAN FD	LCD	Flexcomm Interface	EMC data bus width (bit)	GPIO	SHA
LPC54628 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD, SHA)														
LPC54628J512ET180	TFBGA180	220	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	yes
LPC54618 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0, LCD)														
LPC54618J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16	145	no
LPC54618J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	yes	10	8/16/32	171	no
LPC54616 devices (HS/FS USB, Ethernet, CAN FD, CAN 2.0)														
LPC54616J256ET180	TFBGA180	180	256	136	yes	yes	yes	yes	yes	no	10	8/16	145	no
LPC54616J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	yes	no	10	8/16/32	171	no
LPC54616J512ET100	TFBGA100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54616J512BD100	LQFP100	180	512	200	yes	yes	yes	yes	yes	no	9	8/16	64	no
LPC54608 devices (HS/FS USB, Ethernet, CAN 2.0, LCD)														
LPC54608J512ET180	TFBGA180	180	512	200	yes	yes	yes	yes	no	yes	10	8/16	145	no
LPC54608J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	no	yes	10	8/16/32	171	no
LPC54607 devices (HS/FS USB, LCD)														
LPC54607J256ET180	TFBGA180	180	256	136	yes	yes	no	no	no	yes	10	8/16	145	no
LPC54607J512ET180	TFBGA180	180	512	200	yes	yes	no	no	no	yes	10	8/16	145	no
LPC54607J256BD208	LQFP208	180	256	136	yes	yes	no	no	no	yes	10	8/16/32	171	no
LPC54606 devices (HS/FS USB, Ethernet, CAN 2.0)														
LPC54606J256ET180	TFBGA180	180	256	136	yes	yes	yes	yes	no	no	10	8/16	145	no
LPC54606J512BD208	LQFP208	180	512	200	yes	yes	yes	yes	no	no	10	8/16/32	171	no
LPC54606J256ET100	TFBGA100	180	256	136	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J512ET100	TFBGA100	180	512	200	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J256BD100	LQFP100	180	256	136	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54606J512BD100	LQFP100	180	512	200	yes	yes	yes	yes	no	no	9	8/16	64	no
LPC54605 devices (HS/FS USB)														
LPC54605J256ET180	TFBGA180	180	256	136	yes	yes	no	no	no	no	10	8/16	145	no
LPC54605J512ET180	TFBGA180	180	512	200	yes	yes	no	no	no	no	10	8/16	145	no
LPC54605J256BD100	LQFP100	180	256	136	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J512BD100	LQFP100	180	512	200	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J256ET100	TFBGA100	180	256	136	yes	yes	no	no	no	no	9	8/16	64	no
LPC54605J512ET100	TFBGA100	180	512	200	yes	yes	no	no	no	no	9	8/16	64	no

- yyww: Date code with yy = year and ww = week.
- xR = Boot code version and device revision.

Table 3. Device revision table

Revision identifier (R)	Revision description
1A	Initial device revision with Boot ROM version 19.1

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_30	A2	A2	200	95	[2]	PU	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.
PIO1_1	J10	K12	109	55	[2]	PU	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_2	G9	L14	117	58	[2]	PU	I/O	**PIO1_2 —** General-purpose digital input/output pin.
							O	**CAN0_TD —** Transmitter output for CAN0.
								R — Reserved.
							O	**CT0_MAT3 —** Match output 3 from Timer0.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
								R — Reserved.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_3	F10	J13	120	60	[2]	PU	I/O	**PIO1_3 —** General-purpose digital input/output pin.
							I	**CAN0_RD —** Receiver input for CAN0.
								R — Reserved.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
PIO1_4	C3	D4	3	3	[2]	PU	I/O	**PIO1_4 —** General-purpose digital input/output pin.
							I/O	**FC0_SCK —** Flexcomm 0: USART or SPI clock.
							I/O	**SD_D[0] —** SD/MMC data 0.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
							I/O	**EMC_D[11]) —** External Memory interface data [11].
PIO1_5	C2	E4	5	4	[2]	PU	I/O	**PIO1_5 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[4] —** External memory interface address 4.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_14	A9	C12	160	78	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B5	B7	187	88	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
								R — Reserved.
							O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	H8	N12	98	47	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_1	-	D11	159	-	[2]	PU	I/O	**PIO3_1 —** General-purpose digital input/output pin.
							O	**LCD_VD[15] —** LCD Data [15].
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO3_2	-	C10	164	-	[2]	PU	I/O	**PIO3_2 —** General-purpose digital input/output pin.
							O	**LCD_VD[16] —** LCD Data [16].
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO3_3	-	A13	169	-	[2]	PU	I/O	**PIO3_3 —** General-purpose digital input/output pin.
							O	**LCD_VD[17] —** LCD Data [17].
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO3_4	-	B11	172	-	[2]	PU	I/O	**PIO3_4 —** General-purpose digital input/output pin.
							O	**LCD_VD[18] —** LCD Data [18].
								R — Reserved.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT4_CAP1 —** Capture input 4 to Timer 1.
PIO3_5	-	B10	177	-	[2]	PU	I/O	**PIO3_5 —** General-purpose digital input/output pin.
							O	**LCD_VD[19] —** LCD Data [19].
								R — Reserved.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
PIO3_6	-	C9	180	-	[2]	PU	I/O	**PIO3_6 —** General-purpose digital input/output pin.
							O	**LCD_VD[20] —** LCD Data [20].
							O	**LCD_VD[0] —** LCD Data [0].
								R — Reserved.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
PIO3_7	-	B8	184	-	[2]	PU	I/O	**PIO3_7 —** General-purpose digital input/output pin.
							O	**LCD_VD[21] —** LCD Data [21].
							O	**LCD_VD[1] —** LCD Data [1].
								R — Reserved.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.

7.5 Nested Vectored Interrupt Controller (NVIC) for Cortex-M4

The NVIC is an integral part of the Cortex-M4. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- Supports up to 54 vectored interrupts.
- Eight programmable interrupt priority levels, with hardware priority level masking.
- Relocatable vector table.
- Non-Maskable Interrupt (NMI).
- Software interrupt generation.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags.

7.6 System Tick timer (SysTick)

The ARM Cortex-M4 includes a system tick timer (SysTick) that is intended to generate a dedicated SYSTICK exception. The clock source for the SysTick can be the FRO or the Cortex-M4 core clock.

7.7 On-chip static RAM

The LPC546xx support 200 kB SRAM with separate bus master access for higher throughput and individual power control for low-power operation.

7.8 On-chip flash

The LPC546xx supports up to 512 kB of on-chip flash memory.

7.9 On-chip ROM

The 64 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- Flash In-Application Programming (IAP) and In-System Programming (ISP).
- ROM-based USB drivers (HID, CDC, MSC, and DFU). Supports flash updates via USB.
- Supports booting from valid user code in flash, USART, SPI, and I2C.
- Legacy, Single, and Dual image boot.
- OTP API for programming OTP memory.
- Random Number Generator (RNG) API.

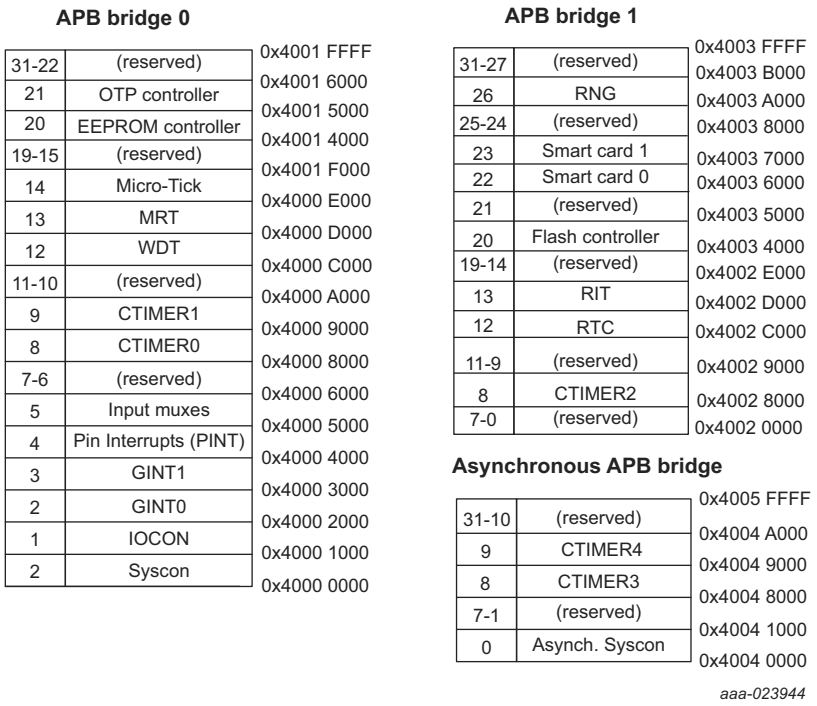

Fig 10. LPC546xx APB Memory map

7.12 System control

7.12.1 Clock sources

The LPC546xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.12.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.12.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

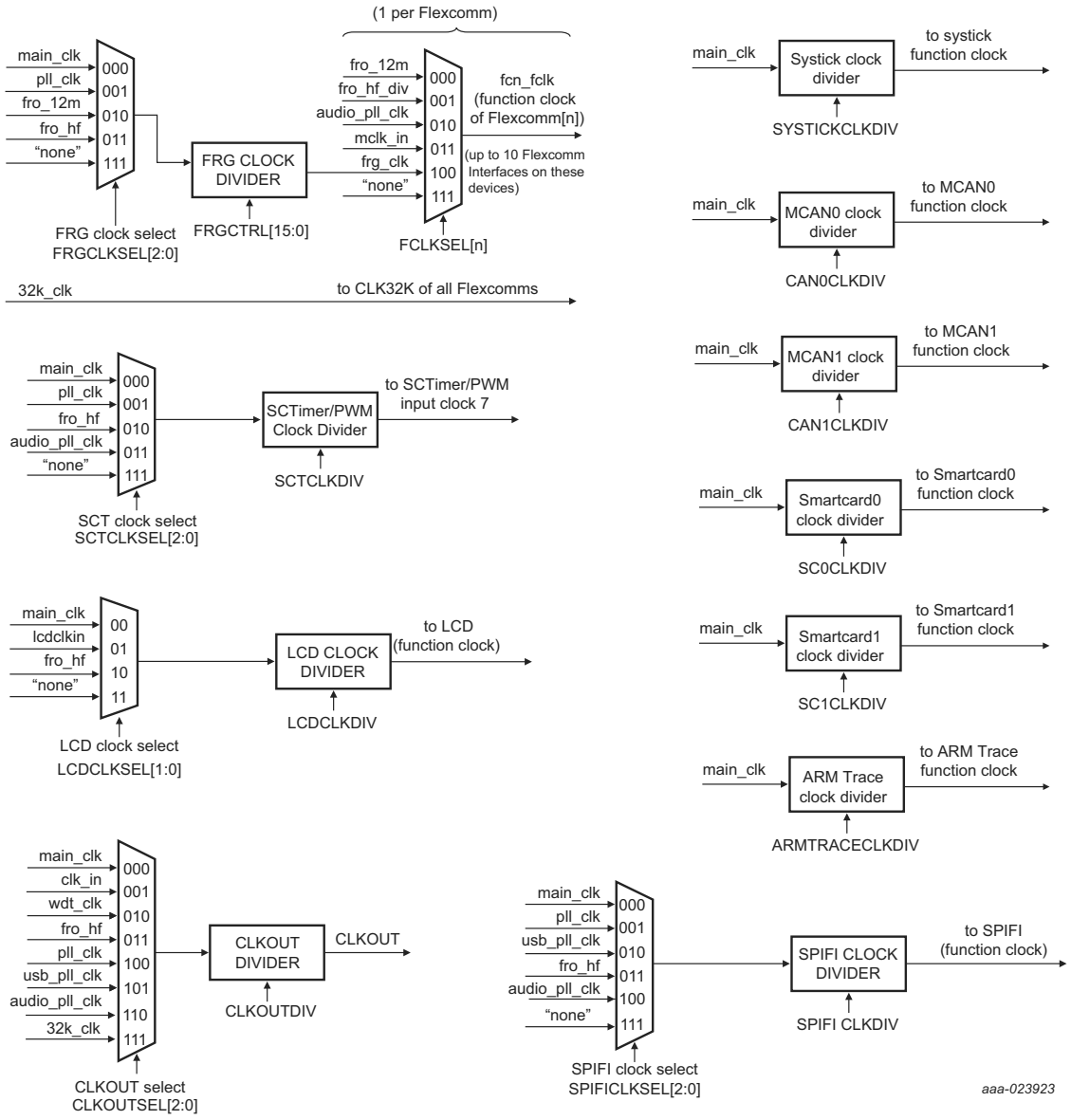

Fig 12. LPC546xx clock generation (continued)

7.12.6 Brownout detection

The LPC546xx includes a monitor for the voltage level on the V_{DD} pin. If this voltage falls below a fixed level, the BOD sets a flag that can be polled or cause an interrupt. In addition, a separate threshold level can be selected to cause chip reset.

7.12.7 Safety

The LPC546xx includes a Windowed WatchDog Timer (WWDT), which can be enabled by software after reset. Once enabled, the WWDT remains locked and cannot be modified in any way until a reset occurs.

- Supports DMA access.
- Provides XIP (execute in place) feature to execute code directly from serial flash.

7.17.5 CAN Flexible Data (CAN FD) interface

The LPC546xx contains two CAN FD interfaces, CAN FD 1 and CAN FD 2.

7.17.5.1 Features

- Conforms with CAN protocol version 2.0 part A, B and ISO 11898-1.
- CAN FD with up to 64 data bytes supported.
- CAN Error Logging.
- AUTOSAR support.
- SAE J1939 support.
- Improved acceptance filtering.

7.17.6 DMIC subsystem

7.17.6.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

7.17.7 Smart card interface

7.17.7.1 Features

- Two DMA supported ISO 7816 Smart Card Interfaces.
- Both asynchronous protocols, T = 0 and T = 1 are supported.

7.17.8 Flexcomm Interface serial communication

7.17.8.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.

- 8 inputs
- 10 outputs
- 10 match/capture registers
- 10 events
- 10 states

- PWM capabilities including dead time and emergency abort functions

7.19.3 Windowed WatchDog Timer (WWDT)

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.19.3.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) uses the WDOSC as the clock source.

7.19.4 Real Time Clock (RTC) timer

The RTC timer is a 32-bit timer which counts down from a preset value to zero. At zero, the preset value is reloaded and the counter continues. The RTC timer uses the 32.768 kHz clock input to create a 1 Hz or 1 kHz clock.

7.19.5 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.19.5.1 Features

- 24-bit interrupt timer.
- Four channels independently counting down from individually set values.
- Repeat and one-shot interrupt modes.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP208 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	33 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		16 ± 15 %	°C/W
LQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	48 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	65 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		19 ± 15 %	°C/W
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W
TFBGA100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	69 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	60 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		10 ± 15 %	°C/W

10. Static characteristics

10.1 General operating conditions

Table 12. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	CPU clock frequency		[3]	-	-	220	MHz
	CPU clock frequency	For USB high-speed device and host operations	[3]	60	-	220	MHz
	CPU clock frequency	For USB full-speed device and host operations	[3]	12	-	220	MHz
		For OTP programming only		-	-	12	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For OTP programming only	[2]	2.7	-	3.6	V
		For USB operation only		3.0	-	3.6	V
V_{DDA}	analog supply voltage			1.71	-	3.6	V
V_{BAT}	battery supply voltage			1.71	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
T_{amb}	Temperature	For EEPROM operation		−40.0	-	+85	°C
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		-0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		-0.5	-	+3.6	V
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	-	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	-	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Attempting to program below 2.7 V will result in unpredictable results and the part might enter an unrecoverable state.

[3] The LPC5460x/61x operates at CPU frequencies of up to 180 MHz. The LPC54628 operates at CPU frequencies of up to 220 MHz.

10.2 Power-up ramp conditions

Table 13. Power-up characteristics[1]

T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1 < V_{DD} < V_2$)		-	-	170	µs
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.62	V

[1] Assert the external reset pin until V_{DD} is > 1.62 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

[3] Tested in production. VDD = 1.71 V. At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage.

Table 17. Static characteristics: Power consumption in deep-sleep and deep power-down modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode; Flash is powered down					
		SRAMX (32 KB) powered T_{amb} = 25 °C		-	23	69	μA
		SRAMX (32 KB) powered T_{amb} = 105 °C		-	-	1150	μA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	464	1500	nA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	42	μA
		RTC oscillator running with external crystal VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	550	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] Tested in production, VDD = 3.6 V.

Table 18. Static characteristics: Power consumption in deep power-down mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
I_{BAT}	battery supply current	deep power-down mode; RTC oscillator running with external crystal					
		VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	0	-	nA
		VDD = VDDA= VREFP = 0 V or tied to ground, VBAT = 3.0 V		-	340[3]	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

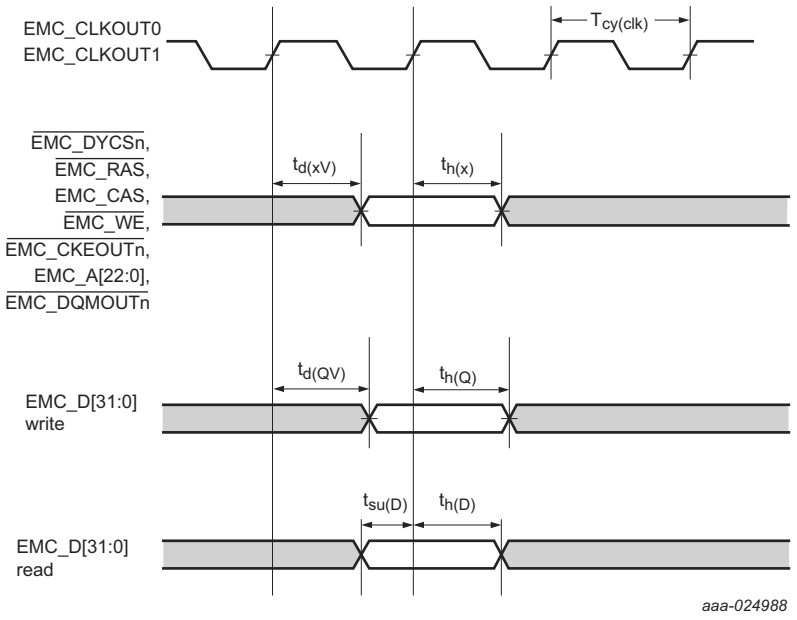

Fig 27. Dynamic external memory interface signal timing

Table 36. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 540$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.9 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 37. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.10 Crystal oscillator

Table 38. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

Table 38. Dynamic characteristic: oscillator *…continued*
T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
High-frequency mode (20 - 25 MHz)[5]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] Select Low Frequency range = 0 in the SYSOSCCTRL register.

[5] Select High Frequency = 1 in the SYSOSCCTRL register.

11.11 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to an external clock source.

Table 39. Dynamic characteristic: RTC oscillator
T_{amb} = −40 °C to +105 °C; 1.71 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.12 Watchdog oscillator

Table 40. Dynamic characteristics: Watchdog oscillator

T_{amb} = −40 °C to +105 °C; 1.71 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency		[2]	200	-	1500	kHz
D_{clkout}	clkout duty cycle			48	-	52	%
J_{PP-CC}	peak-peak period jitter		[3][4]	-	1	20	ns
t_{start}	start-up time		[4]	-	4	-	μs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.