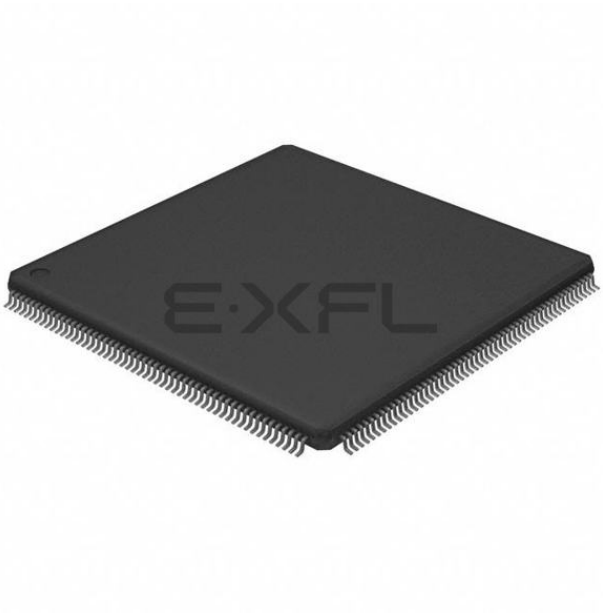

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	171
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54607j256bd208e

4. Marking

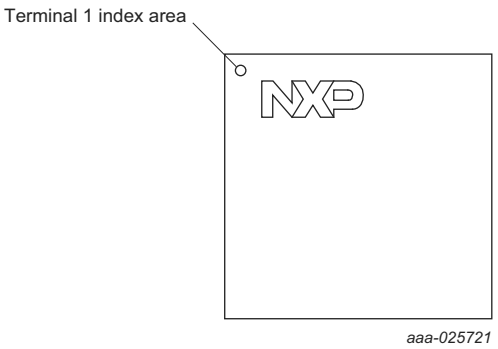


Fig 1. TFBGA180 and TFBGA100 package markings

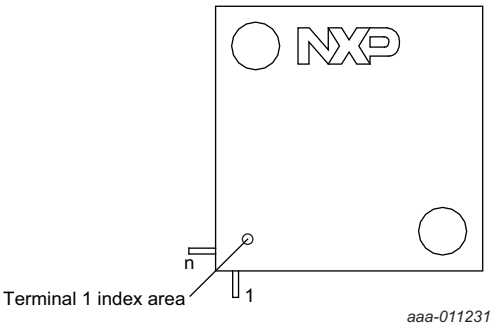


Fig 2. LQFP208 package marking

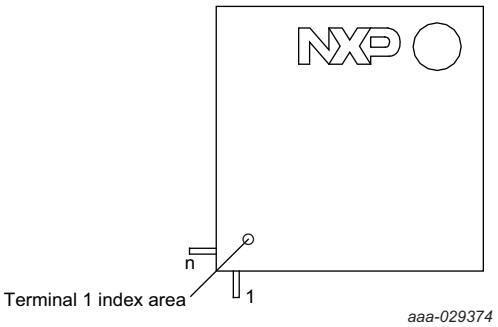


Fig 3. LQFP100 package marking

The LPC546xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC546xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_30	A2	A2	200	95	[2]	PU	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.
PIO1_1	J10	K12	109	55	[2]	PU	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_10	H6	N9	84	41	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
							O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	B4	198	94	[2][8]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
								R — Reserved.
							O	**EMC_CLK[0] —** External memory interface clock 0.
PIO1_12	F8	K9	128	62	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**EMC_DYCSN[0] —** External Memory interface SDRAM chip select 0 (active low).
PIO1_13	D10	G10	139	66	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							O	**EMC_DQM[0] —** External memory interface data mask 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_2	-	C3	4	-	[2]	PU	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	-	C1	12	-	[2]	PU	I/O	**PIO2_5 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	-	F3	17	-	[2]	PU	I/O	**PIO2_6 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	-	J2	29	-	[2]	PU	I/O	**PIO2_7 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_D(1) —** SD/MMC data 1.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_19	-	P12	93	-	[2]	PU	I/O	**PIO2_19 —** General-purpose digital input/output pin.
							O	**LCD_VD[1] —** LCD Data [1].
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
PIO2_20	-	P13	95	-	[2]	PU	I/O	**PIO2_20 —** General-purpose digital input/output pin.
							O	**LCD_VD[2] —** LCD Data [2].
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
PIO2_21	-	L10	99	-	[2]	PU	I/O	**PIO2_21 —** General-purpose digital input/output pin.
							O	**LCD_VD[3] —** LCD Data [3].
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	-	K10	113	-	[2]	PU	I/O	**PIO2_22 —** General-purpose digital input/output pin.
							O	**LCD_VD[4] —** LCD Data [4].
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
								R — Reserved.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
PIO2_23	-	M14	115	-	[2]	PU	I/O	**PIO2_23 —** General-purpose digital input/output pin.
							O	**LCD_VD[5] —** LCD Data [5].
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
PIO2_24	-	K14	118	-	[2]	PU	I/O	**PIO2_24 —** General-purpose digital input/output pin.
							O	**LCD_VD[6] —** LCD Data [6].
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
PIO2_25	-	J11	121	-	[2][8]	PU	I/O	**PIO2_25 —** General-purpose digital input/output pin.
							O	**LCD_VD[7] —** LCD Data [7].
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_26	-	H11	124	-	[2]	PU	I/O	**PIO2_26 —** General-purpose digital input/output pin.
							O	**LCD_VD[8] —** LCD Data [8].
								R — Reserved.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
PIO2_27	-	H14	130	-	[2]	PU	I/O	**PIO2_27 —** General-purpose digital input/output pin.
							O	**LCD_VD[9] —** LCD Data [9].
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
PIO2_28	-	G13	134	-	[2]	PU	I/O	**PIO2_28 —** General-purpose digital input/output pin.
							O	**LCD_VD[10]) —** LCD Data [10].
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
PIO2_29	-	G11	137	-	[2]	PU	I/O	**PIO2_29 —** General-purpose digital input/output pin.
							O	**LCD_VD[11] —** LCD Data [11].
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT2_CAP3 —** Capture 3 input to Timer 2.
							O	**CLKOUT —** Output of the CLKOUT function.
PIO2_30	-	F12	143	-	[2]	PU	I/O	**PIO2_30 —** General-purpose digital input/output pin.
							O	**LCD_VD[12] —** LCD Data [12].
								R — Reserved.
								R — Reserved.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
PIO2_31	-	D14	149	-	[2]	PU	I/O	**PIO2_31 —** General-purpose digital input/output pin.
							O	**LCD_VD[13] —** LCD Data [13].
PIO3_0	-	D12	155	-	[2]	PU	I/O	**PIO3_0 —** General-purpose digital input/output pin.
							O	**LCD_VD[14] —** LCD Data [14].
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_1	-	G14	132	-	[2]	PU	I/O	**PIO4_1 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	-	F14	138	-	[2]	PU	I/O	**PIO4_2 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	-	F13	140	-	[2]	PU	I/O	**PIO4_3 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	-	D9	147	-	[2]	PU	I/O	**PIO4_4 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

- Toggle on match.
- Do nothing on match.

- Up to two match registers can be used to generate timed DMA requests.
- The timer and prescaler may be configured to be cleared on a designated capture event. This feature permits easy pulse width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Up to four match registers can be configured for PWM operation, allowing up to three single edged controlled PWM outputs. (The number of match outputs for each timer that are actually available on device pins may vary by device.)

7.19.2 SCTimer/PWM

The SCTimer/PWM allows a wide variety of timing, counting, output modulation, and input capture operations. The inputs and outputs of the SCTimer/PWM are shared with the capture and match inputs/outputs of the 32-bit general-purpose counter/timers.

The SCTimer/PWM can be configured as two 16-bit counters or a unified 32-bit counter. In the two-counter case, in addition to the counter value the following operational elements are independent for each half:

- State variable.
- Limit, halt, stop, and start conditions.
- Values of Match/Capture registers, plus reload or capture control values.

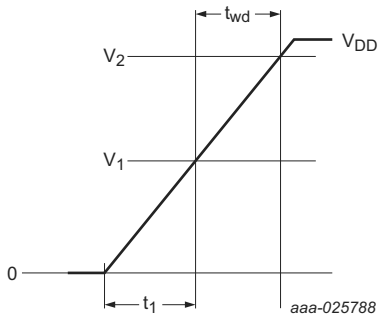
In the two-counter case, the following operational elements are global to the SCTimer/PWM, but the last three can use match conditions from either counter:

- Clock selection
- Inputs
- Events
- Outputs
- Interrupts

7.19.2.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counter(s) clocked by bus clock or selected input.
- Up counter(s) or up-down counter(s).
- State variable allows sequencing across multiple counter cycles.
- Event combines input or output condition and/or counter match in a specified state.
- Events control outputs, interrupts, and the SCTimer/PWM states.
  - Match register 0 can be used as an automatic limit.
  - In bi-directional mode, events can be enabled based on the count direction.
  - Match events can be held until another qualifying event occurs.
- Selected event(s) can limit, halt, start, or stop a counter.
- Supports:

[3] V_{DD} to stay below V_2 for the minimum duration of t_{wd}.



t_1: The time when there is no restriction on the ramp rate.

Fig 13. Power-up ramp

10.3 CoreMark data

Table 14. CoreMark score[1]

T_{amb} = 25 °C, V_{DD} = 3.3V

Parameter	Conditions		Typ	Unit
ARM Cortex-M4 in active mode				
CoreMark score	CoreMark code executed from SRAMX; CCLK = 12 MHz	[2][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 96 MHz	[2][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 180 MHz	[3][4][5][7][8]	3.38	Iterations/s/MHz
	CCLK = 220 MHz	[3][4][5][7][8]	3.38	Iterations/s/MHz
CoreMark score	CoreMark code executed from flash; CCLK = 12 MHz; 1 system clock flash access time.	[2][4][5][6][8]	3.38	Iterations/s/MHz
	CCLK = 96 MHz; 5 system clock flash access time.	[2][4][5][6][8]	2.59	Iterations/s/MHz
	CCLK = 180 MHz; 9 system clock flash access time.	[3][4][5][6][8]	1.99	Iterations/s/MHz
	CCLK = 220 MHz; 8 system clock flash access time.	[3][4][5][6][8][9]	2.11	Iterations/s/MHz
	CCLK = 220 MHz; 9 system clock flash access time.	[3][4][5][6][8]	1.99	Iterations/s/MHz

[1] Based on the power API library from the SDK software package available on nxp.com.

[2] Clock source FRO. PLL disabled.

[3] Clock source 12 MHz FRO. PLL enabled.

[4] Characterized through bench measurements using typical samples.

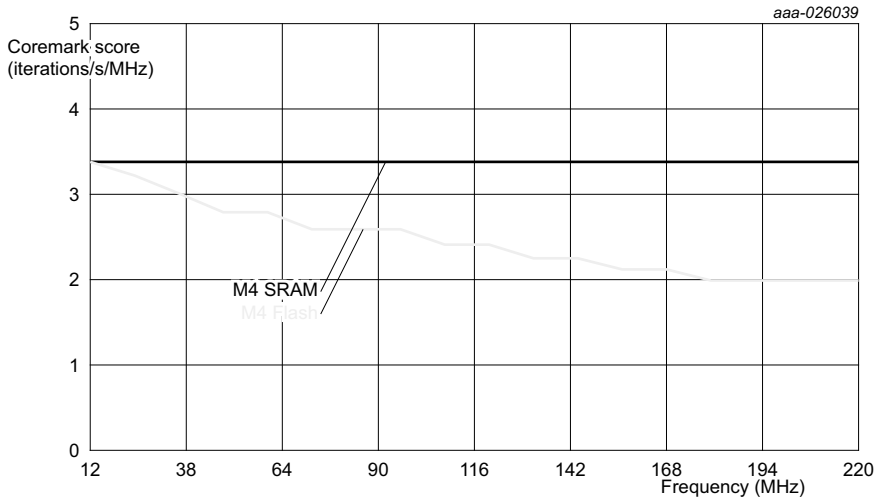
[5] Compiler settings: IAR C/C++ Compiler for Arm ver 8.22.2, optimization level 3, optimized for time on.

[6] See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASHCFG register is set to 1.

[7] Flash is powered down

[8] SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.

[9] At 220 MHz the minimum system clock/access time can be lower when compared to 180 MHz because the power library optimizes the on-chip voltage regulator.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASCFG register is set to 1. Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON. Coremark score is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark score from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark score from SRAMX: SRAM0 is powered; flash is powered down.

Fig 14. Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX

Table 21. Static characteristics: pin characteristics *…continued*

T_{amb} = −40 °C to +105 °C, unless otherwise specified. 1.71 V ≤ V_{DD} ≤ 3.6 V unless otherwise specified. Values tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	V_{DD}	V
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; on-chip pull-up/pull-down resistors disabled		-	3	180	nA
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; 1.71 V ≤ V_{DD} < 2.7 V		V_{DD} − 0.4	-	-	V
		I_{OH} = −6 mA; 2.7 V ≤ V_{DD} ≤ 3.6 V		V_{DD} − 0.4			
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; 1.71 V ≤ V_{DD} < 2.7 V		-	-	0.4	V
		I_{OL} = 6 mA; 2.7 V ≤ V_{DD} ≤3.6 V		-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = V_{DD} − 0.4 V; 1.71 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OH} = V_{DD} − 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; 1.71 V ≤ V_{DD} < 2.7 V		4.0	-	-	mA
		V_{OL} = 0.4 V; 2.7 V ≤ V_{DD} ≤ 3.6 V		6.0	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	1.71 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	35	mA
	drive HIGH; connected to ground;	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	87	mA
I_{OLS}	LOW-level short-circuit output current	1.71 V ≤ V_{DD} < 2.7 V	[2][4]	-	-	30	mA
	drive LOW; connected to V_{DD}	2.7 V ≤ V_{DD} ≤ 3.6 V		-	-	77	mA
Weak input pull-up/pull-down characteristics							
I_{pd}	pull-down current	V_I = V_{DD}		25		80	µA
		V_I = 5 V	[2]	80		100	µA
I_{pu}	pull-up current	V_I = 0 V		−25		−80	µA
		V_{DD} < V_I < 5 V	[2][7]	6		30	µA
Open-drain I^2C pins							
V_{IH}	HIGH-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		0.7 × V_{DD}	-	-	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0.7 × V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	1.71 V ≤ V_{DD} < 2.7 V		0	-	0.3 × V_{DD}	V
		2.7 V ≤ V_{DD} ≤ 3.6 V		0	-	0.3 × V_{DD}	V
V_{hys}	hysteresis voltage			0.1 × V_{DD}	-	-	V
I_{LI}	input leakage current	V_I = V_{DD}	[5]	-	2.5	3.5	µA
		V_I = 5 V		-	5.5	10	µA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; pin configured for standard mode or fast mode		4.0	-	-	mA
		V_{OL} = 0.4V; pin configured for Fast-mode Plus		20	-	-	mA

11. Dynamic characteristics

11.1 Flash memory

Table 22. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	sector erase/program	[1]	10000	-	-	cycles
		page erase/program; page in a sector		1000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[2]	-	1	-	ms

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

11.2 EEPROM

Table 23. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			800	1500	1600	kHz
N_{endu}	endurance			100000	-	-	cycles
t_{ret}	retention time	T_{amb} = −40 °C to +85 °C		20	-	-	years
t_a	access time	read		-	100	-	ns
		erase/program; f_{clk} = 1500 kHz		-	1.99	-	ms
		erase/program; f_{clk} = 1600 kHz		-	1.87	-	ms
t_{wait}	wait time	read; RPHASE1	[1]	70	-	-	ns
		read; RPHASE2	[1]	35	-	-	ns
		write; PHASE1	[1]	20	-	-	ns
		write; PHASE2	[1]	40	-	-	ns
		write; PHASE3	[1]	10	-	-	ns

[1] See the LPC546xx. user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).

Remark: EEPROM is not accessible in deep-sleep and deep power-down modes

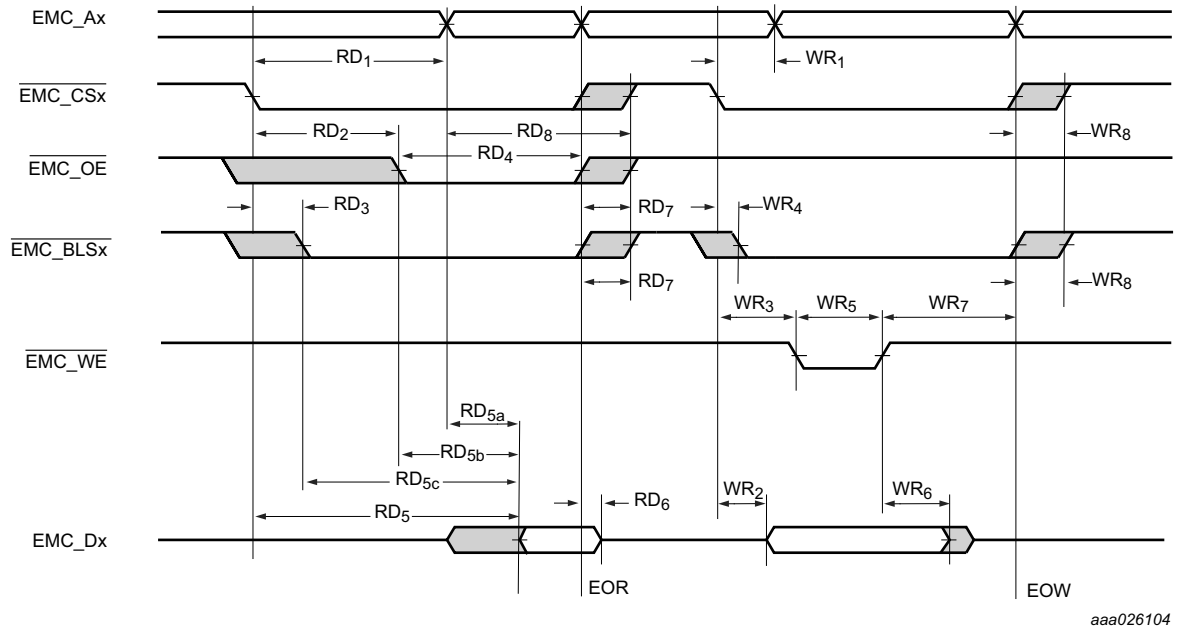


Fig 25. External static memory read/write access (PB =1)

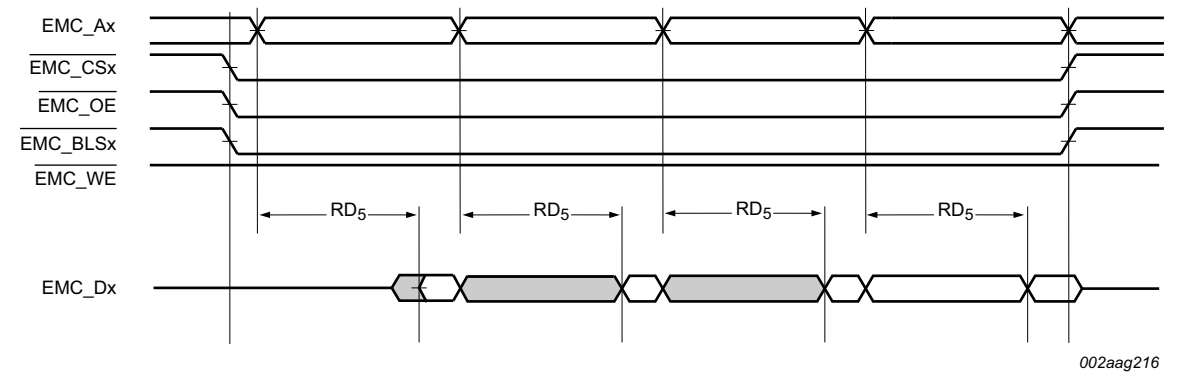


Fig 26. External static memory burst read cycle

Table 36. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 540$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.9 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 37. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.10 Crystal oscillator

Table 38. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

11.15 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 14 Mbit/s.

Table 43. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		6.3	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		6.7	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		2.6	-	5.0	ns
		100 MHz < CCLK ≤ 180 MHz		0.3	-	4.7	ns
SPI slave 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		2.2	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		18.8	-	37.0	ns
		100 MHz < CCLK ≤ 180 MHz		18.0	-	36.0	ns
SPI master 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		2.2	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		4.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.5	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		1.8	-	4.6	ns
		100 MHz < CCLK ≤ 180 MHz		1.7	-	4.0	ns
SPI slave 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.0	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		14	-	23.9	ns
		100 MHz < CCLK ≤ 180 MHz		13.3	-	22.2	ns

[1] Based on characterization; not tested in production.

11.16 SPIFI

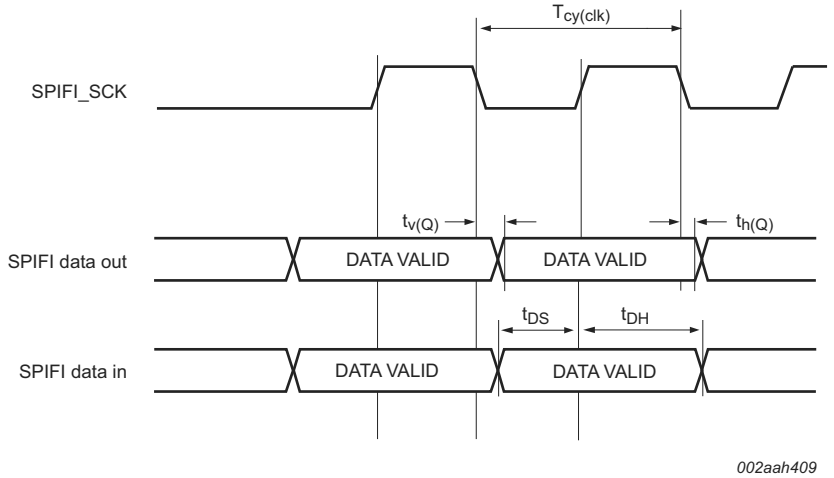
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 44. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge. Maximum SPIFI clock = 100 MHZ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		100 MHz < CCLK ≤ 180 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		100 MHz < CCLK ≤ 180 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 33. SPIFI control register (Mode 0)

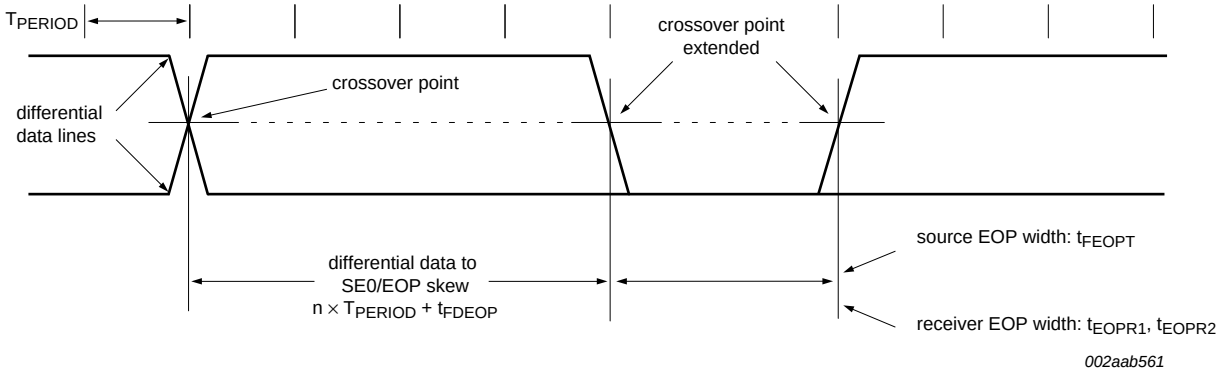


Fig 36. Differential data-to-EOP transition skew and EOP width

11.23 Ethernet AVB

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

Table 50. Dynamic characteristics: Ethernet

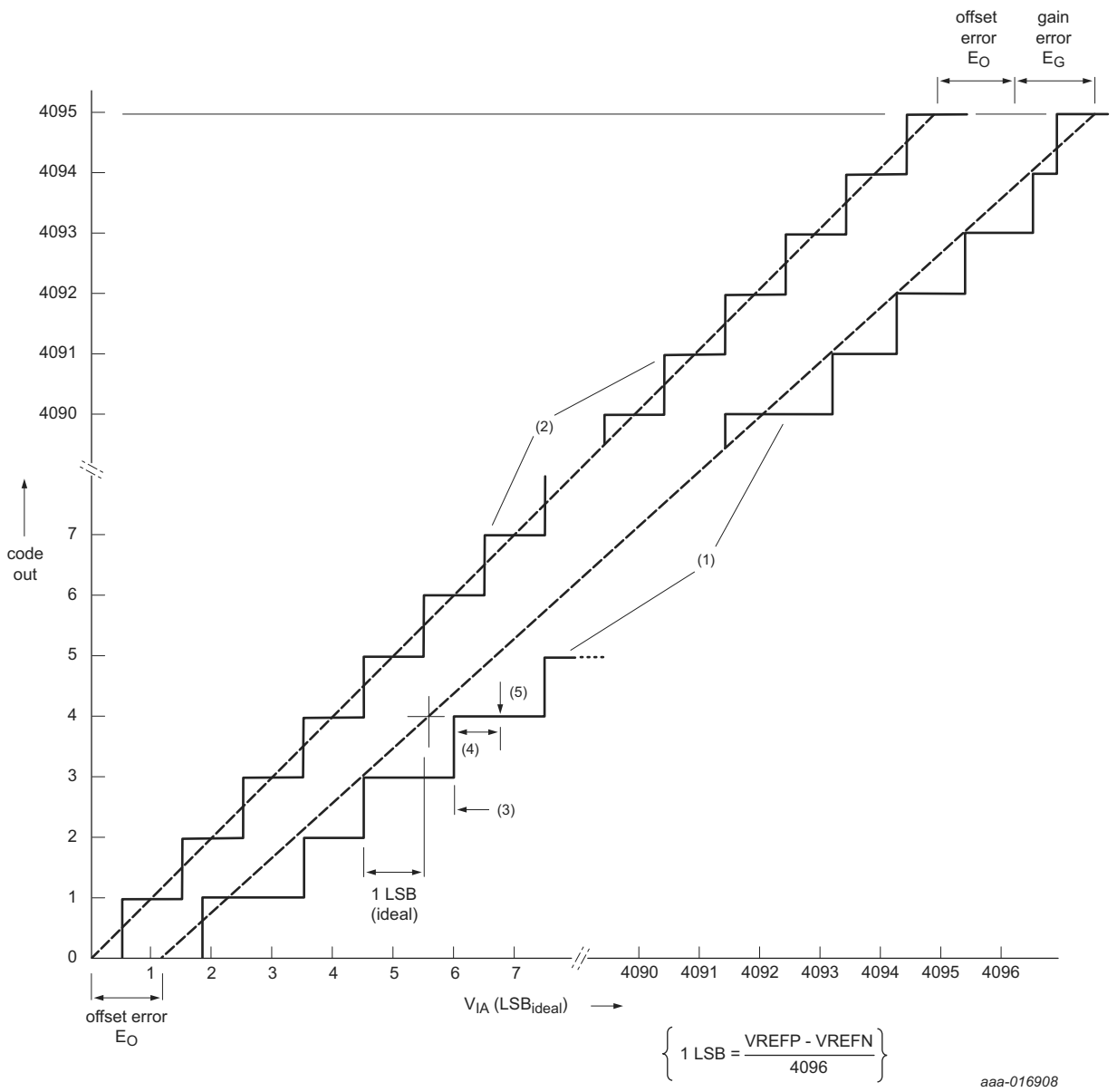
T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Based on simulation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RMII mode							
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	50.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.4	-	-	ns
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.3	-	0	ns
		100 MHz < CCLK ≤ 180 MHz		−1.3	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN	[1][2]				
		CCLK ≤ 100 MHz		9.9	-	17.3	ns
		100 MHz < CCLK ≤ 180 MHz		9.9	-	17.3	ns
MII mode							
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.7	-	-	ns

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 40.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 21 for C_{io}. See Figure 41.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

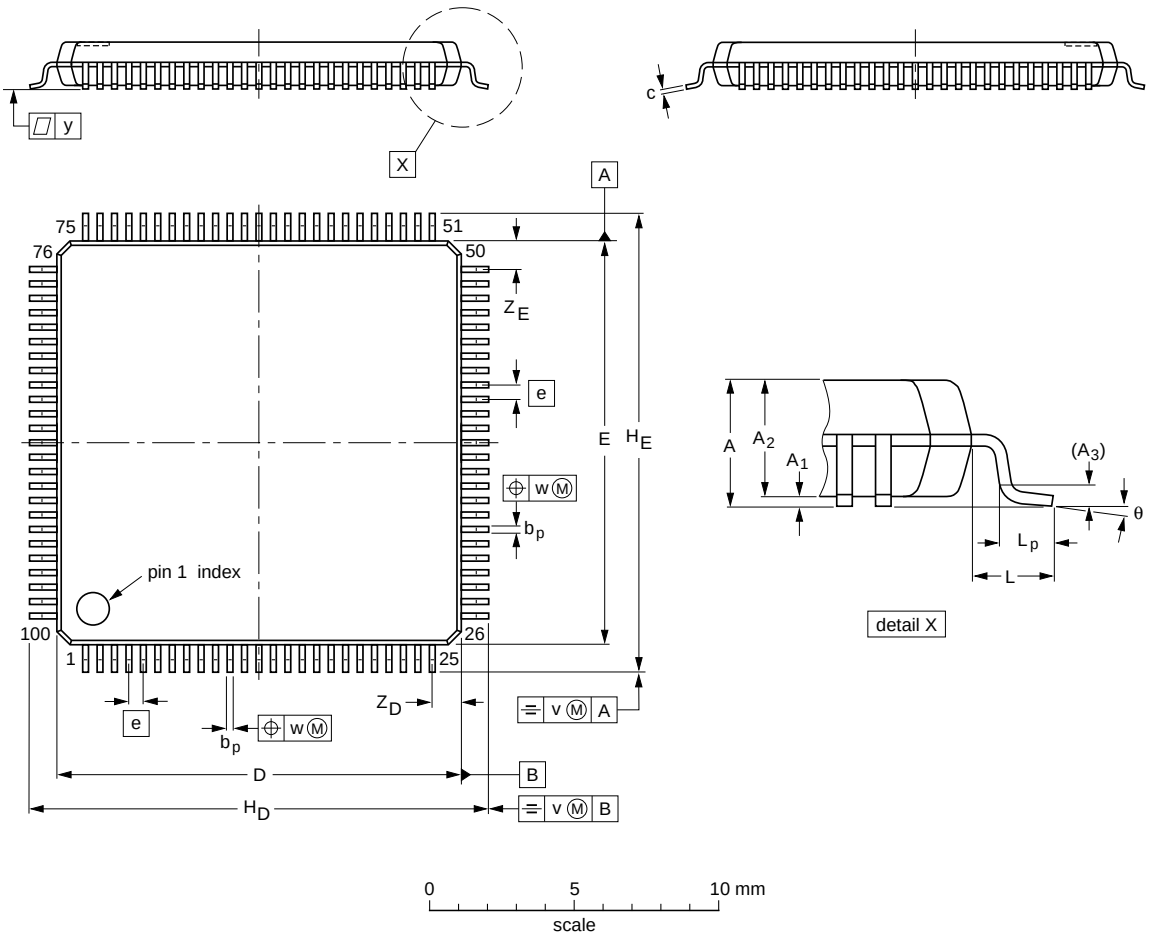
(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 40. 12-bit ADC characteristics

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1	0.75 0.45	0.2	0.08	0.08	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT407-1	136E20	MS-026				~~00-02-01~~ 03-02-20

Fig 51. LQFP100 package

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• Regrouped Table 2 “Ordering options”. • Added text to Section 7.15.3.1 “Features”: Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details. • Removed Table note 2: fclk = cclk/CLKDIV +1. See LPC5460x UM10912 and updated Table note 1 “See the LPC5460x user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).”of Section 11.2 “EEPROM”. • Updated Table 50 “Dynamic characteristics: SD/MMC and SDIO”: changed the maximum clock frequency to 52 MHz. • Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”:			
LPC5460x v.1	20161215	Product data sheet	-	-