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Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54607j256et180e

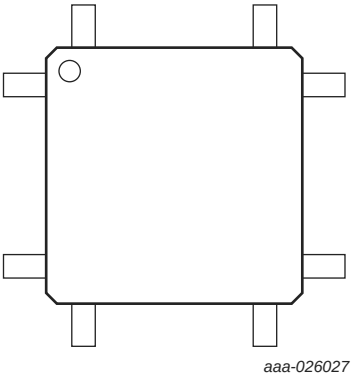


Fig 7. LQFP 208 Pin configuration

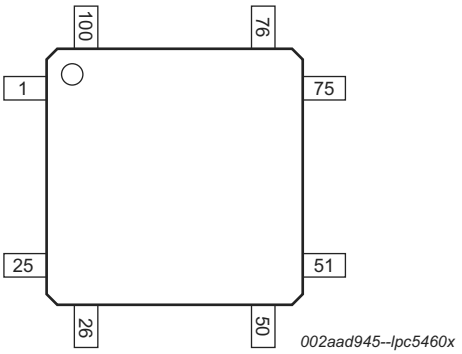


Fig 8. LQFP 100 Pin configuration

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_10	H6	N9	84	41	[2]	PU	I/O	**PIO1_10 —** General-purpose digital input/output pin.
							O	**ENET_TXD1 —** Ethernet transmit data 1.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
							O	**EMC_RASN —** External memory interface row address strobe (active low).
PIO1_11	B4	B4	198	94	[2][8]	PU	I/O	**PIO1_11 —** General-purpose digital input/output pin.
							O	**ENET_TX_EN —** Ethernet transmit enable (RMII/MII interface).
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
								R — Reserved.
							O	**EMC_CLK[0] —** External memory interface clock 0.
PIO1_12	F8	K9	128	62	[2]	PU	I/O	**PIO1_12 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**EMC_DYCSN[0] —** External Memory interface SDRAM chip select 0 (active low).
PIO1_13	D10	G10	139	66	[2]	PU	I/O	**PIO1_13 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							O	**EMC_DQM[0] —** External memory interface data mask 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_14	A9	C12	160	78	[2]	PU	I/O	**PIO1_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							O	**EMC_DQM[1] —** External memory interface data mask 0.
PIO1_15	C7	A11	176	84	[2]	PU	I/O	**PIO1_15 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							O	**EMC_CKE[0] —** External memory interface SDRAM clock enable 0.
PIO1_16	B5	B7	187	88	[2]	PU	I/O	**PIO1_16 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
								R — Reserved.
							O	**EMC_A[10] —** External memory interface address 10.
PIO1_17	H8	N12	98	47	[2]	PU	I/O	**PIO1_17 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							O	**EMC_BLSN[0] —** External memory interface byte lane select 0 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_22	K8	P11	89	43	[2]	PU	I/O	**PIO1_22 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**EMC_CKE[1] —** External memory interface SDRAM clock enable 1.
PIO1_23	K10	M10	97	46	[2]	PU	I/O	**PIO1_23 —** General-purpose digital input/output pin.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**EMC_A[11] —** External memory interface address 11.
PIO1_24	G8	N14	111	57	[2]	PU	I/O	**PIO1_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
								R — Reserved.
								R — Reserved.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	G10	M12	119	59	[2]	PU	I/O	**PIO1_25 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_A[13] —** External memory interface address 13.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_14	-	L7	77	-	[2][8]	PU	I/O	**PIO2_14 —** General-purpose digital input/output pin.
							O	**LCD_FP —** LCD frame pulse (STN). Vertical synchronization pulse (TFT).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
PIO2_15	-	M8	79	-	[2]	PU	I/O	**PIO2_15 —** General-purpose digital input/output pin.
							O	**LCD_AC —** LCD STN AC bias drive or TFT data enable output.
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**CT0_MAT3 —** Match output 3 from Timer 0.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
PIO2_16	-	L8	81	-	[2][8]	PU	I/O	**PIO2_16 —** General-purpose digital input/output pin.
							O	**LCD_LP —** LCD line synchronization pulse (STN). Horizontal synchronization pulse (TFT).
							O	**USB1_FRAME —** USB1 frame toggle signal.
							O	**USB1_PORTPWRN —** USB1 VBUS drive indicator (Indicates VBUS must be driven).
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
PIO2_17	-	P10	86	-	[2]	PU	I/O	**PIO2_17 —** General-purpose digital input/output pin.
							I	**LCD_CLKIN —** LCD clock input.
							O	**USB1_LEDN —** USB1-configured LED indicator (active low).
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).
							I	**CT1_CAP1 —** Capture 1 input to Timer 1.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO2_18	-	N10	90	-	[2]	PU	I/O	**PIO2_18 —** General-purpose digital input/output pin.
							O	**LCD_VD[0] —** LCD Data [0].
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_31	-	-	114	-	[2]	PU	I/O	**PIO4_31 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
							I/O	**EMC_D[26] —** External Memory interface data [26].
PIO5_0	-	-	122	-	[2]	PU	I/O	**PIO5_0 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I/O	**EMC_D[27] —** External Memory interface data [27].
PIO5_1	-	-	126	-	[2]	PU	I/O	**PIO5_1 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**EMC_D[28] —** External Memory interface data [28].
PIO5_2	-	-	202	-	[2]	PU	I/O	**PIO5_2 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I/O	**EMC_D[29] —** External Memory interface data [29].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
USB1_AVDDC3V3	E1	G3	24	10				USB1 analog 3.3 V supply.
USB1_AVDDTX3V3	E2	H1	25	11				USB1 analog 3.3 V supply for line drivers.
USB1_DP	F2	H3	27	13	[6]		I/O	USB1 bidirectional D+ line.
USB1_DM	E3	H2	26	12	[6]		I/O	USB1 bidirectional D- line.
USB1_AVSSTX3V3	G1	J1	28	14				USB1 analog ground for line drivers.
USB0_DP	B3	E5	204	97	[6]		I/O	USB0 bidirectional D+ line.
USB0_DM	B2	D5	205	98	[6]		I/O	USB0 bidirectional D- line.
RESETN	J8	N13	101	48	[5]			External reset input: A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and the boot code to execute. Wakes up the part from deep power-down mode.
VDD	D5; D7; E4; E6; F5; F7; G4; G6	E6; E8; F5; G5; J12; L6; L11	1; 48; 65; 104; 108; 156; 157; 206	1; 21; 33; 50; 54; 75; 76; 99		-	-	Single 1.71 V to 3.6 V power supply powers internal digital functions and I/Os.
VSS	D4; D6; E5; E7; F4; F6; G5; G7	B3; D7; D8; E11; H5; J5; K7	2; 49; 66; 103; 107; 148; 162; 201	2; 22; 34; 49; 53; 71; 79; 96		-	-	Ground.
VDDA	J4	N6	64	32		-	-	Analog supply voltage.
VREFN	-	N4	59	-		-	-	ADC negative reference voltage. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
VREFP	K4	P6	63	31		-	-	ADC positive reference voltage.
VSSA	H4	L5	60	30		-	-	Analog ground. On TFBGA100 and LQFP100 packages, the ADC negative reference voltage is internally tied to the VSSA pin.
XTALIN	H2	K4	41	20	[7]	-	-	Main oscillator input.
XTALOUT	G3	J4	40	19	[7]	-	-	Main oscillator output.
VBAT	K9	N11	94	45		-	-	Battery supply voltage. If no battery is used, tie VBAT to VDD or to ground.
RTCXIN	J9	L12	105	51		-	-	RTC oscillator input.
RTCXOUT	H9	K11	106	52		-	-	RTC oscillator output.

7.18.4 DMA controller

The DMA controller allows peripheral-to memory, memory-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional DMA transfers for a single source and destination.

7.18.4.1 Features

- One channel per on-chip peripheral direction: typically one for input and one for output for most peripherals.
- DMA operations can optionally be triggered by on- or off-chip events.
- Priority is user selectable for each channel.
- Continuous priority arbitration.
- Address cache.
- Efficient use of data bus.
- Supports single transfers up to 1,024 words.
- Address increment options allow packing and/or unpacking data.

7.19 Counter/timers

7.19.1 General-purpose 32-bit timers/external event counter

The LPC546xx includes five general-purpose 32-bit timer/counters.

The timer/counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts, generate timed DMA requests, or perform other actions at specified timer values, based on four match registers. Each timer/counter also includes two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.19.1.1 Features

- A 32-bit timer/counter with a programmable 32-bit prescaler.
- Counter or timer operation.
- Up to four 32-bit captures can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt. The number of capture inputs for each timer that are actually available on device pins may vary by device.
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
  - Shadow registers are added for glitch-free PWM output.
- For each timer, up to four external outputs corresponding to match registers with the following capabilities (the number of match outputs for each timer that are actually available on device pins may vary by device):
  - Set LOW on match.
  - Set HIGH on match.

7.21 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.21.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.22 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.23 Security features

The OTP memory contains a memory bank of 128 bits each. OTP bank contains 4 words: word 0 for ECRP, word 1 is reserved, words 2 and 3 can be used by user application for storing application specific options.

7.23.1 Features

- OTP memory.
- Random number generator (RNG).

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

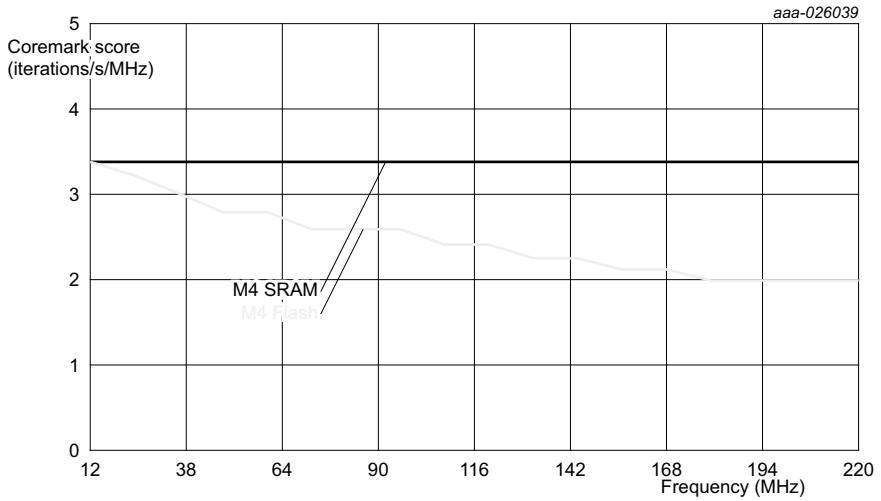
$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

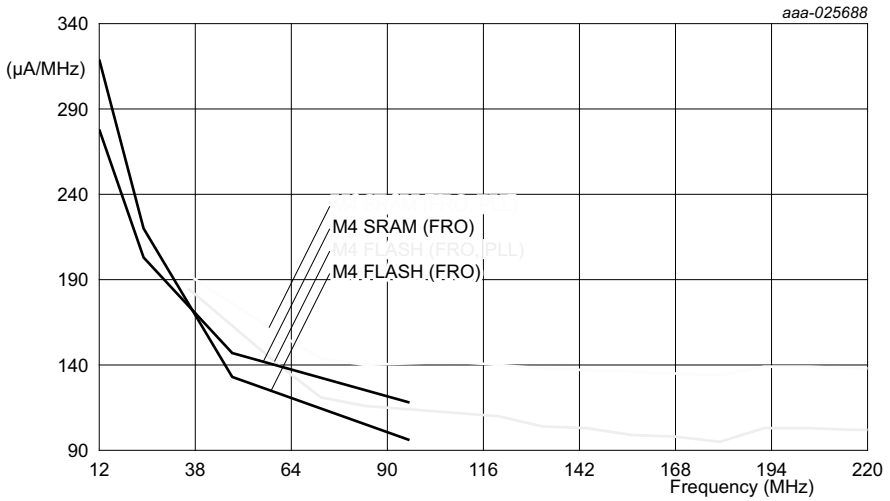
Symbol	Parameter	Conditions	Max/Min	Unit
LQFP208 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	33 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		16 ± 15 %	°C/W
LQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	48 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	65 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		19 ± 15 %	°C/W
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W
TFBGA100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	69 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	60 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		10 ± 15 %	°C/W



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASCFG register is set to 1. Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON. Coremark score is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark score from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark score from SRAMX: SRAM0 is powered; flash is powered down.

Fig 14. Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; Acceleration enable bit in the FLASHCFG register is set to 0. See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Measured with Keil uVision v.5.21. Optimization level 0, optimized for time off. Coremark power consumption is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark µA/MHz from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark µA/MHz from SRAMX: SRAM0 is powered; flash is powered down.

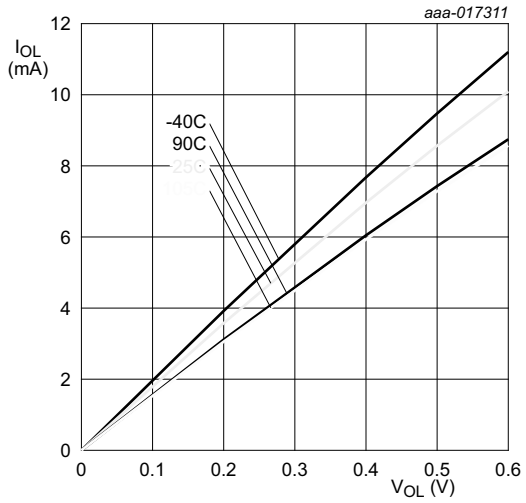
Fig 15. CoreMark power consumption: typical µA/MHz vs. frequency (MHz) from flash and SRAMX

Table 16. Static characteristics: Power consumption in deep-sleep and deep power-down modes
T_{amb} = −40 °C to +105 °C, unless otherwise specified, 1.71 V ≤ V_{DD} ≤ 2.7 V.

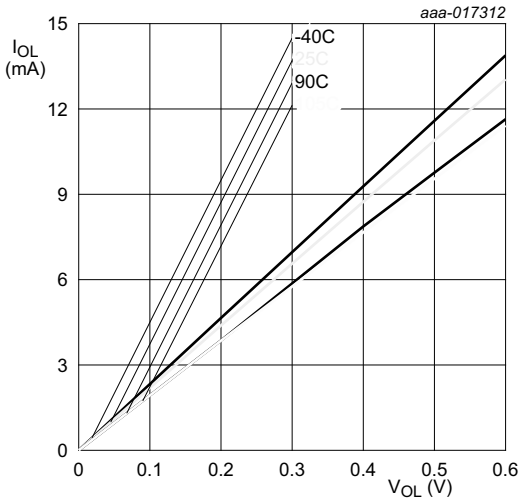
Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode; Flash is powered down					
		SRAMX (32 KB) powered T_{amb} = 25 °C		-	22	69	µA
		SRAMX (32 KB) powered T_{amb} = 105 °C		-	-	1150	µA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	326	1000	nA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	27	µA
		RTC oscillator running with external crystal VDD = VDDA = VREFP = VBAT = 1.8 V		-	340	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 1.8 V.

[2] Characterized through bench measurements using typical samples.

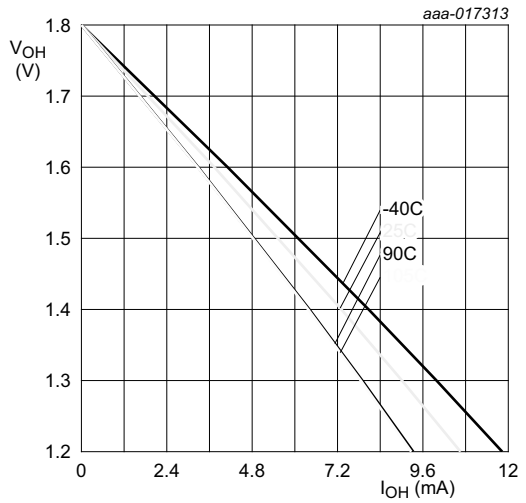


Conditions: V_{DD} = 1.8 V; on standard port pins.

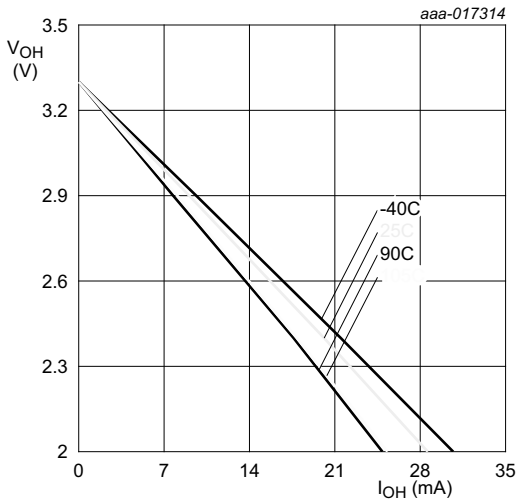


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 20. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

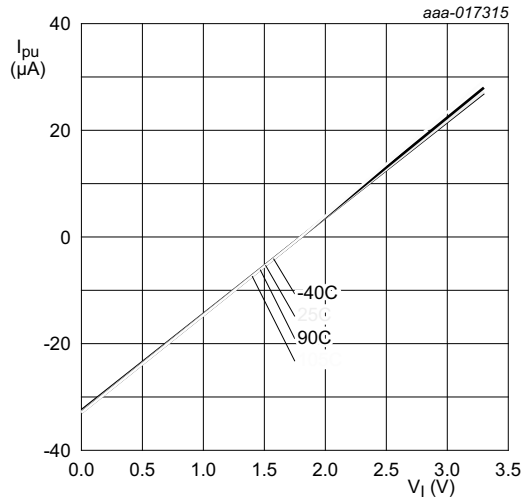


Conditions: V_{DD} = 1.8 V; on standard port pins.

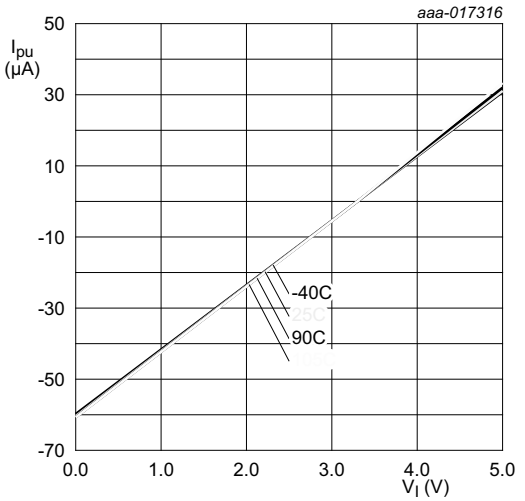


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 21. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

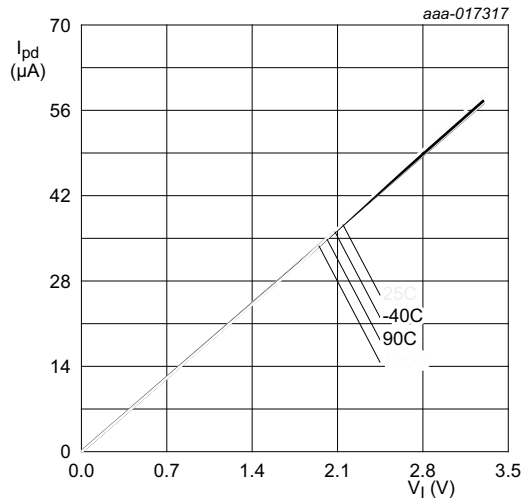


Conditions: V_{DD} = 1.8 V; on standard port pins.

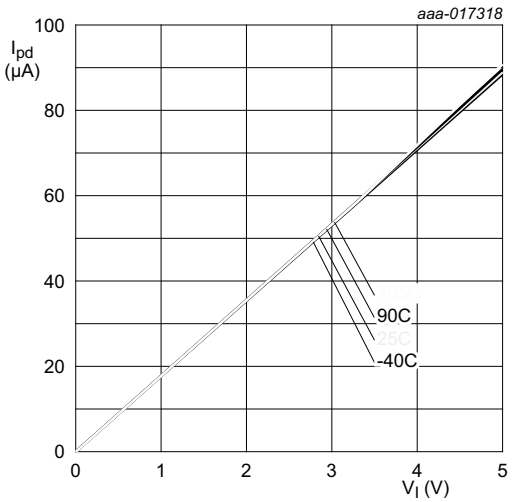


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 22. Typical pull-up current I_{PU} versus input voltage V_I



Conditions: V_{DD} = 1.8V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 23. Typical pull-down current I_{PD} versus input voltage V_I

Table 29. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 20 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 4.9	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 5.4	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 2.5	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 5.6	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 2.6	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 6.3	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 3.1	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 6.1	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 2.4	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	9.3	ns
$t_{h(Q)}$	data output hold time		−2.4	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 30 for internal programmable delay.

Table 36. Dynamic characteristics of the PLL2[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL2 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL2 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at $f_{out} = f_{CCO} = 540$ MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.9 FRO

The FRO is trimmed to ±1 % accuracy over the entire voltage and temperature range.

Table 37. Dynamic characteristic: FRO

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	FRO clock frequency	-	11.88	12	12.12	MHz
$f_{osc(RC)}$	FRO clock frequency	-	47.52	48	48.48	MHz
$f_{osc(RC)}$	FRO clock frequency	-	95.04	96	96.96	MHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

11.10 Crystal oscillator

Table 38. Dynamic characteristic: oscillator

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Low-frequency mode (1-20 MHz)[4]							
$t_{jit(per)}$	period jitter time	5 MHz crystal	[3]	-	13.2	-	ps
		10 MHz crystal		-	6.6	-	ps
		15 MHz crystal		-	4.8	-	ps

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Master; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		21.4	-	30.4	ns
		100 MHz < CCLK ≤ 180 MHz		20.6	-	28.7	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		21.1	-	29	ns
		100 MHz < CCLK ≤ 180 MHz		20.3	-	28.3	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		1.3	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		2.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.3	-	-	ns
Slave; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		13.8	-	23.6	ns
		100 MHz < CCLK ≤ 180 MHz		13	-	21.9	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.2	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0.7	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		1.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.3	-	-	ns

[1] Based on characterization; not tested in production.

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

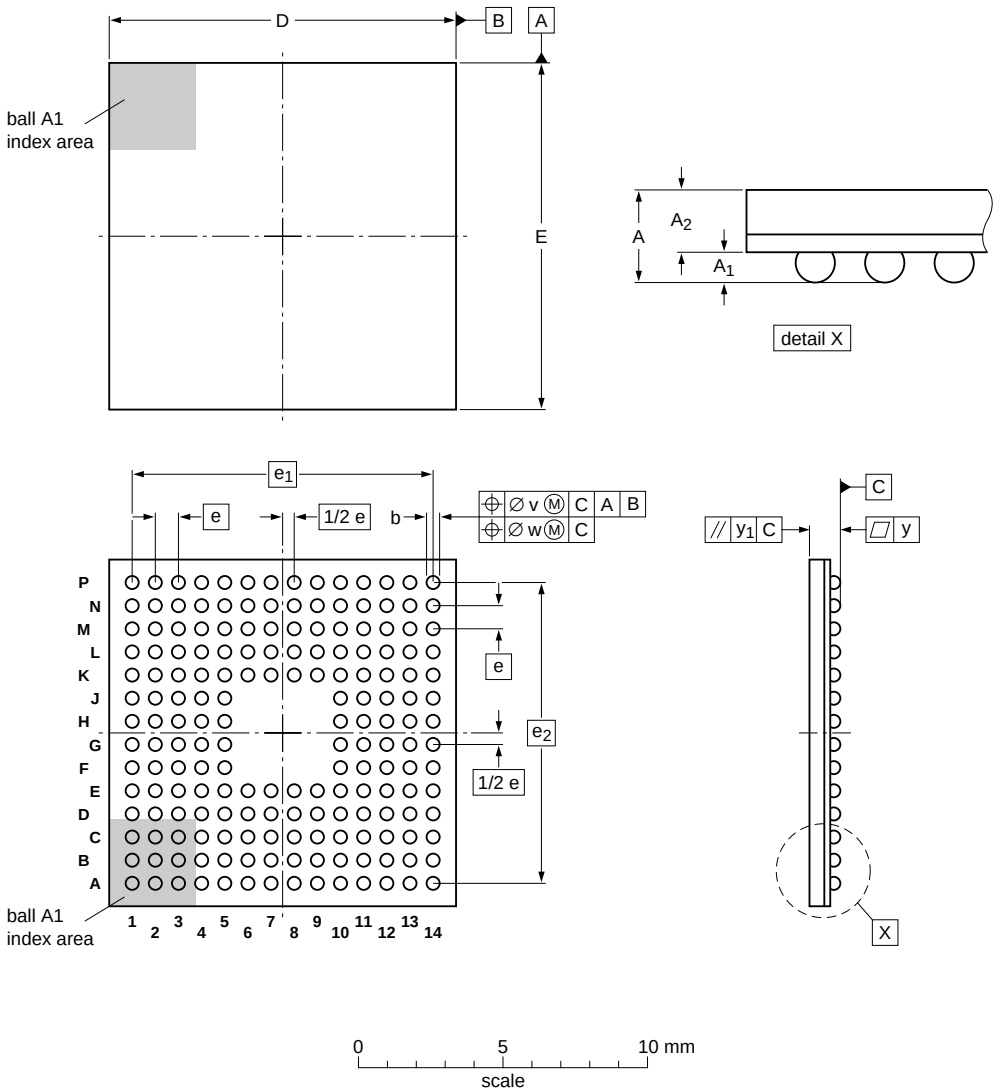
[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM10912) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

TFBGA180: thin fine-pitch ball grid array package; 180 balls **SOT570-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.20	0.40	0.80	0.50	12.1	12.1	0.8	10.4	10.4	0.15	0.05	0.12	0.1
	nom	1.06	0.35	0.71	0.45	12.0	12.0							
	min	0.95	0.30	0.65	0.40	11.9	11.9							

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT570-3						~~08-07-09~~ 10-04-15

Fig 52. TFBGA180 package

21. Contents

continued >>