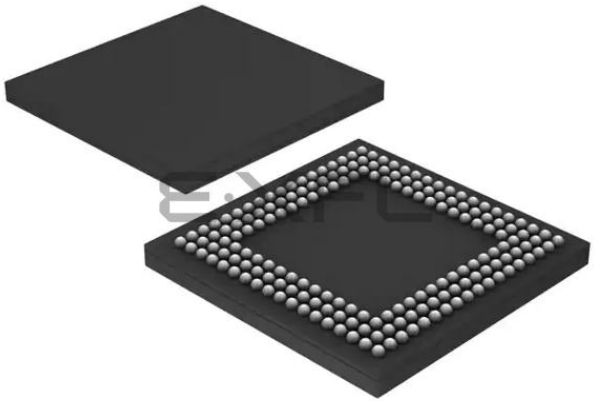

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	145
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54607j512et180e

4. Marking

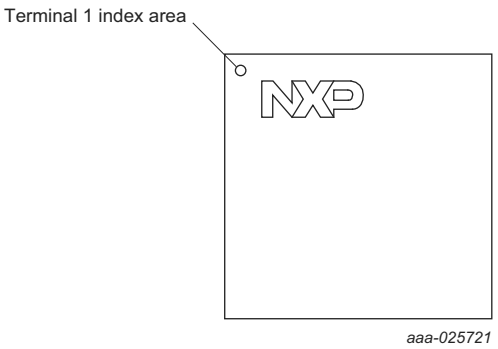


Fig 1. TFBGA180 and TFBGA100 package markings

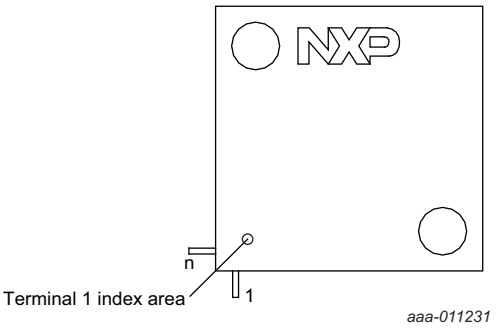


Fig 2. LQFP208 package marking

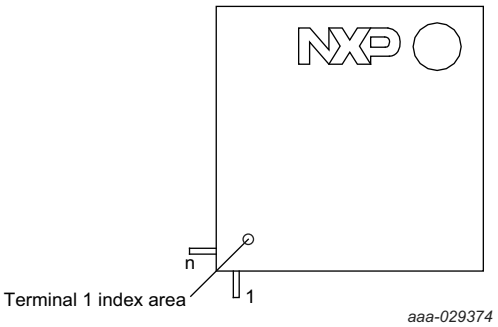


Fig 3. LQFP100 package marking

The LPC546xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC546xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_6/ TDO	A4	A5	191	90	[2]	PU	I/O	**PIO0_6 —** General-purpose digital input/output pin. In boundary scan mode: TDO (Test Data Out). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_5 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[4] —** External Memory interface data [4].
							I	**ENET_RX_DV —** Ethernet receive data valid.
PIO0_7	F9	H12	125	61	[2]	PU	I/O	**PIO0_7 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I/O	**EMC_D[5] —** External Memory interface data [5].
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
PIO0_8	E9	H10	133	64	[2]	PU	I/O	**PIO0_8 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SWO —** Serial Wire Debug trace output.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**EMC_D[6] —** External Memory interface data [6].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_26	-	H11	124	-	[2]	PU	I/O	**PIO2_26 —** General-purpose digital input/output pin.
							O	**LCD_VD[8] —** LCD Data [8].
								R — Reserved.
							I/O	**FC3_SCK —** Flexcomm 3: USART or SPI clock.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
PIO2_27	-	H14	130	-	[2]	PU	I/O	**PIO2_27 —** General-purpose digital input/output pin.
							O	**LCD_VD[9] —** LCD Data [9].
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
PIO2_28	-	G13	134	-	[2]	PU	I/O	**PIO2_28 —** General-purpose digital input/output pin.
							O	**LCD_VD[10]) —** LCD Data [10].
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
PIO2_29	-	G11	137	-	[2]	PU	I/O	**PIO2_29 —** General-purpose digital input/output pin.
							O	**LCD_VD[11] —** LCD Data [11].
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I	**CT2_CAP3 —** Capture 3 input to Timer 2.
							O	**CLKOUT —** Output of the CLKOUT function.
PIO2_30	-	F12	143	-	[2]	PU	I/O	**PIO2_30 —** General-purpose digital input/output pin.
							O	**LCD_VD[12] —** LCD Data [12].
								R — Reserved.
								R — Reserved.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
PIO2_31	-	D14	149	-	[2]	PU	I/O	**PIO2_31 —** General-purpose digital input/output pin.
							O	**LCD_VD[13] —** LCD Data [13].
PIO3_0	-	D12	155	-	[2]	PU	I/O	**PIO3_0 —** General-purpose digital input/output pin.
							O	**LCD_VD[14] —** LCD Data [14].
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_31	-	-	114	-	[2]	PU	I/O	**PIO4_31 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
							I/O	**EMC_D[26] —** External Memory interface data [26].
PIO5_0	-	-	122	-	[2]	PU	I/O	**PIO5_0 —** General-purpose digital input/output pin.
							I	**ENET_RX_DV —** Ethernet receive data valid.
							I/O	**SD_D[7] —** SD/MMC data 7.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I/O	**EMC_D[27] —** External Memory interface data [27].
PIO5_1	-	-	126	-	[2]	PU	I/O	**PIO5_1 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							O	**SD_VOLT[0] —** SD/MMC card regulator voltage control [0].
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**EMC_D[28] —** External Memory interface data [28].
PIO5_2	-	-	202	-	[2]	PU	I/O	**PIO5_2 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							O	**SD_VOLT[1] —** SD/MMC card regulator voltage control [1].
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							I/O	**EMC_D[29] —** External Memory interface data [29].

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M4 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus. The I-code and D-code core buses allow for concurrent code and data accesses from different slave ports.

The LPC546xx uses a multi-layer AHB matrix to connect the ARM Cortex-M4 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals that are on different slave ports of the matrix to be accessed simultaneously by different bus masters.

7.2 ARM Cortex-M4 processor

The ARM Cortex-M4 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M4 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptable/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller with wake-up interrupt controller, and multiple core buses capable of simultaneous accesses.

A 3-stage pipeline is employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

7.3 ARM Cortex-M4 integrated Floating Point Unit (FPU)

The FPU fully supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between fixed-point and floating-point data formats, and floating-point constant instructions.

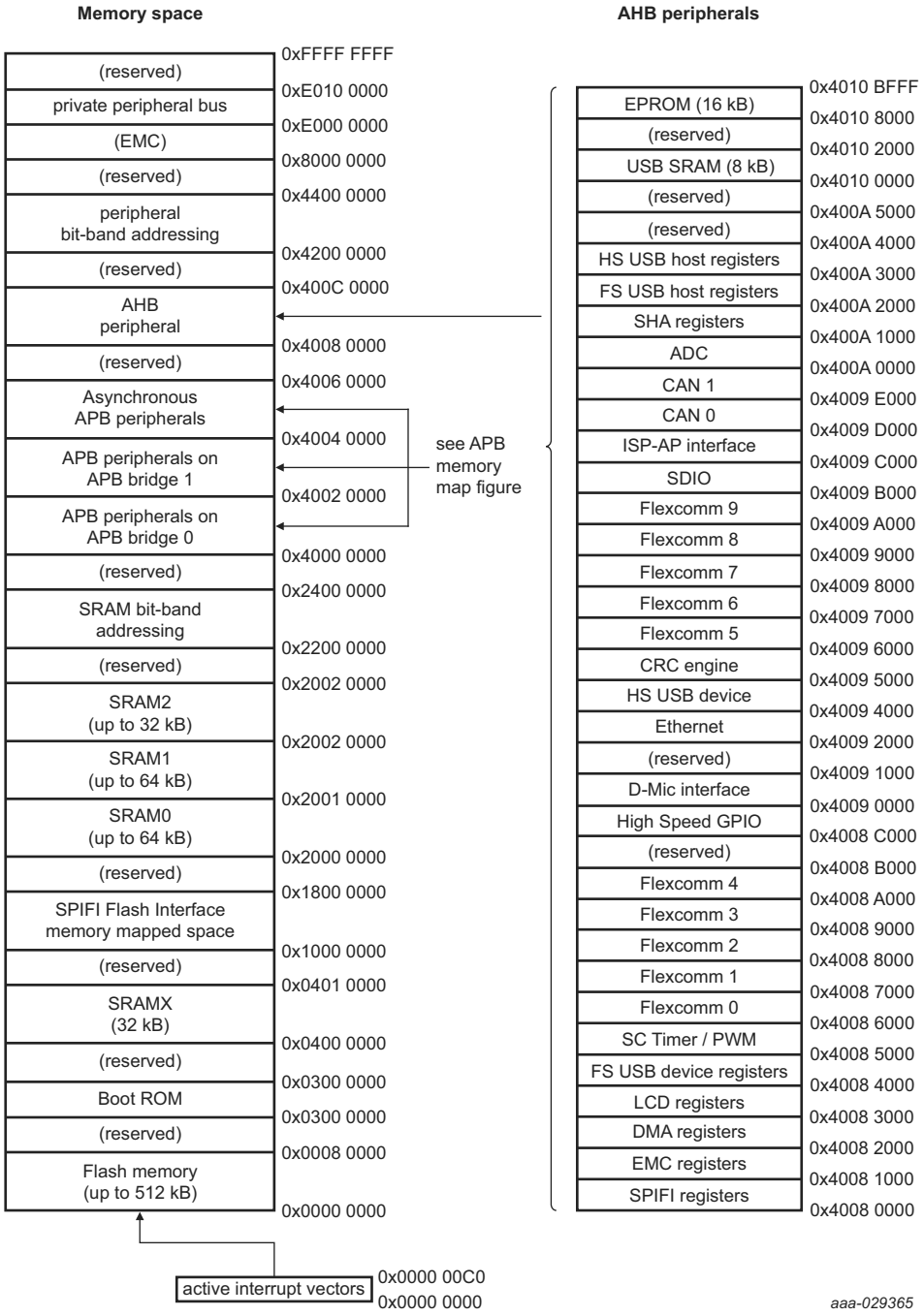
The FPU provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard.

7.4 Memory Protection Unit (MPU)

The Cortex-M4 includes a Memory Protection Unit (MPU) which can be used to improve the reliability of an embedded system by protecting critical data within the user application.

The MPU allows separating processing tasks by disallowing access to each other's data, disabling access to memory regions, allowing memory regions to be defined as read-only and detecting unexpected memory accesses that could potentially break the system.

The MPU separates the memory into distinct regions and implements protection by preventing disallowed accesses. The MPU supports up to eight regions each of which can be divided into eight subregions. Accesses to memory locations that are not defined in the MPU regions, or not permitted by the region setting, will cause the Memory Management Fault exception to take place.



The private peripheral bus includes CPU peripherals such as the NVIC, SysTick, and the core control registers.

Fig 9. LPC546xx Memory mapping

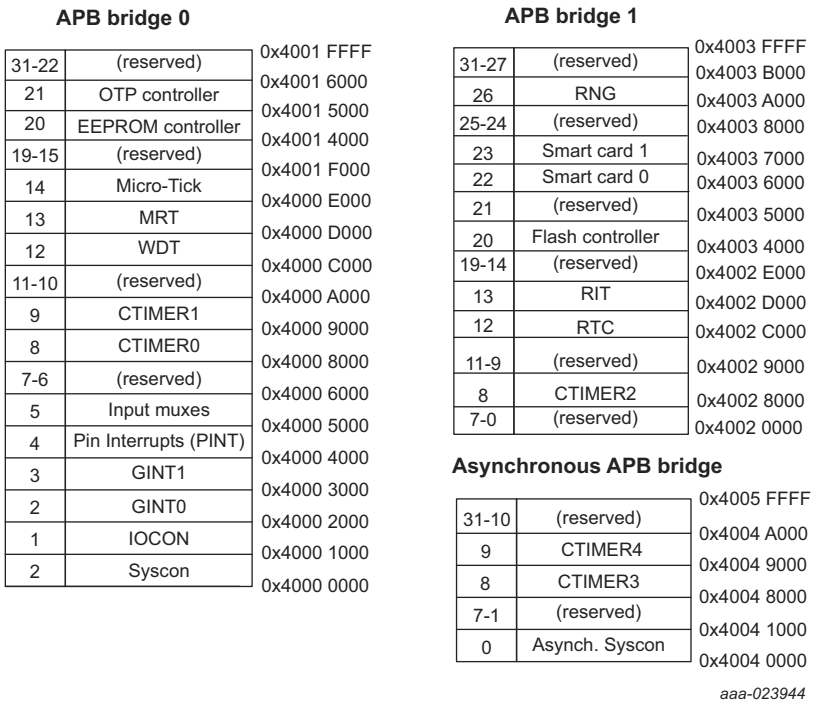


Fig 10. LPC546xx APB Memory map

7.12 System control

7.12.1 Clock sources

The LPC546xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.12.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.12.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

7.12.1.3 Crystal oscillator

The LPC546xx include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC546xx will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 11 and Figure 12 for an overview of the LPC546xx clock generation.

7.12.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.17.3 Ethernet AVB

The Ethernet block enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration.

7.17.3.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Supports IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
  - Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.17.4 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the LPC546xx microcontroller with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.17.4.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.

- Supports DMA access.
- Provides XIP (execute in place) feature to execute code directly from serial flash.

7.17.5 CAN Flexible Data (CAN FD) interface

The LPC546xx contains two CAN FD interfaces, CAN FD 1 and CAN FD 2.

7.17.5.1 Features

- Conforms with CAN protocol version 2.0 part A, B and ISO 11898-1.
- CAN FD with up to 64 data bytes supported.
- CAN Error Logging.
- AUTOSAR support.
- SAE J1939 support.
- Improved acceptance filtering.

7.17.6 DMIC subsystem

7.17.6.1 Features

- Pulse-Density Modulation (PDM) data input for left and/or right channels on 1 or 2 buses.
- Flexible decimation.
- 16 entry FIFO for each channel.
- DC blocking or unaltered DC bias can be selected.
- Data can be transferred using DMA from deep-sleep mode without waking up the CPU, then automatically returning to deep-sleep mode.
- Data can be streamed directly to I^2S on Flexcomm Interface 7.

7.17.7 Smart card interface

7.17.7.1 Features

- Two DMA supported ISO 7816 Smart Card Interfaces.
- Both asynchronous protocols, T = 0 and T = 1 are supported.

7.17.8 Flexcomm Interface serial communication

7.17.8.1 Features

- USART with asynchronous operation or synchronous master or slave operation.
- SPI master or slave, with up to 4 slave selects.
- I^2C, including separate master, slave, and monitor functions.
- Two I2S functions using Flexcomm Interface 6 and Flexcomm Interface 7.
- Data for USART, SPI, and I2S traffic uses the Flexcomm Interface FIFO. The I^2C function does not use the FIFO.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP208 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	33 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		16 ± 15 %	°C/W
LQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	48 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	65 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		19 ± 15 %	°C/W
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W
TFBGA100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	69 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	60 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		10 ± 15 %	°C/W

10.4 Power consumption

Power measurements in Active, sleep, and deep-sleep modes were performed under the following conditions:

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 1 to the GPIO CLR register to drive the outputs LOW.
- All peripherals disabled.

Table 15. Static characteristics: Power consumption in active and sleep mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified.1.71 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
Active mode[1]							
I_{DD}	supply current	CoreMark code executed from SRAMX; flash powered down					
		CCLK = 12 MHz	[3][4][5][7]	-	3.3	-	mA
		CCLK = 96 MHz	[3][4][5][7]	-	11	-	mA
		CCLK = 180 MHz	[4][5][7][8]	-	24	-	mA
		CCLK = 220 MHz	[4][5][7][8]	-	30	-	mA
I_{DD}	supply current	CoreMark code executed from flash;					
		CCLK = 12 MHz; 1 system clock flash access time.	[3][4][5][6]	-	4	-	mA
		CCLK = 96 MHz; 5 system clock flash access time.	[3][4][5][6]	-	9.4	-	mA
		CCLK = 180 MHz; 9 system clock flash access time.	[4][5][6][8]	-	17	-	mA
		CCLK = 220 MHz; 8 system clock flash access time.	[4][5][6][8][9]	-	22.4	-	mA
		CCLK = 220 MHz; 9 system clock flash access time.	[4][5][6][8]	-	21.9	-	mA
Sleep mode							
I_{DD}	supply current	CCLK = 12 MHz	[3][4][5][7]	-	1.7	-	mA
		CCLK = 96 MHz	[3][4][5][7]	-	4.1	-	mA
		CCLK = 180 MHz	[4][5][8]	-	8.3	-	mA

[1] Based on the power API library from the SDK software package available on nxp.com.

[2] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), 3.3V.

[3] Clock source FRO. PLL disabled.

[4] Characterized through bench measurements using typical samples.

[5] Compiler settings: Keil uVision v.5.21, optimization level 0, optimized for time off.

[6] Acceleration enable bit in the FLASHCFG register is set to 0. SRAM0 powered. SRAM1, SRAM2, SRAM3, USB SRAM and SRAMX powered down.

[7] Flash is powered down; SRAM0 and SRAMX are powered; SRAM1, SRAM2, SRAM3, and USB SRAM are powered down. All peripheral clocks disabled.

[8] Clock source FRO. PLL enabled.

[9] At 220 MHz the system clock/access time can be lower when compared to 180 MHz because the power library optimizes the on-chip voltage regulator.

11.12 Watchdog oscillator

Table 40. Dynamic characteristics: Watchdog oscillator

T_{amb} = −40 °C to +105 °C; 1.71 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal watchdog oscillator frequency		[2]	200	-	1500	kHz
D_{clkout}	clkout duty cycle			48	-	52	%
J_{PP-CC}	peak-peak period jitter		[3][4]	-	1	20	ns
t_{start}	start-up time		[4]	-	4	-	μs

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = −40 °C to +105 °C) is ±40 %.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Guaranteed by design. Not tested in production samples.

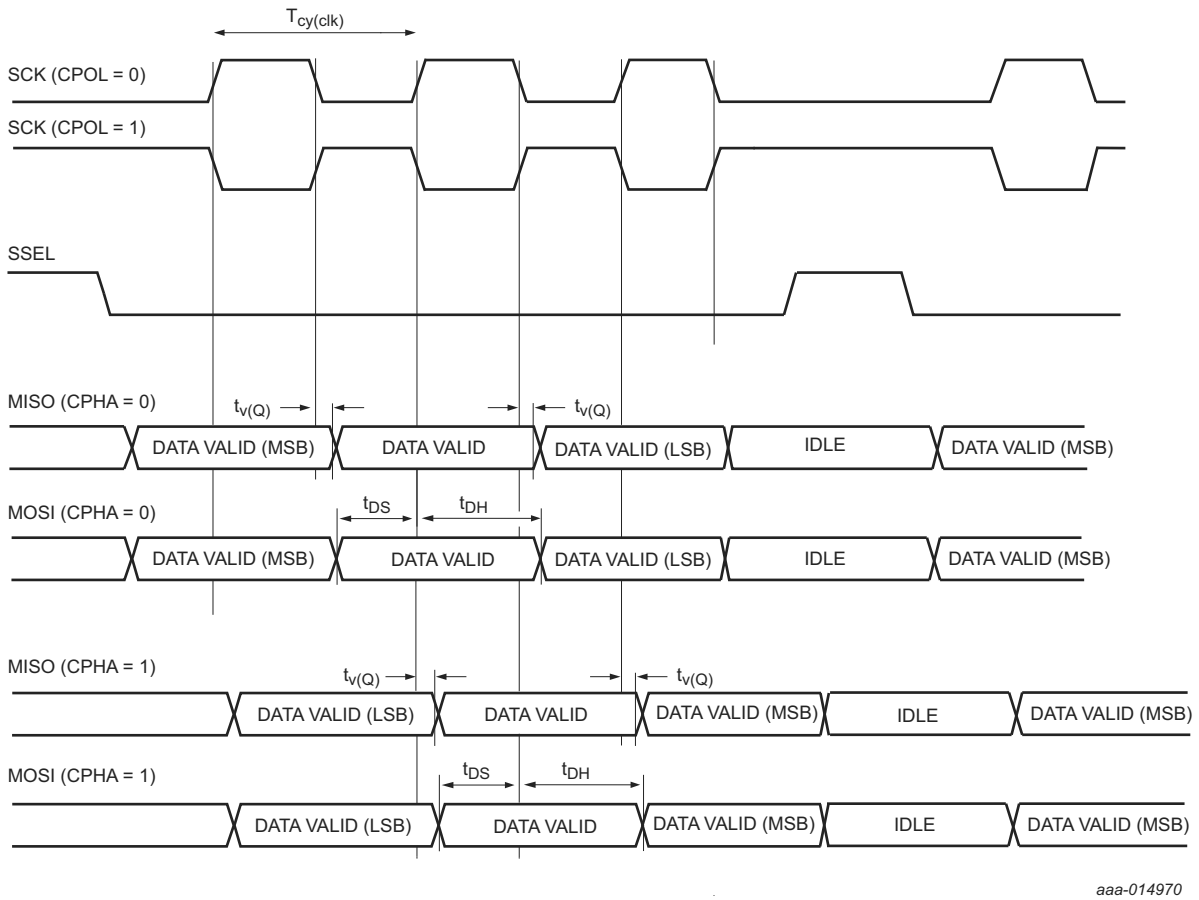


Fig 32. SPI slave timing

11.16 SPIFI

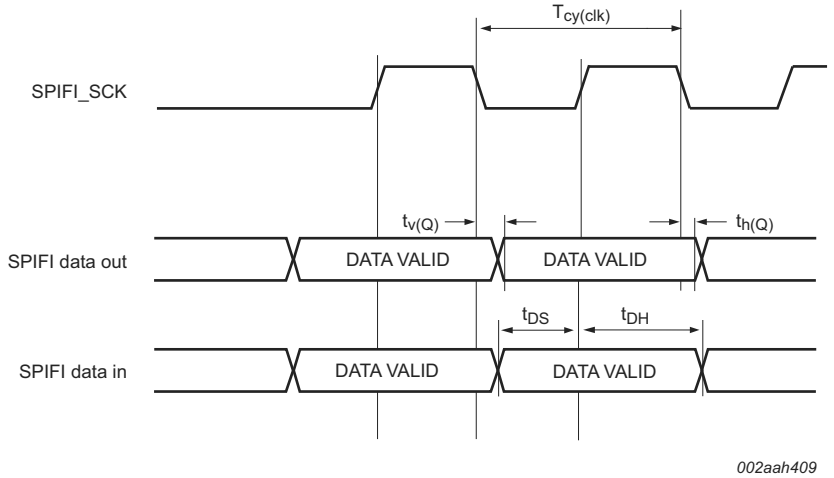
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 44. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge. Maximum SPIFI clock = 100 MHZ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		100 MHz < CCLK ≤ 180 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		100 MHz < CCLK ≤ 180 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 33. SPIFI control register (Mode 0)

11.18 Smart card interface

Table 46. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		100 MHz < CCLK ≤ 180 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

12. Analog characteristics

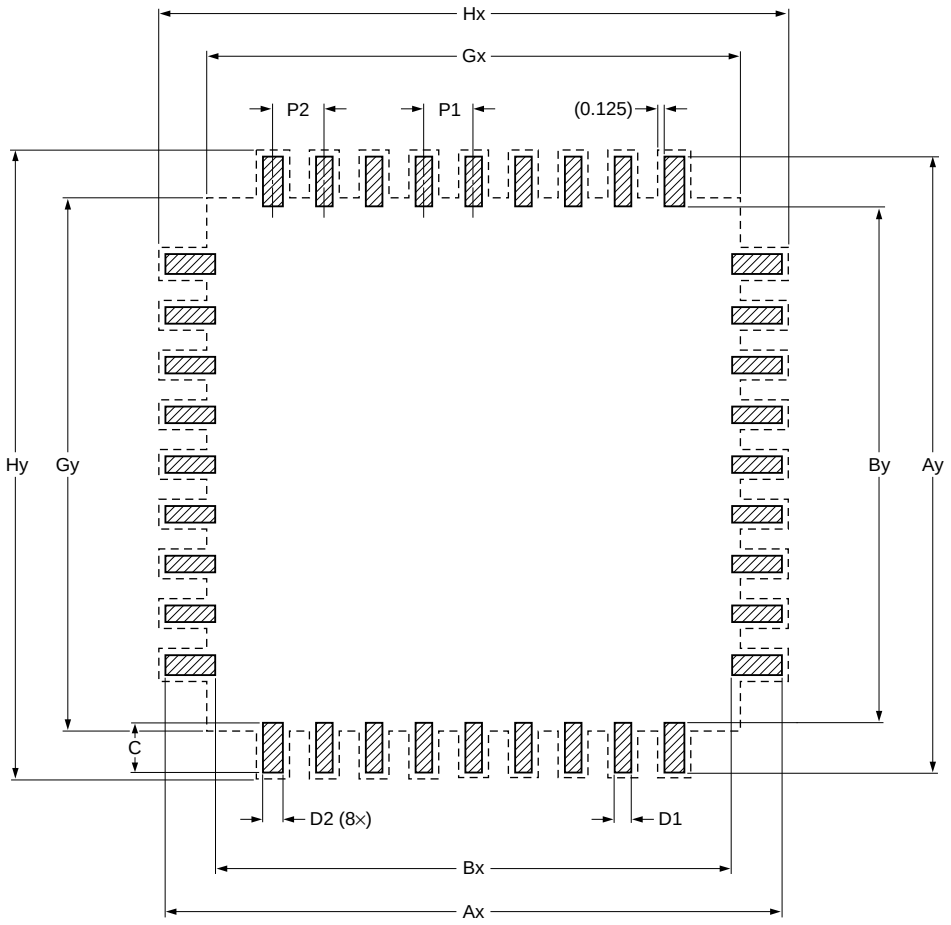
12.1 BOD

Table 53. BOD static characteristics

T_{amb} = 25 °C; based on characterization; not tested in production.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0					
		assertion		1.5	-	1.63	V
		de-assertion		1.55	-	1.69	V
		reset level 0					
		assertion		1.5	-	1.62	V
		de-assertion		1.55	-	1.69	V
V_{th}	threshold voltage	interrupt level 1					
		assertion		1.54	-	1.68	V
		de-assertion		1.6	-	1.75	V
		reset level 1					
		assertion		1.55	-	1.68	V
		de-assertion		1.61	-	1.74	V
V_{th}	threshold voltage	interrupt level 2					
		assertion		1.79	-	1.95	V
		de-assertion		1.85	-	2.02	V
		reset level 2					
		assertion		2.04	-	2.21	V
		de-assertion		2.19	-	2.38	V
V_{th}	threshold voltage	interrupt level 3					
		assertion		2.62	-	2.86	V
		de-assertion		2.77	-	3.03	V
		reset level 3					
		assertion		2.62	-	2.85	V
		de-assertion		2.78	-	3.02	V

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering of the LQFP100 package