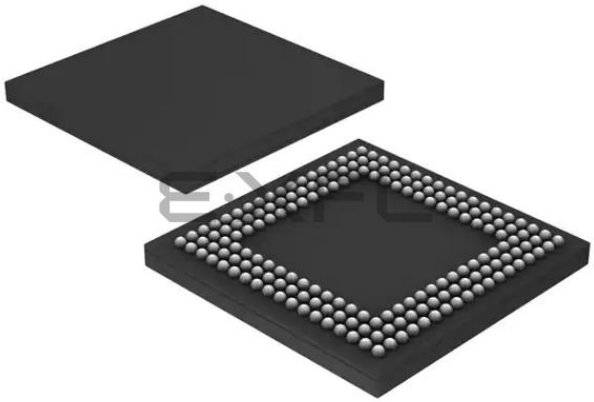

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	145
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54616j256et180e

- CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - SCTimer/PWM with 8 input and 10 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 10 match/captures, 10 events, and 10 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - enhanced Code Read Protection (eCRP) to protect user code.
  - OTP memory for ECRP settings, and user application specific data.
  - Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ± 1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.

- Watchdog Oscillator (WDTOSC) with a frequency range of 6 kHz to 1.5 MHz.
- 32.768 kHz low-power RTC oscillator.
- System PLL allows CPU operation up to the maximum CPU rate and can run from the main oscillator, the internal FRO, the watchdog oscillator or the 32.768 KHz RTC oscillator.
- Two additional PLLs for USB clock and audio subsystem.
- Independent clocks for the SPIFI interface, ADC, USBs, and the audio subsystem.
- Clock output function with divider.
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.

- Power control:
  - Programmable PMU (Power Management Unit) to minimize power consumption and to match requirements at different performance levels.
  - Reduced power modes: sleep, deep-sleep, and deep power-down.
  - Wake-up from deep-sleep modes due to activity on the USART, SPI, and I2C peripherals when operating as slaves.
  - Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes.
  - Power-On Reset (POR).
  - Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- Single power supply 1.71 V to 3.6 V.
- Power-On Reset (POR).
- Brown-Out Detect (BOD) with separate thresholds for interrupt and forced reset.
- JTAG boundary scan supported.
- 128 bit unique device serial number for identification.
- Operating temperature range −40 °C to +105 °C.
- Available in TFBGA180, TFBGA100, LQFP208, and LQFP100 packages.

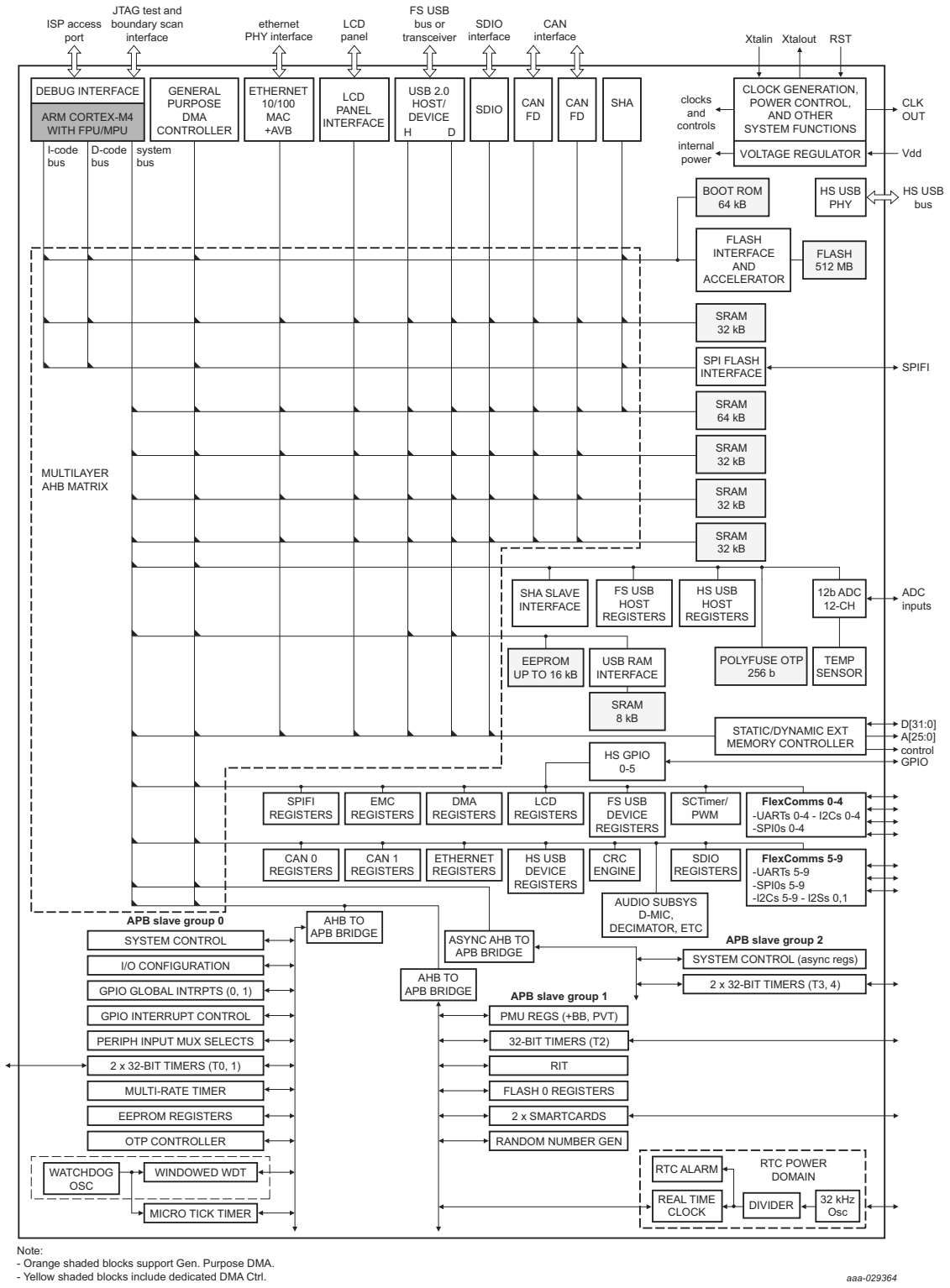


Fig 4. LPC546xx Block diagram

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_3/ TCK	A6	A10	178	85	[2]	PU	I/O	**PIO0_3 —** General-purpose digital input/output pin. In boundary scan mode: TCK (Test Clock In). **Remark:** In ISP mode, this pin is set to the Flexcomm 3 SPI MOSI function.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[1] —** External Memory interface data [1].
PIO0_4/ TMS	B6	C8	185	87	[2]	PU	I/O	**PIO0_4 —** General-purpose digital input/output pin. In boundary scan mode: TMS (Test Mode Select). **Remark:** The state of this pin at Reset in conjunction with PIO0_5 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							I	**CAN0_RD —** Receiver input for CAN 0.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I	**CT3_CAP0 —** Capture input 0 to Timer 3.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[2] —** External Memory interface data [2].
							O	**ENET_MDC —** Ethernet management data clock.
PIO0_5/ TDI	A5	E7	189	89	[2]	PU	I/O	**PIO0_5 —** General-purpose digital input/output pin. In boundary scan mode: TDI (Test Data In). **Remark:** The state of this pin at Reset in conjunction with PIO0_4 and PIO0_6 will determine the boot source for the part or if ISP handler is invoked. See the Boot Process chapter in UM10912 for more details.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT3_MAT0 —** Match output 0 from Timer 3.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**EMC_D[3] —** External Memory interface data [3].
							I/O	**ENET_MDIO —** Ethernet management data I/O.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_25	-	P9	82	-	[2]	PU	I/O	**PIO3_25 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP2 —** Capture input 2 to Timer 4.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[14] —** External memory interface address 14.
PIO3_26	-	K5	88	-	[2]	PU	I/O	**PIO3_26 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[15] —** External memory interface address 15.
PIO3_27	-	P14	96	-	[2]	PU	I/O	**PIO3_27 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[16] —** External memory interface address 16.
PIO3_28	-	M11	100	-	[2]	PU	I/O	**PIO3_28 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
								R — Reserved.
							O	**EMC_A[17] —** External memory interface address 17.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_5	-	E10	154	-	[2]	PU	I/O	**PIO4_5 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**EMC_CKE[2] —** External memory interface SDRAM clock enable 2.
PIO4_6	-	D10	161	-	[2]	PU	I/O	**PIO4_6 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**EMC_CKE[3] —** External memory interface SDRAM clock enable 3.
PIO4_7	-	A14	166	-	[2][8]	PU	I/O	**PIO4_7 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP3 —** Capture input 3 to Timer 4.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
PIO4_8	-	B14	170	-	[2]	PU	I/O	**PIO4_8 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
USBn_DM	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.
USB1_AVSCC	F	Tie to VSS.
USB1_VBUS	F	Tie to VDD.
USB1_AVDDC3V3	F	Tie to VDD.
USB1_AVDDTX3V3	F	Tie to VDD.
USB1_AVSSTX3V3	F	Tie to VSS.
USB1_ID	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected.

[1] I = Input, IA = Inactive (no pull-up/pull-down enabled), PU = Pull-Up enabled, F = Floating

6.2.2 Pin states in different power modes

Table 6. Pin states in different power modes

Pin	Active	Sleep	Deep-sleep	Deep power-down[2]
PIOn_m pins (not I2C)	As configured in the IOCON[1]. Default: internal pull-up enabled.			Floating
PIO0_13 to PIO0_14 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
PIO3_23 to PIO3_24 (open-drain I2C-bus pins)	As configured in the IOCON[1].			Floating
$\overline{\text{RESET}}$	Reset function enabled. Default: input, internal pull-up enabled. Reset function disabled.			

[1] Default and programmed pin states are retained in sleep and deep-sleep.

[2] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

7.13 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

Remark: If the ECRP is set to the most restrictive combination of OTP and the ECRP of the images, no future factory testing can be performed on the device.

7.14 Power control

The LPC546xx support a variety of power control features. In Active mode, when the chip is running, power and clocks to selected peripherals can be adjusted for power consumption. In addition, there are three special modes of processor power reduction with different peripherals running: sleep mode, deep-sleep mode, and deep power-down mode that can be activated using the power API library from the LPCOpen software package.

7.14.1 Sleep mode

In sleep mode, the system clock to the CPU is stopped and execution of instructions is suspended until either a reset or an interrupt occurs. Peripheral functions, if selected to be clocked can continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, internal buses, and unused peripherals. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.14.2 Deep-sleep mode

In deep-sleep mode, the system clock to the processor is disabled as in sleep mode. All analog blocks are powered down by default but can be selected to keep running through the power API if needed as wake-up sources. The main clock and all peripheral clocks are disabled. The FRO is disabled. The flash memory is put in standby mode.

Deep-sleep mode eliminates all power used by analog peripherals and all dynamic power used by the processor itself, memory systems and related controllers, and internal buses. The processor state and registers, peripheral registers, and internal SRAM values are maintained, and the logic levels of the pins remain static.

7.17.3 Ethernet AVB

The Ethernet block enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard. The Ethernet interface contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration.

7.17.3.1 Features

- 10/100 Mbit/s
- DMA support
- Power management remote wake-up frame and magic packet detection
- Supports both full-duplex and half-duplex operation
  - Supports CSMA/CD Protocol for half-duplex operation.
  - Supports IEEE 802.3x flow control for full-duplex operation.
  - Optional forwarding of received pause control frames to the user application in full-duplex operation.
  - Supports IEEE 802.1AS-2011 and 802.1-Qav-2009 for Audio Video (AV) traffic.
  - Software support for AVB feature is available from NXP Professional Services. See nxp.com for more details.
  - Back-pressure support for half-duplex operation.
  - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation.
- Supports IEEE1588 time stamping and IEEE 1588 advanced time stamping (IEEE 1588-2008 v2).

7.17.4 SPI Flash Interface (SPIFI)

The SPI Flash Interface allows low-cost serial flash memories to be connected to the LPC546xx microcontroller with little performance penalty compared to parallel flash devices with higher pin count.

After a few commands configure the interface at startup, the entire flash content is accessible as normal memory using byte, halfword, and word accesses by the processor and/or DMA channels. Simple sequences of commands handle erasure and programming.

Many serial flash devices use a half-duplex command-driven SPI protocol for device setup and initialization and then move to a half-duplex, command-driven 4-bit protocol for normal operation. Different serial flash vendors and devices accept or require different commands and command formats. SPIFI provides sufficient flexibility to be compatible with common flash devices and includes extensions to help insure compatibility with future devices.

7.17.4.1 Features

- Interfaces to serial flash memory in the main memory map.
- Supports classic and 4-bit bidirectional serial protocols.
- Half-duplex protocol compatible with various vendors and devices.
- Quad SPI Flash Interface with 1-, 2-, or 4-bit data at rates of up to 52 MB per second.

7.19.6 Repetitive Interrupt Timer (RIT)

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.19.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Can be used for ETM debug time stamping.

7.20 12-bit Analog-to-Digital Converter (ADC)

The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.20.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.

7.21 CRC engine

The Cyclic Redundancy Check (CRC) generator with programmable polynomial settings supports several CRC standards commonly used. To save system power and bus bandwidth, the CRC engine supports DMA transfers.

7.21.1 Features

- Supports three common polynomials CRC-CCITT, CRC-16, and CRC-32.
  - CRC-CCITT: $x^{16} + x^{12} + x^5 + 1$
  - CRC-16: $x^{16} + x^{15} + x^2 + 1$
  - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Bit order reverse and 1's complement programmable setting for input data and CRC sum.
- Programmable seed number setting.
- Supports CPU PIO or DMA back-to-back transfer.
- Accept any size of data width per write: 8, 16 or 32-bit.
  - 8-bit write: 1-cycle operation.
  - 16-bit write: 2-cycle operation (8-bit x 2-cycle).
  - 32-bit write: 4-cycle operation (8-bit x 4-cycle).

7.22 Temperature sensor

The temperature sensor transducer uses an intrinsic pn-junction diode reference and outputs a CTAT voltage (Complement To Absolute Temperature). The output voltage varies inversely with device temperature with an absolute accuracy of better than ±5 °C over the full temperature range (−40 °C to +105 °C). The temperature sensor is only approximately linear with a slight curvature. The output voltage is measured over different ranges of temperatures and fit with linear-least-square lines.

After power-up, the temperature sensor output must be allowed to settle to its stable value before it can be used as an accurate ADC input.

For an accurate measurement of the temperature sensor by the ADC, the ADC must be configured in single-channel burst mode. The last value of a nine-conversion (or more) burst provides an accurate result.

7.23 Security features

The OTP memory contains a memory bank of 128 bits each. OTP bank contains 4 words: word 0 for ECRP, word 1 is reserved, words 2 and 3 can be used by user application for storing application specific options.

7.23.1 Features

- OTP memory.
- Random number generator (RNG).

7.23.2 SHA-1 and SHA-2

The Hash peripheral is used to perform SHA-1 and SHA-2 (256) based hashing. A hash takes an arbitrarily large message or image and forms a relatively small fixed size “unique” number called a digest. The data is fed by words from the processor, DMA, or hosted access; the words are converted from little-endian (ARM standard) to big-endian (SHA standard) by the block.

7.23.2.1 Features

- Used with an HMAC to support a challenge/response or to validate a message.
- Can be used to verify external memory that has not been compromised.

7.24 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

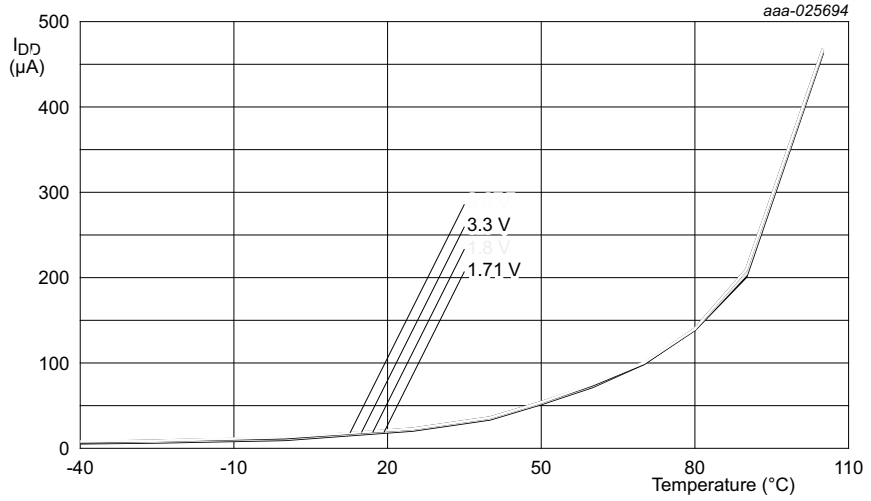
For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

7.25 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

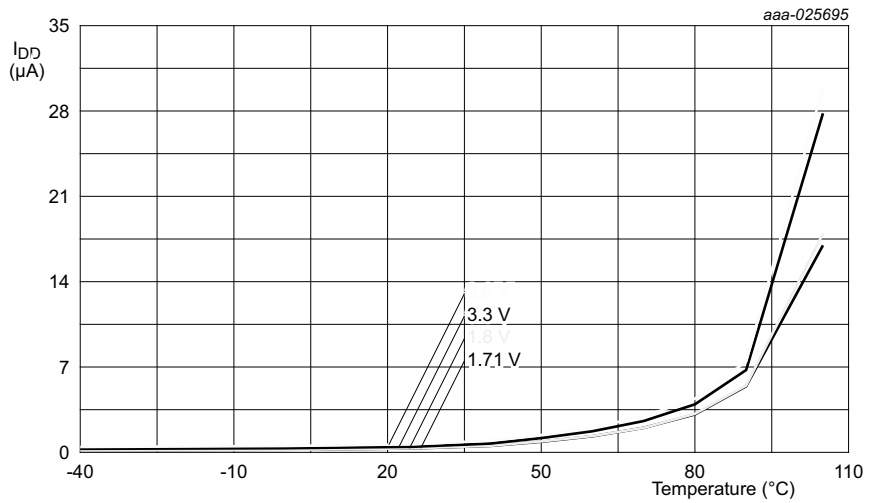
The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.



Conditions: BOD disabled; all oscillators and analog blocks disabled; all SRAM disabled except 32 KB SRAMX.

Remark: At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage.

Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



RTC disabled (RTC oscillator input grounded).

Fig 17. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 19 shows the typical peripheral power consumption measured on a typical sample at Tamb = 25 °C and VDD = 3.3 V. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1/2, and PDRUNCFG0/1

11.7 USB PLL (PLL1)

Table 33. PLL1 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL1 configuration: input frequency 12 MHz; output frequency 48 MHz							
$t_{lock(PLL1)}$	PLL1 lock time		[1]	-	7.4	-	μs
$I_{DD(PLL1)}$	PLL1 current	When locked	[1][2]	-	260	-	μA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 34. Dynamic characteristics of the PLL1[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL1 clkout output	[2]	9.75	-	160	MHz
d_o	output duty cycle	for PLL1 clkout output		45	-	55	%
f_{CCO}	CCO frequency			156	-	320	MHz
Dynamic parameters at f_{out} = f_{CCO} = 320 MHz; standard bandwidth settings							
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 4 MHz	[3][4]	-	-	300	ps

[1] Data based on simulation, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.8 Audio PLL (PLL2)

Table 35. PLL2 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	96	μs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	2.0	mA
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	108	μs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

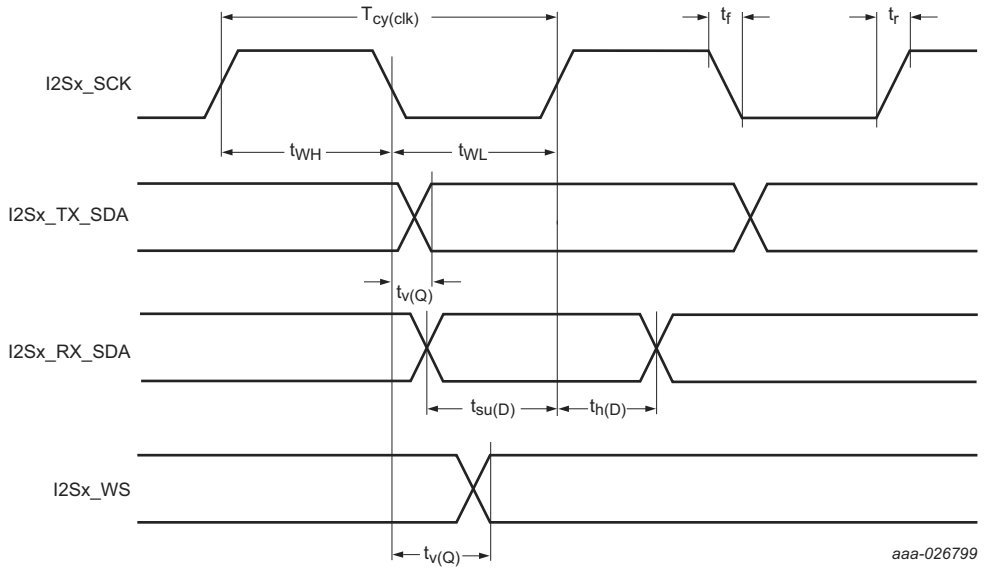


Fig 29. I²S-bus timing (master)

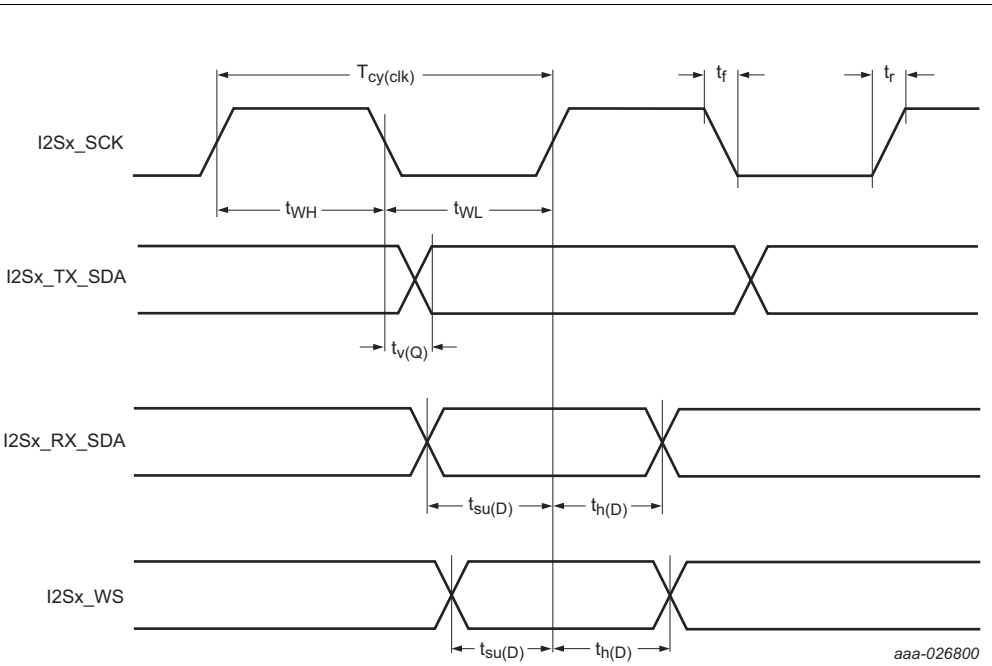


Fig 30. I²S-bus timing (slave)

11.16 SPIFI

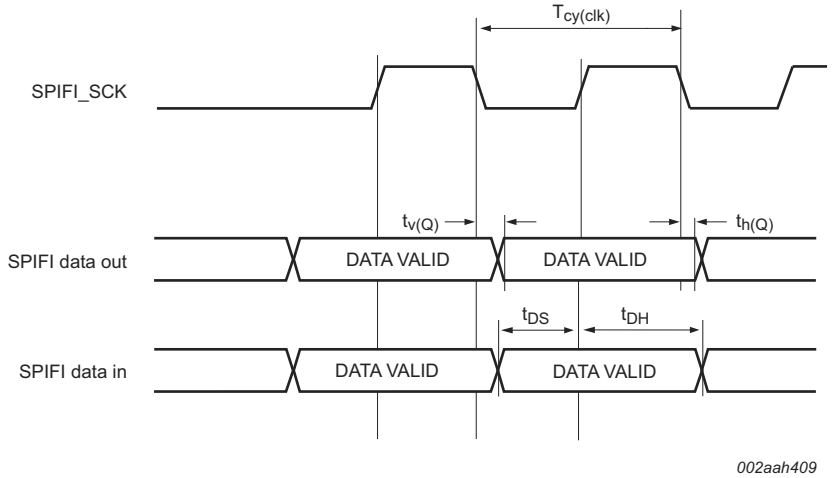
The actual SPIFI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPIFI mode is 100 Mbit/s.

Table 44. Dynamic characteristics: SPIFI[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW set to standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge. Maximum SPIFI clock = 100 MHZ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPIFI 1.71 V ≤ VDD ≤ 2.7 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	6.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	6.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	5.7	-	13.7	ns
		100 MHz < CCLK ≤ 180 MHz	5.7	-	13.7	ns
SPIFI 2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	4	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	3.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	3.6	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	3.3	-	11.5	ns
		100 MHz < CCLK ≤ 180 MHz	3.3	-	11.5	ns

[1] Based on simulation; not tested in production.



In mode 0, MODE3 bit (23) in SPIFI CTRL register is set to '0' (default). The SPIFI drives SCK low after the rising edge at which the last bit of each command is captured, and keeps it LOW while CS is HIGH.

Fig 33. SPIFI control register (Mode 0)

11.18 Smart card interface

Table 46. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		100 MHz < CCLK ≤ 180 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

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