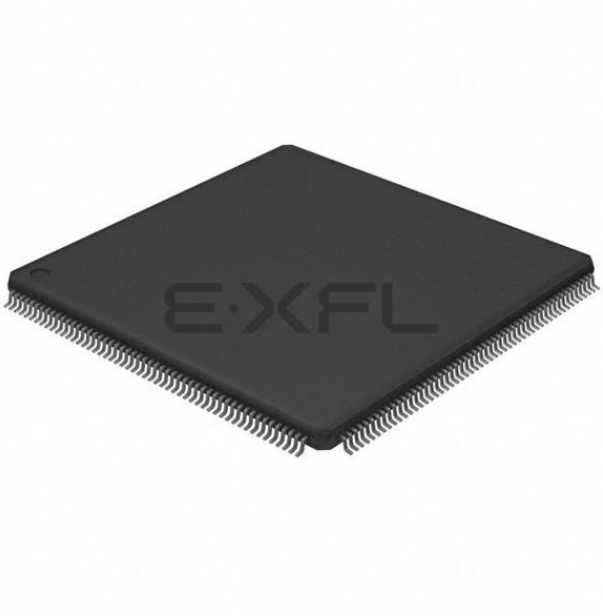

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	171
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54616j512bd208e

- CRC engine block can calculate a CRC on supplied data using one of three standard polynomials with DMA support.
- Up to 171 General-Purpose Input/Output (GPIO) pins.
- GPIO registers are located on the AHB for fast access. The DMA supports GPIO ports.
- Up to eight GPIOs can be selected as Pin Interrupts (PINT), triggered by rising, falling or both input edges.
- Two GPIO Grouped Interrupts (GINT) enable an interrupt based on a logical (AND/OR) combination of input states.
- CRC engine.

- Analog peripherals:
  - 12-bit ADC with 12 input channels and with multiple internal and external trigger inputs and sample rates of up to 5.0 MSamples/sec. The ADC supports two independent conversion sequences.
  - Integrated temperature sensor connected to the ADC.
- DMIC subsystem including a dual-channel PDM microphone interface, flexible decimators, 16 entry FIFOs, optional DC locking, hardware voice activity detection, and the option to stream the processed output data to I^2S.
- Timers:
  - Five 32-bit general purpose timers/counters, four of which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests. The fifth timer does not have external pin connections and may be used for internal timing operations.
  - SCTimer/PWM with 8 input and 10 output functions (including capture and match). Inputs and outputs can be routed to/from external pins and internally to or from selected peripherals. Internally, the SCTimer/PWM supports 10 match/captures, 10 events, and 10 states.
  - 32-bit Real-time clock (RTC) with 1 s resolution running in the always-on power domain. A timer in the RTC can be used for wake-up from all low power modes including deep power-down, with 1 ms resolution.
  - Multiple-channel multi-rate 24-bit timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
  - Windowed Watchdog Timer (WWDT).
  - Repetitive Interrupt Timer (RIT) for debug time stamping and for general purpose use.
- Security features:
  - enhanced Code Read Protection (eCRP) to protect user code.
  - OTP memory for ECRP settings, and user application specific data.
  - Secure Hash Algorithm (SHA1/SHA2) module with dedicated DMA controller.
- Clock generation:
  - 12 MHz internal Free Running Oscillator (FRO). This oscillator provides a selectable 48 MHz or 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to ± 1 % accuracy over the entire voltage and temperature range.
  - External clock input for clock frequencies of up to 25 MHz.
  - Crystal oscillator with an operating range of 1 MHz to 25 MHz.

4. Marking

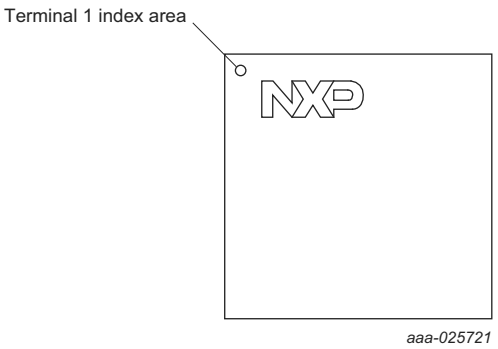


Fig 1. TFBGA180 and TFBGA100 package markings

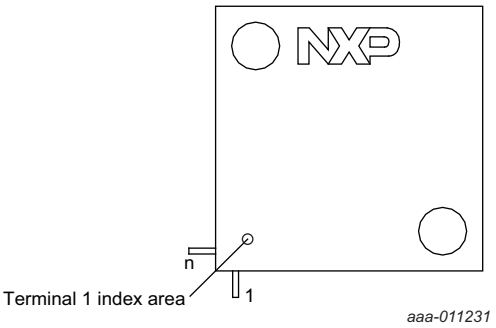


Fig 2. LQFP208 package marking

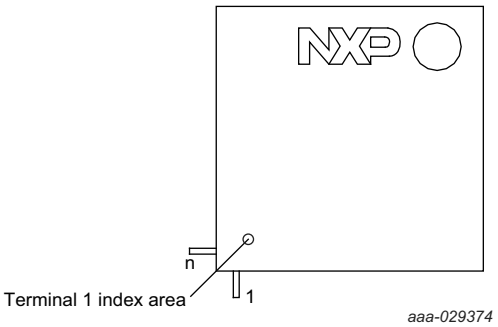


Fig 3. LQFP100 package marking

The LPC546xx TFBGA180 and TFBGA100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: ET180 or ET100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The LPC546xx LQFP208 and LQFP100 packages have the following top-side marking:

- First line: LPC546xxJyyy
  - yyy: flash size
- Second line: BD208 or BD100
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]x

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_18	D2	D1	15	5	[2]	PU	I/O	**PIO1_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							I	**CAN1_RD —** Receiver input for CAN 1.
							O	**EMC_BLSN[1] —** External memory interface byte lane select 1 (active low).
PIO1_19	F3	L1	33	16	[2]	PU	I/O	**PIO1_19 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							I/O	**FC4_SCK —** Flexcomm 4: USART or SPI clock.
							I/O	**EMC_D[8] —** External Memory interface data [8].
PIO1_20	G2	M1	35	17	[2]	PU	I/O	**PIO1_20 —** General-purpose digital input/output pin.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**CT3_CAP2 —** Capture 2 input to Timer 3.
								R — Reserved.
							I/O	**FC4_TXD_SCL_MISO —** Flexcomm 4: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**EMC_D[9] —** External Memory interface data [9].
PIO1_21	K6	N8	74	37	[2]	PU	I/O	**PIO1_21 —** General-purpose digital input/output pin.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
								R — Reserved.
							I/O	**FC4_RXD_SDA_MOSI —** Flexcomm 4: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**EMC_D[10] —** External Memory interface data [10].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_19	-	P12	93	-	[2]	PU	I/O	**PIO2_19 —** General-purpose digital input/output pin.
							O	**LCD_VD[1] —** LCD Data [1].
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
PIO2_20	-	P13	95	-	[2]	PU	I/O	**PIO2_20 —** General-purpose digital input/output pin.
							O	**LCD_VD[2] —** LCD Data [2].
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							O	**CT3_MAT2 —** Match output 2 from Timer 3.
							I	**CT4_CAP0 —** Capture input 4 to Timer 0.
PIO2_21	-	L10	99	-	[2]	PU	I/O	**PIO2_21 —** General-purpose digital input/output pin.
							O	**LCD_VD[3] —** LCD Data [3].
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
PIO2_22	-	K10	113	-	[2]	PU	I/O	**PIO2_22 —** General-purpose digital input/output pin.
							O	**LCD_VD[4] —** LCD Data [4].
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
								R — Reserved.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
PIO2_23	-	M14	115	-	[2]	PU	I/O	**PIO2_23 —** General-purpose digital input/output pin.
							O	**LCD_VD[5] —** LCD Data [5].
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
PIO2_24	-	K14	118	-	[2]	PU	I/O	**PIO2_24 —** General-purpose digital input/output pin.
							O	**LCD_VD[6] —** LCD Data [6].
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
PIO2_25	-	J11	121	-	[2][8]	PU	I/O	**PIO2_25 —** General-purpose digital input/output pin.
							O	**LCD_VD[7] —** LCD Data [7].
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_1	-	G14	132	-	[2]	PU	I/O	**PIO4_1 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							O	**EMC_CSN[2] —** External memory interface static chip select 2 (active low).
PIO4_2	-	F14	138	-	[2]	PU	I/O	**PIO4_2 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**EMC_CSN[3] —** External memory interface static chip select 3 (active low).
PIO4_3	-	F13	140	-	[2]	PU	I/O	**PIO4_3 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
								R — Reserved.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**EMC_DYCSN[2] —** External Memory interface SDRAM chip select 2 (active low).
PIO4_4	-	D9	147	-	[2]	PU	I/O	**PIO4_4 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							O	**EMC_DYCSN[3] —** External Memory interface SDRAM chip select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_23	-	-	42	-	[2]	PU	I/O	**PIO4_23 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							I/O	**EMC_D[18] —** External Memory interface data [18].
PIO4_24	-	-	67	-	[2]	PU	I/O	**PIO4_24 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I	**SD_CARD_INT_N —** Card interrupt line.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I/O	**EMC_D[19] —** External Memory interface data [19].
PIO4_25	-	-	69	-	[2]	PU	I/O	**PIO4_25 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**EMC_D[20] —** External Memory interface data [20].
PIO4_26	-	-	73	-	[2]	PU	I/O	**PIO4_26 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[1] —** SD/MMC data 1.
								R — Reserved.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**EMC_D[21] —** External Memory interface data [21].

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Deep power-down	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTC CTRL register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC.
	Reset pin	Always available.

7.15 General Purpose I/O (GPIO)

The LPC546xx provides six GPIO ports with a total of up to 171 GPIO pins.

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current level of a port pin can be read back no matter what peripheral is selected for that pin.

7.15.1 Features

- Accelerated GPIO functions:
  - GPIO registers are located on the AHB so that the fastest possible I/O timing can be achieved.
  - Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
  - All GPIO registers are byte and half-word addressable.
  - Entire port value can be written in one instruction.
- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- All I/O default to inputs after reset.
- All GPIO pins can be selected to create an edge or level-sensitive GPIO interrupt request.
- One GPIO group interrupt can be triggered by a combination of any pin or pins.

7.16 Pin interrupt/pattern engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC. The pattern match engine can be used in conjunction with software to create complex state machines based on pin inputs. Any digital pin, independent of the function selected through the switch matrix can be configured through the SYSCON block as an input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the I/O+ bus for fast single-cycle access.

7.19.6 Repetitive Interrupt Timer (RIT)

The repetitive interrupt timer provides a free-running 48-bit counter which is compared to a selectable value, generating an interrupt when a match occurs. Any bits of the timer/compare can be masked such that they do not contribute to the match detection. The repetitive interrupt timer can be used to create an interrupt that repeats at predetermined intervals.

7.19.6.1 Features

- 48-bit counter running from the main clock. Counter can be free-running or can be reset when an RIT interrupt is generated.
- 48-bit compare value.
- 48-bit compare mask. An interrupt is generated when the counter value equals the compare value, after masking. This allows for combinations not possible with a simple compare.
- Can be used for ETM debug time stamping.

7.20 12-bit Analog-to-Digital Converter (ADC)

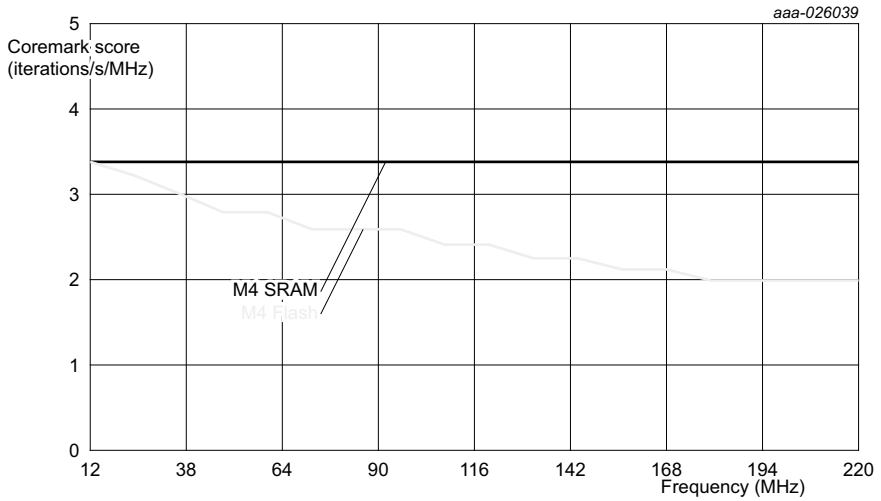
The ADC supports a resolution of 12-bit and fast conversion rates of up to 5 Msamples/s. Sequences of analog-to-digital conversions can be triggered by multiple sources. Possible trigger sources are the SCTimer/PWM, external pins, and the ARM TXEV interrupt.

The ADC supports a variable clocking scheme with clocking synchronous to the system clock or independent, asynchronous clocking for high-speed conversions

The ADC includes a hardware threshold compare function with zero-crossing detection. The threshold crossing interrupt is connected internally to the SCTimer/PWM inputs for tight timing control between the ADC and the SCTimer/PWM.

7.20.1 Features

- 12-bit successive approximation analog to digital converter.
- Input multiplexing among up to 12 pins.
- Two configurable conversion sequences with independent triggers.
- Optional automatic high/low threshold comparison and “zero crossing” detection.
- Measurement range VREFN to VREFP (typically 3 V; not to exceed VDDA voltage level).
- 12-bit conversion rate of 5.0 Msamples/s. Options for reduced resolution at higher conversion rates.
- Burst conversion mode for single or multiple inputs.
- Synchronous or asynchronous operation. Asynchronous operation maximizes flexibility in choosing the ADC clock frequency, Synchronous mode minimizes trigger latency and can eliminate uncertainty and jitter in response to a trigger.



Conditions: V_{DD} = 3.3 V; T_{amb} = 25 °C; active mode; all peripherals disabled; BOD disabled; See the FLASHCFG register in the LPC546xx. User Manual for system clock flash access time settings. Acceleration enable bit in the FLASCFG register is set to 1. Measured with IAR ver 8.22.2. Optimization level 3, optimized for time ON. Coremark score is based on the power API library from the SDK software package available on nxp.com.

12 MHz, 24 MHz, 48 MHz, and 96 MHz: FRO enabled; PLL disabled.
36 MHz, 60 MHz, 72 MHz, 84 MHz, 108 MHz, 120 MHz, 132 MHz, 144 MHz, 156 MHz, 168 MHz, 180 MHz, 192 MHz, 204 MHz, 216 MHz, and 220 MHz: FRO enabled; PLL enabled.
CoreMark score from flash: SRAM1, SRAM2, SRAM3, and USB SRAM powered down. SRAM0 and SRAMX powered.
CoreMark score from SRAMX: SRAM0 is powered; flash is powered down.

Fig 14. Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX

11.6 System PLL (PLL0)

Table 31. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL0 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]			96	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	2.0	mA
PLL0 configuration: input frequency 32 kHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]	-	-	108	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 32. Dynamic characteristics of the PLL0[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			32.768 kHz	-	25 MHz	
Clock output							
f_o	output frequency	for PLL0 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL0 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at f_{out} = f_{CCO} = 540 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

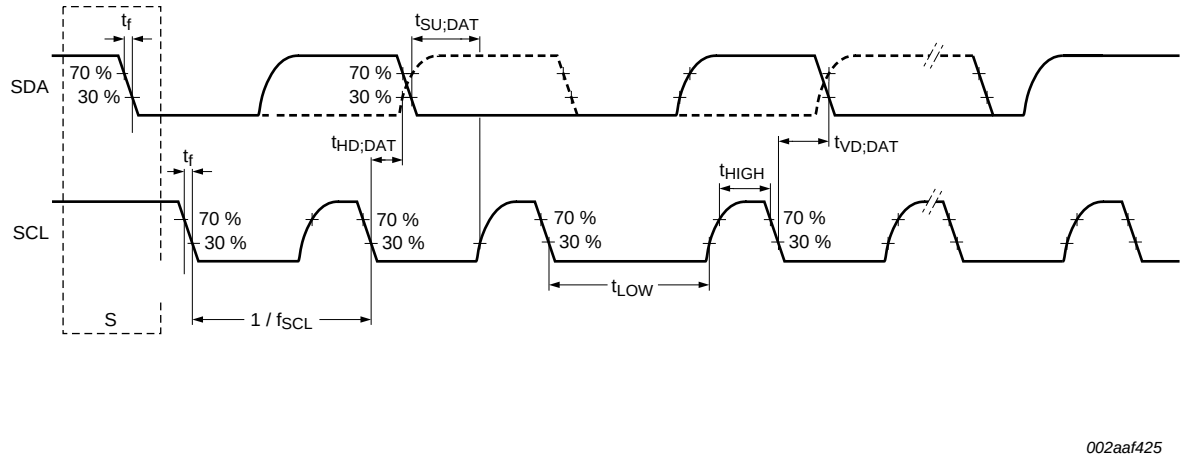


Fig 28. I²C-bus pins clock timing

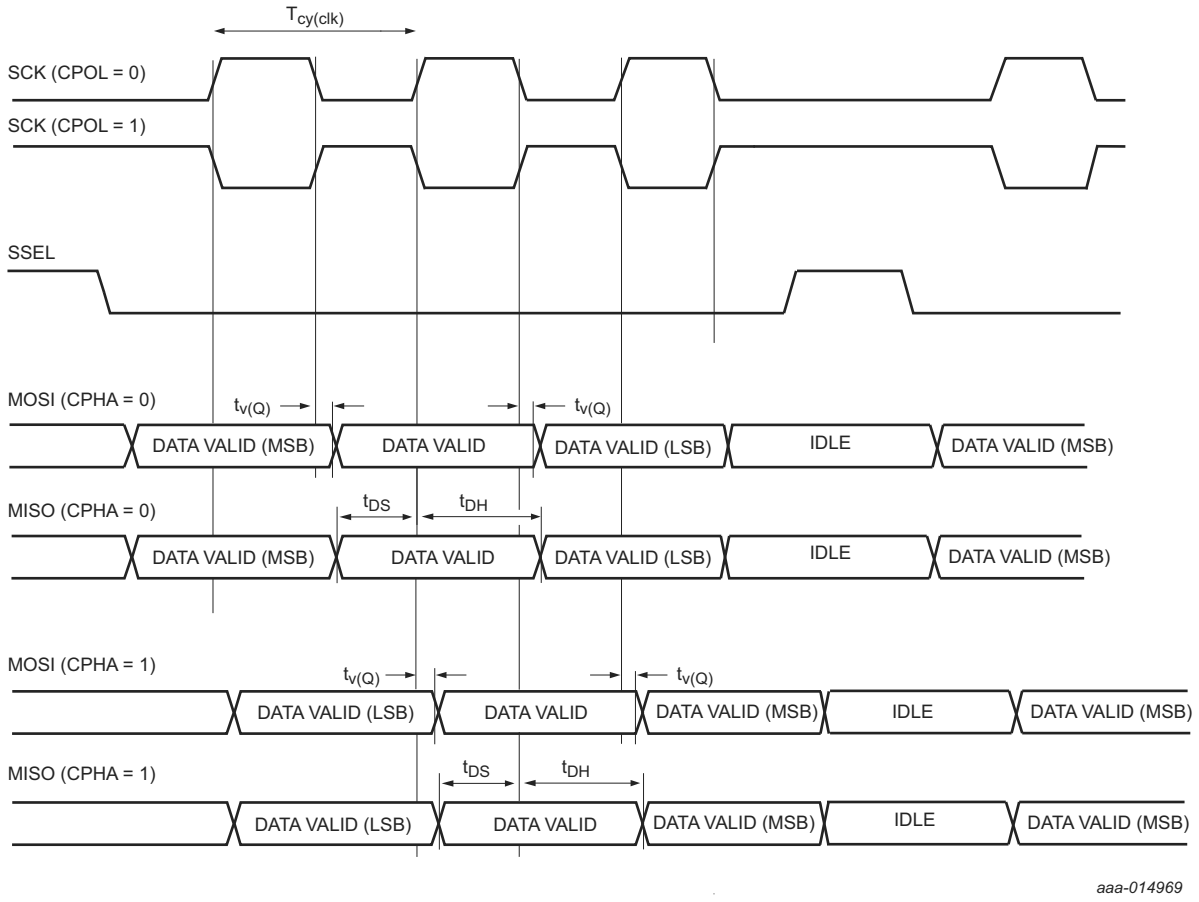


Fig 31. SPI master timing

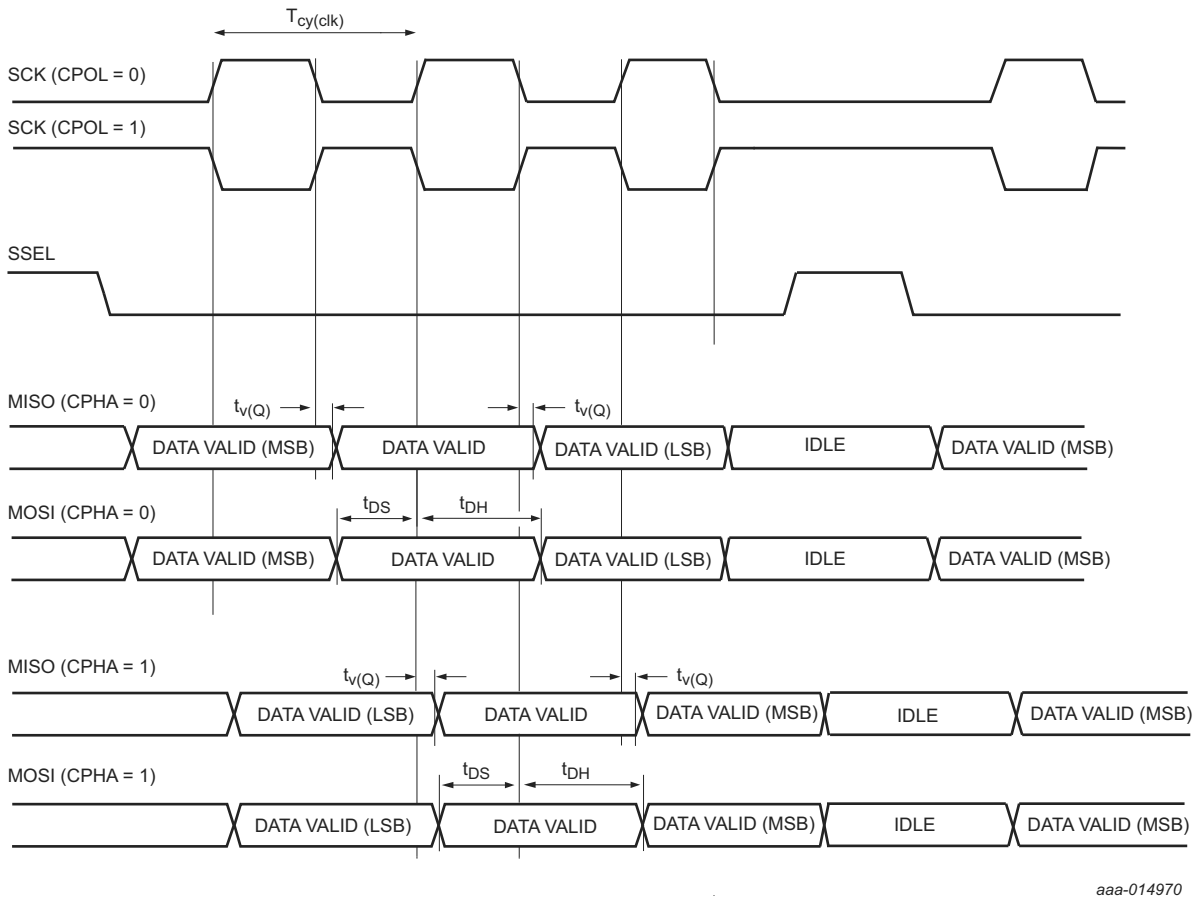


Fig 32. SPI slave timing

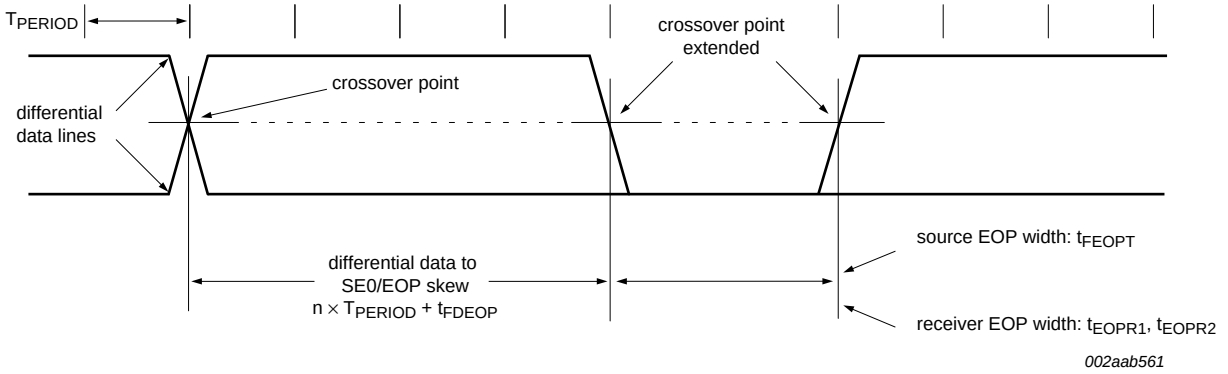


Fig 36. Differential data-to-EOP transition skew and EOP width

11.23 Ethernet AVB

Remark: The timing characteristics of the ENET_MDC and ENET_MDIO signals comply with the *IEEE standard 802.3*.

Table 50. Dynamic characteristics: Ethernet

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Based on simulation.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
RMII mode							
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	50.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.4	-	-	ns
t_h	data input hold time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		−1.3	-	0	ns
		100 MHz < CCLK ≤ 180 MHz		−1.3	-	0	ns
$t_{v(Q)}$	data output valid time	for ENET_TXDn, ENET_TX_EN	[1][2]				
		CCLK ≤ 100 MHz		9.9	-	17.3	ns
		100 MHz < CCLK ≤ 180 MHz		9.9	-	17.3	ns
MII mode							
f_{clk}	clock frequency	for ENET_TX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
f_{clk}	clock frequency	for ENET_RX_CLK	[1]	-	-	25.0	MHz
δ_{clk}	clock duty cycle		[1]	45.0	-	55.0	%
t_{su}	data input set-up time	for ENET_RXDn, ENET_RX_ER, ENET_RX_DV	[1][2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.7	-	-	ns

13. Application information

13.1 Start-up behavior

Figure 43 shows the start-up timing after reset. The FRO 12 MHz oscillator provides the default clock at Reset and provides a clean system clock shortly after the supply pins reach operating voltage.

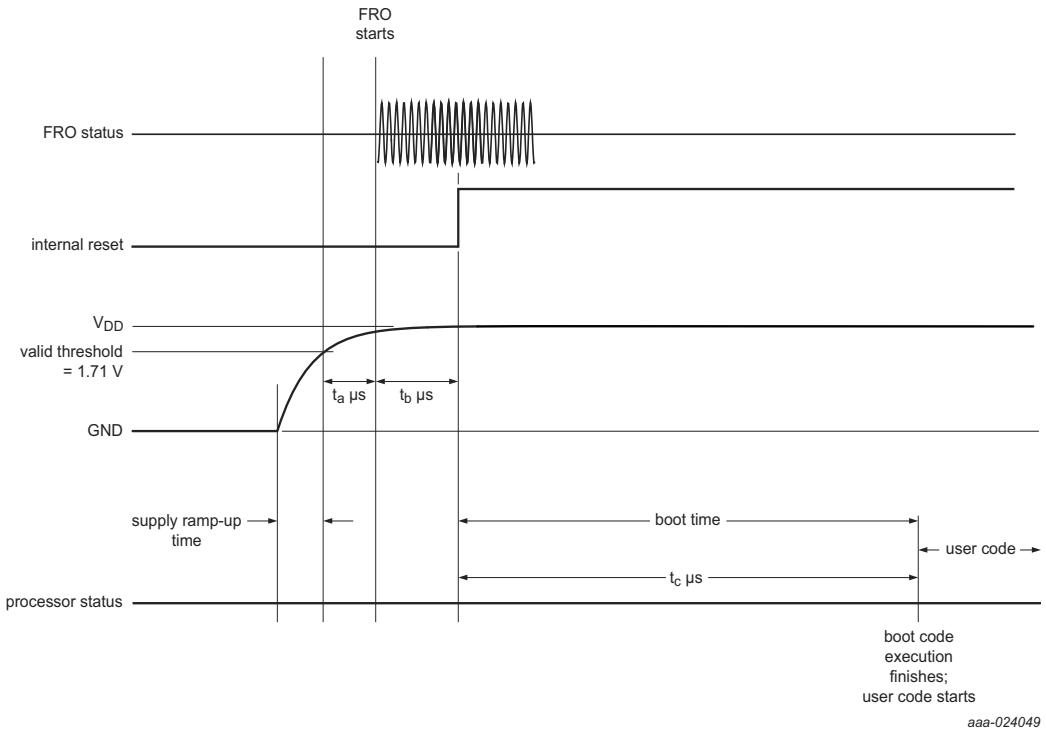


Fig 43. Start-up timing

Table 58. Typical start-up timing parameters

Parameter	Description	Value
t_a	FRO start time	≤ 20 µs
t_b	Internal reset de-asserted	151 µs
t_c	Legacy image	262 µs
	Single image without CRC	245 µs
	Dual image without CRC	289 µs

13.4 I/O power consumption

I/O pins are contributing to the overall dynamic and static power consumption of the part. If pins are configured as digital inputs, a static current can flow depending on the voltage level at the pin and the setting of the internal pull-up and pull-down resistors. This current can be calculated using the parameters R_{pu} and R_{pd} given in Table 21 for a given input voltage V_I. For pins set to output, the current drive strength is given by parameters I_{OH} and I_{OL} in Table 21, but for calculating the total static current, you also need to consider any external loads connected to the pin.

I/O pins also contribute to the dynamic power consumption when the pins are switching because the V_{DD} supply provides the current to charge and discharge all internal and external capacitive loads connected to the pin in addition to powering the I/O circuitry.

The contribution from the I/O switching current I_{sw} can be calculated as follows for any given switching frequency f_{sw} if the external capacitive load (C_{ext}) is known (see Table 21 for the internal I/O capacitance):

$$I_{sw} = V_{DD} \times f_{sw} \times (C_{io} + C_{ext})$$

13.6 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 47.

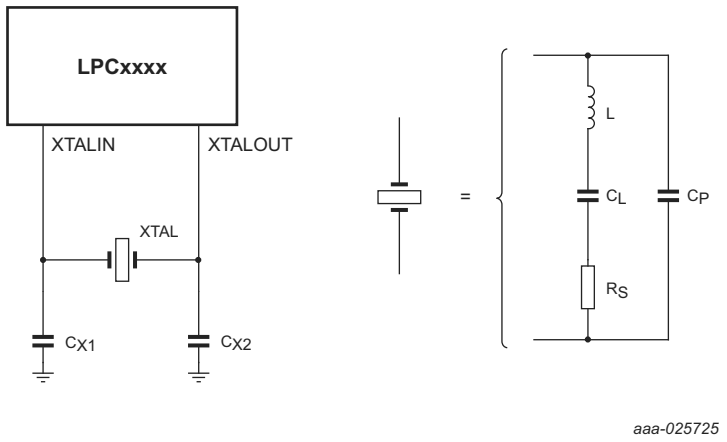


Fig 47. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC546xx v.1.5	20170331	Product data sheet	-	LPC546xx v.1.4
Modifications:	• Updated Table 51 “Dynamic characteristics: SD/MMC and SDIO”. The max clock frequency is 50 MHz. • Updated Section 7.18.2 “SD/MMC card interface”: Supports up to a maximum of 50 MHz of interface frequency. • Updated Table 41 “Dynamic characteristic: I2C-bus pins[1]” • Updated Figure 28 “I2S-bus timing (master)” and Figure 29 “I2S-bus timing (slave)”. • Updated Table 2 “Ordering options”. Parts LPC54618J512ET180 and LPC54618J512BD208 have Classic CAN. • Added Section 11.4 “Wake-up process”.			
LPC546xx v.1.4	20170307	Product data sheet	-	LPC5460x v.1.3
Modifications:	• Changed data sheet title to LPC546xx. • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes” and Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”.			
LPC5460x v.1.3	20170224	Product data sheet	-	LPC5460x v.1.2
Modifications:	• Removed S parts. Data sheet title renamed to LPC5460x. • Removed AES-256 engine and SHA references throughout the document. • Security peripherals renamed to Security features. • Updated Section 4 “Marking”. • Updated Section 5 “Block diagram”. • Updated Figure 6 “LPC546xx Memory mapping”. • Updated Table 20 “Typical AHB/APB peripheral power consumption [3][4][5]”.			
LPC5460x v.1.2	20170206	Product data sheet	-	LPC5460x v.1.1
Modifications:	• Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”: Static memory chip select: was 0x9000 0000 - 0x93 FFFF, now, 0x9000 0000 – 0x93FF FFFF. • Updated Figure 8 “LPC5460x clock generation”. • Updated Power control in Section 2 “Features and benefits”: Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes. • Updated Table 4 “Pin description”: PIO0_26, USB0_IDVALUE, Type is Input (I). • Updated Section 7.18.1.1 “Features”. • Updated Table 31 “Dynamic characteristics of the PLL0[1]”: Input frequency, $F_{in,}$ Max value is 25 MHZ.			
LPC5460x v.1.1	20170124	Product data sheet	-	LPC5460x v.1