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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	64
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54616j512et100e

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_6	F1	G4	30	15	[2]	PU	I/O	**PIO1_6 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[3] —** SD/MMC data 3.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[5] —** External memory interface address 5.
PIO1_7	H1	N1	38	18	[2]	PU	I/O	**PIO1_7 —** General-purpose digital input/output pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[1] —** SD/MMC data 1.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
								R — Reserved.
							O	**EMC_A[6] —** External memory interface address 6.
PIO1_8	H5	P8	72	36	[2]	PU	I/O	**PIO1_8 —** General-purpose digital input/output pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SD_CLK —** SD/MMC clock.
								R — Reserved.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
							O	**EMC_A[7] —** External memory interface address 7.
PIO1_9	K7	K6	78	39	[2]	PU	I/O	**PIO1_9 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC1_SCK —** Flexcomm 1: USART or SPI clock.
							I	**CT1_CAP0 —** Capture 0 input to Timer 1.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**EMC_CASN —** External memory interface column access strobe (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO1_22	K8	P11	89	43	[2]	PU	I/O	**PIO1_22 —** General-purpose digital input/output pin.
							I/O	**FC8_RTS_SCL_SSEL1 —** Flexcomm 8: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_CMD —** SD/MMC card command I/O.
							O	**CT2_MAT3 —** Match output 3 from Timer 2.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**EMC_CKE[1] —** External memory interface SDRAM clock enable 1.
PIO1_23	K10	M10	97	46	[2]	PU	I/O	**PIO1_23 —** General-purpose digital input/output pin.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							O	**SCT0_OUT0 —** SCTimer/PWM output 0.
								R — Reserved.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**EMC_A[11] —** External memory interface address 11.
PIO1_24	G8	N14	111	57	[2]	PU	I/O	**PIO1_24 —** General-purpose digital input/output pin.
							I/O	**FC2_RXD_SDA_MOSI —** Flexcomm 2: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
								R — Reserved.
								R — Reserved.
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**EMC_A[12] —** External memory interface address 12.
PIO1_25	G10	M12	119	59	[2]	PU	I/O	**PIO1_25 —** General-purpose digital input/output pin.
							I/O	**FC2_TXD_SCL_MISO —** Flexcomm 2: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_A[13] —** External memory interface address 13.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_23	-	-	42	-	[2]	PU	I/O	**PIO4_23 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							I/O	**EMC_D[18] —** External Memory interface data [18].
PIO4_24	-	-	67	-	[2]	PU	I/O	**PIO4_24 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I	**SD_CARD_INT_N —** Card interrupt line.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I/O	**EMC_D[19] —** External Memory interface data [19].
PIO4_25	-	-	69	-	[2]	PU	I/O	**PIO4_25 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**EMC_D[20] —** External Memory interface data [20].
PIO4_26	-	-	73	-	[2]	PU	I/O	**PIO4_26 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[1] —** SD/MMC data 1.
								R — Reserved.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**EMC_D[21] —** External Memory interface data [21].

7.12.1.3 Crystal oscillator

The LPC546xx include four independent oscillators. These are the main oscillator, the FRO, the watchdog oscillator, and the RTC oscillator.

Following reset, the LPC546xx will operate from the Internal FRO until switched by software. This allows systems to operate without any external crystal and the boot loader code to operate at a known frequency. See Figure 11 and Figure 12 for an overview of the LPC546xx clock generation.

7.12.2 System PLL (PLL0)

The system PLL accepts an input clock frequency in the range of 32.768 kHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.3 USB PLL (PLL1)

The USB PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

7.12.4 Audio PLL (PLL2)

The audio PLL accepts an input clock frequency in the range of 1 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO).

The PLL can be enabled or disabled by software.

Table 9 shows wake-up sources for reduced power modes.

Table 9. Wake-up sources for reduced power modes

Power mode	Wake-up source	Conditions
Sleep	Any interrupt	Enable interrupt in NVIC.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.
Deep-sleep	Pin interrupts	Enable pin interrupts in NVIC and STARTER0 and/or STARTER1 registers.
	BOD interrupt	• Enable interrupt in NVIC and STARTER0 registers. • Enable interrupt in BODCTRL register. • Configure the BOD to keep running in this mode with the power API.
	BOD reset	Enable reset in BODCTRL register.
	Watchdog interrupt	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog interrupt in NVIC and STARTER0 registers. • Enable the watchdog in the WWDT MOD register and feed. • Enable interrupt in WWDT MOD register. • Configure the WDTOSC to keep running in this mode with the power API.
	Watchdog reset	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the watchdog and watchdog reset in the WWDT MOD register and feed.
	Reset pin	Always available.
	RTC 1 Hz alarm timer	• Enable the RTC 1 Hz oscillator in the RTCOSCCTRL register. • Enable the RTC bus clock in the AHBCLKCTRL0 register. • Start RTC alarm timer by writing a time-out value to the RTC COUNT register. • Enable the RTCALARM interrupt in the STARTER0 register.
	RTC 1 kHz timer time-out and alarm	• Enable the RTC 1 Hz oscillator and the RTC 1 kHz oscillator in the RTC CTRL register. • Start RTC 1 kHz timer by writing a value to the WAKE register of the RTC. • Enable the RTC wake-up interrupt in the STARTER0 register.
	Micro-tick timer (intended for ultra-low power wake-up from deep-sleep mode	• Enable the watchdog oscillator in the PDRUNCFG0 register. • Enable the Micro-tick timer clock by writing to the AHBCLKCTRL1 register. • Start the Micro-tick timer by writing UTICK CTRL register. • Enable the Micro-tick timer interrupt in the STARTER0 register.
	I2C interrupt	Interrupt from I2C in slave mode.
	SPI interrupt	Interrupt from SPI in slave mode.
	USART interrupt	Interrupt from USART in slave or 32 kHz mode.
	USB0 need clock interrupt	Interrupt from USB0 when activity is detected that requires a clock.
	USB1 need clock interrupt	Interrupt from USB1 when activity is detected that requires a clock.
	Ethernet interrupt	Interrupt from ethernet.
	DMA interrupt	Interrupt from DMA.
	HWWAKE	Certain Flexcomm Interface and DMIC subsystem activity.

7.17.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.17.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC546xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

8. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)	on pin VDD	[2]	-0.5	+4.6	V
V_{DDA}	analog supply voltage	on pin VDDA		-0.5	+4.6	V
V_{BAT}	battery supply voltage	on pin VBAT		-0.5	+4.6	V
V_{ref}	reference voltage	on pin VREFP	-	-0.5	+4.6	V
V_I	input voltage	only valid when the V_{DD} > 1.8 V; 5 V tolerant I/O pins	[6][7]	-0.5	+5.0	V
		on I2C open-drain pins	[5]	-0.5	+5.0	V
		USB_DM, USB_DP pins		-0.5	+5.0	V
V_{IA}	analog input voltage	on digital pins configured for an analog function	[8][9]	-0.5	VDD	V
I_{DD}	supply current	per supply pin, 1.71 V ≤ V_{DD} < 2.7 V	[3]	-	200	mA
	supply current	per supply pin, 2.7 V ≤ V_{DD} < 3.6 V	[3]	-	300	mA
I_{SS}	ground current	per ground pin, 1.71 V ≤ V_{DD} < 2.7 V	[3]	-	200	mA
	ground current	per ground pin, 2.7 V ≤ V_{DD} < 3.6 V	[3]	-	300	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	100	mA
T_{stg}	storage temperature		[10]	-65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C

Table 10. Limiting values *…continued*
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$P_{tot(pack)}$	total power dissipation (per package)	LQFP208, based on package heat transfer, not device power consumption	[11]	-	1.2	W
		LQFP208, based on package heat transfer, not device power consumption	[12]	-	0.95	W
		LQFP100, based on package heat transfer, not device power consumption	[11]	-	0.82	W
		LQFP100, based on package heat transfer, not device power consumption	[12]	-	0.60	W
		TFBGA180, based on package heat transfer, not device power consumption	[11]	-	0.95	W
		TFBGA180, based on package heat transfer, not device power consumption	[13]	-	1.2	W
		TFBGA100, based on package heat transfer, not device power consumption	[11]	-	0.57	W
		TFBGA100, based on package heat transfer, not device power consumption	[13]	-	0.65	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	-	2000	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in Table 21.

[2] Maximum/minimum voltage above the maximum operating voltage (see Table 21) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.

[3] The peak current is limited to 25 times the corresponding maximum current.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[5] V_{DD} present or not present. Compliant with the I^2C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.

[6] Applies to all 5 V tolerant I/O pins except true open-drain pins.

[7] Including the voltage on outputs in 3-state mode.

[8] An ADC input voltage above 3.6 V can be applied for a short time without leading to immediate, unrecoverable failure. Accumulated exposure to elevated voltages at 4.6 V must be less than 10^6 s total over the lifetime of the device. Applying an elevated voltage to the ADC inputs for a long time affects the reliability of the device and reduces its lifetime.

9. Thermal characteristics

The average chip junction temperature, T_j (°C), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature (°C),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance (°C/W)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD}. The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 11. Thermal resistance

Symbol	Parameter	Conditions	Max/Min	Unit
LQFP208 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	33 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	41 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		16 ± 15 %	°C/W
LQFP100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	48 ± 15 %	°C/W
		Single-layer (4.5 in × 3 in); still air	65 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		19 ± 15 %	°C/W
TFBGA180 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	41 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	33 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		14 ± 15 %	°C/W
TFBGA100 Package				
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in × 4 in); still air	69 ± 15 %	°C/W
		8-layer (4.5 in × 3 in); still air	60 ± 15 %	°C/W
$R_{th(j-c)}$	thermal resistance from junction to case		10 ± 15 %	°C/W

10. Static characteristics

10.1 General operating conditions

Table 12. General operating conditions

T_{amb} = −40 °C to +105 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_{clk}	CPU clock frequency		[3]	-	-	220	MHz
	CPU clock frequency	For USB high-speed device and host operations	[3]	60	-	220	MHz
	CPU clock frequency	For USB full-speed device and host operations	[3]	12	-	220	MHz
		For OTP programming only		-	-	12	MHz
V_{DD}	supply voltage (core and external rail)			1.71	-	3.6	V
		For OTP programming only	[2]	2.7	-	3.6	V
		For USB operation only		3.0	-	3.6	V
V_{DDA}	analog supply voltage			1.71	-	3.6	V
V_{BAT}	battery supply voltage			1.71	-	3.6	V
V_{refp}	ADC positive reference voltage	$V_{DDA} \geq 2$ V		2.0	-	V_{DDA}	V
		$V_{DDA} < 2$ V		V_{DDA}	-	V_{DDA}	V
T_{amb}	Temperature	For EEPROM operation		−40.0	-	+85	°C
RTC oscillator pins							
$V_{i(rtcx)}$	32.768 kHz oscillator input voltage	on pin RTCXIN		-0.5	-	+3.6	V
$V_{o(rtcx)}$	32.768 kHz oscillator output voltage	on pin RTCXOUT		-0.5	-	+3.6	V
$V_{i(xtal)}$	crystal input voltage	on pin XTALIN		−0.5	-	1.95	V
$V_{o(xtal)}$	crystal output voltage	on pin XTALOUT		−0.5	-	1.95	V

[1] Typical ratings are not guaranteed. The values listed are for room temperature (25 °C), nominal supply voltages.

[2] Attempting to program below 2.7 V will result in unpredictable results and the part might enter an unrecoverable state.

[3] The LPC5460x/61x operates at CPU frequencies of up to 180 MHz. The LPC54628 operates at CPU frequencies of up to 220 MHz.

10.2 Power-up ramp conditions

Table 13. Power-up characteristics[1]

T_{amb} = −40 °C to +105 °C.

Symbol	Parameter		Min	Typ	Max	Unit
t_{wd}	Window duration (time where $V_1 < V_{DD} < V_2$)		-	-	170	µs
V_1	Window low voltage	[2]	1.4	-	-	V
V_2	Window high voltage	[3]	-	-	1.62	V

[1] Assert the external reset pin until V_{DD} is > 1.62 V if the power-up characteristic specification cannot be implemented.

[2] V_{DD} to stay above V_1 for the entire duration t_{wd}.

[3] Tested in production. VDD = 1.71 V. At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage.

Table 17. Static characteristics: Power consumption in deep-sleep and deep power-down modes

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max[3]	Unit
I_{DD}	supply current	Deep-sleep mode; Flash is powered down					
		SRAMX (32 KB) powered T_{amb} = 25 °C		-	23	69	μA
		SRAMX (32 KB) powered T_{amb} = 105 °C		-	-	1150	μA
		Deep power-down mode					
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 25 °C*		-	464	1500	nA
		RTC oscillator input grounded (RTC oscillator disabled) *T_{amb} = 105 °C*		-	-	42	μA
		RTC oscillator running with external crystal VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	550	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C), VDD = 3.3 V.

[2] Characterized through bench measurements using typical samples.

[3] Tested in production, VDD = 3.6 V.

Table 18. Static characteristics: Power consumption in deep power-down mode

T_{amb} = −40 °C to +105 °C, unless otherwise specified, 2.7 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1][2]	Max	Unit
I_{BAT}	battery supply current	deep power-down mode; RTC oscillator running with external crystal					
		VDD = VDDA= VREFP = 3.3 V, VBAT = 3.0 V		-	0	-	nA
		VDD = VDDA= VREFP = 0 V or tied to ground, VBAT = 3.0 V		-	340[3]	-	nA

[1] Typical ratings are not guaranteed. Typical values listed are at room temperature (25 °C).

[2] Characterized through bench measurements using typical samples.

[3] If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage.

11.4 Wake-up process

Table 25. Dynamic characteristic: Typical wake-up times from low power modes
V_{DD} = 3.3 V;T_{amb} = 25 °C; using FRO as the system clock.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{wake}	wake-up time	from sleep mode	[2][3]	-	2.0	-	µs
		from deep-sleep mode; SRAMx powered. SRAM0, SRAM1, SRAM2, SRAM3, and USB SRAM powered down.	[2][5]	-	150	-	µs
		from deep power-down mode; RTC disabled; using $\overline{\text{RESET}}$ pin.	[4][5]	-	1.2	-	ms

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The wake-up time measured is the time between when a GPIO input pin is triggered to wake the device up from the low power modes and from when a GPIO output pin is set in the interrupt service routine (ISR) wake-up handler.

[3] FRO enabled, all peripherals off. PLL disabled.

[4] RTC disabled. Wake up from deep power-down causes the part to go through entire reset process. The wake-up time measured is the time between when the $\overline{\text{RESET}}$ pin is triggered to wake the device up and when a GPIO output pin is set in the reset handler.

[5] FRO disabled.

Table 28. Dynamic characteristics: Dynamic external memory interface, read strategy bits (RD bits) = 01 [2]

C_L = 10 pF balanced loading on all pins, T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V. Max EMC clock = 100 MHz. Input slew = 1 ns; SLEW set to fast-mode. Parameters sampled at the 90 % and 10 % level of the rising or falling edge. Excluding delays introduced by external device and PCB. Values based on simulation. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbol	Parameter		Min	Typ	Max	Unit
For RD = 1						
Common to read and write cycles						
$T_{cy(clk)}$	clock cycle time	[1]	10	-	-	ns
$t_{d(SV)}$	chip select valid delay time		-	-	t_{cmddly} + 3.7	ns
$t_{h(S)}$	chip select hold time		t_{cmddly} + 1.7	-	-	ns
$t_{d(RASV)}$	row address strobe valid delay time		-	-	t_{cmddly} + 4.1	ns
$t_{h(RAS)}$	row address strobe hold time		t_{cmddly} + 1.8	-	-	ns
$t_{d(CASV)}$	column address strobe valid delay time		-	-	t_{cmddly} + 4.4	ns
$t_{h(CAS)}$	column address strobe hold time		t_{cmddly} + 1.9	-	-	ns
$t_{d(WV)}$	write valid delay time		-	-	t_{cmddly} + 5.1	ns
$t_{h(W)}$	write hold time		t_{cmddly} + 2.4	-	-	ns
$t_{d(AV)}$	address valid delay time		-	-	t_{cmddly} + 4.8	ns
$t_{h(A)}$	address hold time		t_{cmddly} + 1.7	-	-	ns
Read cycle parameters						
$t_{su(D)}$	data input set-up time		0.5	-	-	ns
$t_{h(D)}$	data input hold time		2.1	-	-	ns
Write cycle parameters						
$t_{d(QV)}$	data output valid delay time		-	-	8.1	ns
$t_{h(Q)}$	data output hold time		−1.7	-	-	ns

[1] Refers to SDRAM clock signal EMC_CLKOUTn where n = 0 and 1.

[2] See Table 30 for internal programmable delay.

Table 38. Dynamic characteristic: oscillator *…continued*
T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V.[1]

Symbol	Parameter	Conditions		Min	Typ[2]	Max	Unit
High-frequency mode (20 - 25 MHz)[5]							
$t_{jit(per)}$	period jitter time	20 MHz crystal	[3]	-	4.3	-	ps
		25 MHz crystal		-	3.7	-	ps

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Indicates RMS period jitter.

[4] Select Low Frequency range = 0 in the SYSOSCCTRL register.

[5] Select High Frequency = 1 in the SYSOSCCTRL register.

11.11 RTC oscillator

See Section 13.5 for connecting the RTC oscillator to an external clock source.

Table 39. Dynamic characteristic: RTC oscillator
T_{amb} = −40 °C to +105 °C; 1.71 ≤ V_{DD} ≤ 3.6[1]

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
f_i	input frequency	-		-	32.768	-	kHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

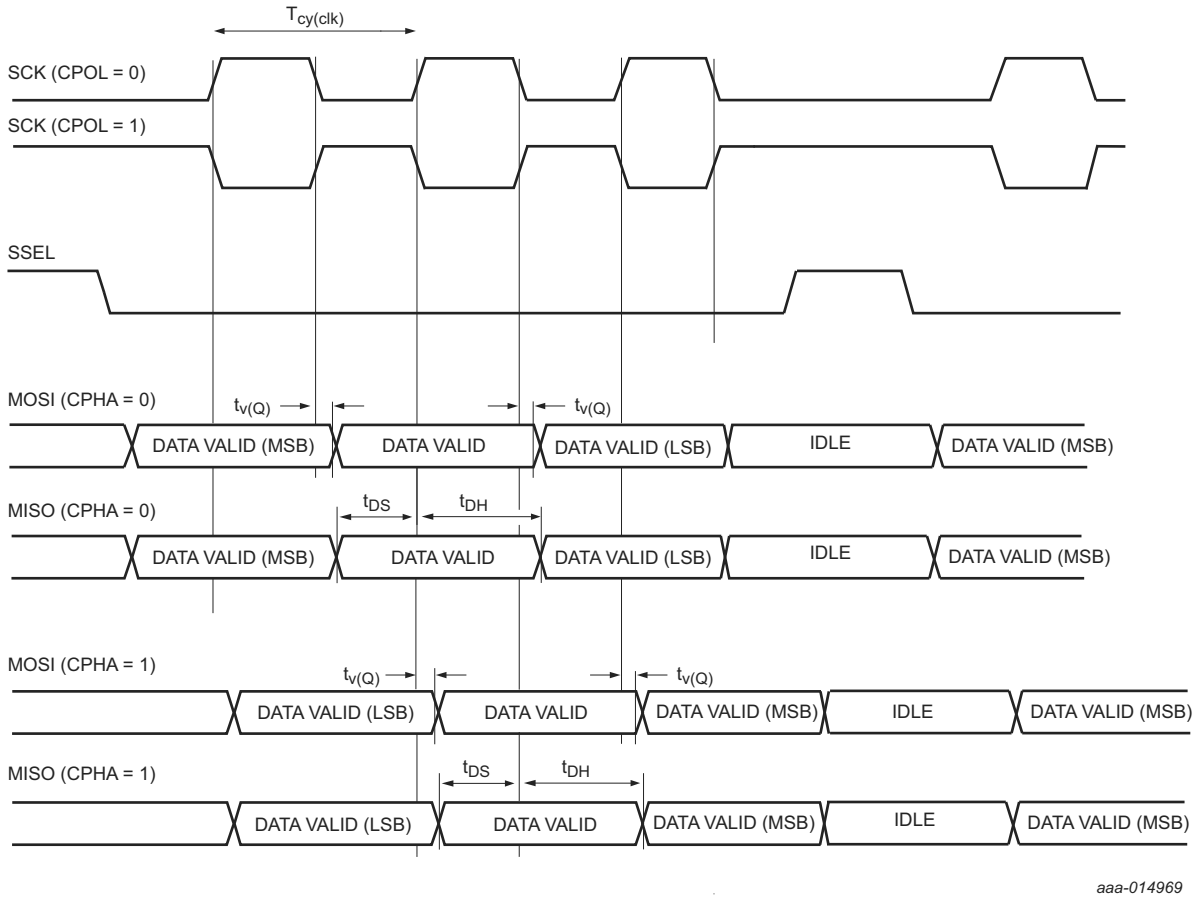


Fig 31. SPI master timing

11.19 USART interface

The actual USART bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.

Table 47. USART dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
USART master (in synchronous mode) 1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	21.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	19.7	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	0	-	4.9	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	4.5	ns
USART slave (in synchronous mode)1.71 V ≤ VDD ≤ 2.7 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.4	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	20.2	-	39.5	ns
		100 MHz < CCLK ≤ 180 MHz	19.3	-	37.7	ns
USART master (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	20.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	18.9	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	1.5	-	3.6	ns
		100 MHz < CCLK ≤ 180 MHz	1.3	-	3.2	ns
USART slave (in synchronous mode) 2.7 V ≤ VDD ≤ 3.6 V						
$t_{su(D)}$	data input set-up time	CCLK ≤ 100 MHz	1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1	-	-	ns
$t_{h(D)}$	data input hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	15.2	-	26.1	ns
		100 MHz < CCLK ≤ 180 MHz	14.3	-	24.2	ns

[1] Based on characterization; not tested in production.

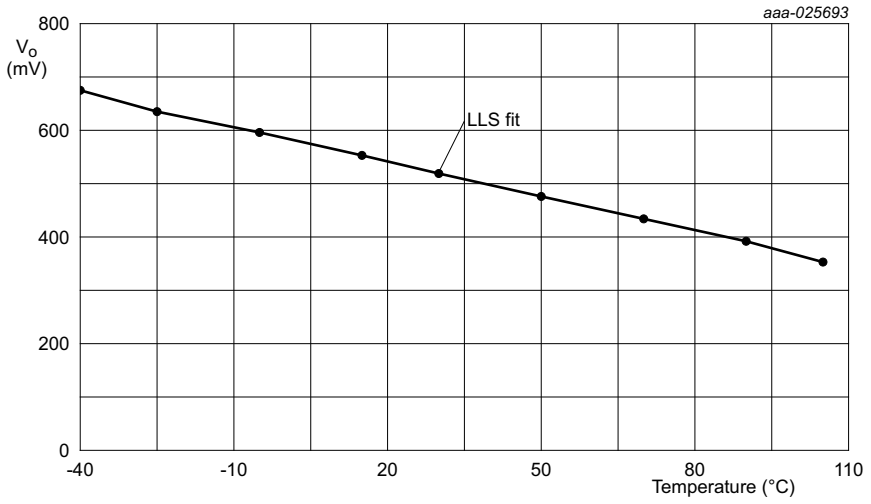
Table 57. Temperature sensor Linear-Least-Square (LLS) fit parameters

$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Fit parameter	Range		Min	Typ	Max	Unit
LLS slope	T_{amb} = −40 °C to +105 °C	[1]	-	−2.04	-	mV/°C
LLS intercept at 0 °C	T_{amb} = −40 °C to +105 °C	[1]	-	584.0	-	mV
Value at 30 °C		[2]	515.9	-	531.5	mV

[1] Measured over typical samples.

[2] Measured for samples over process corners.

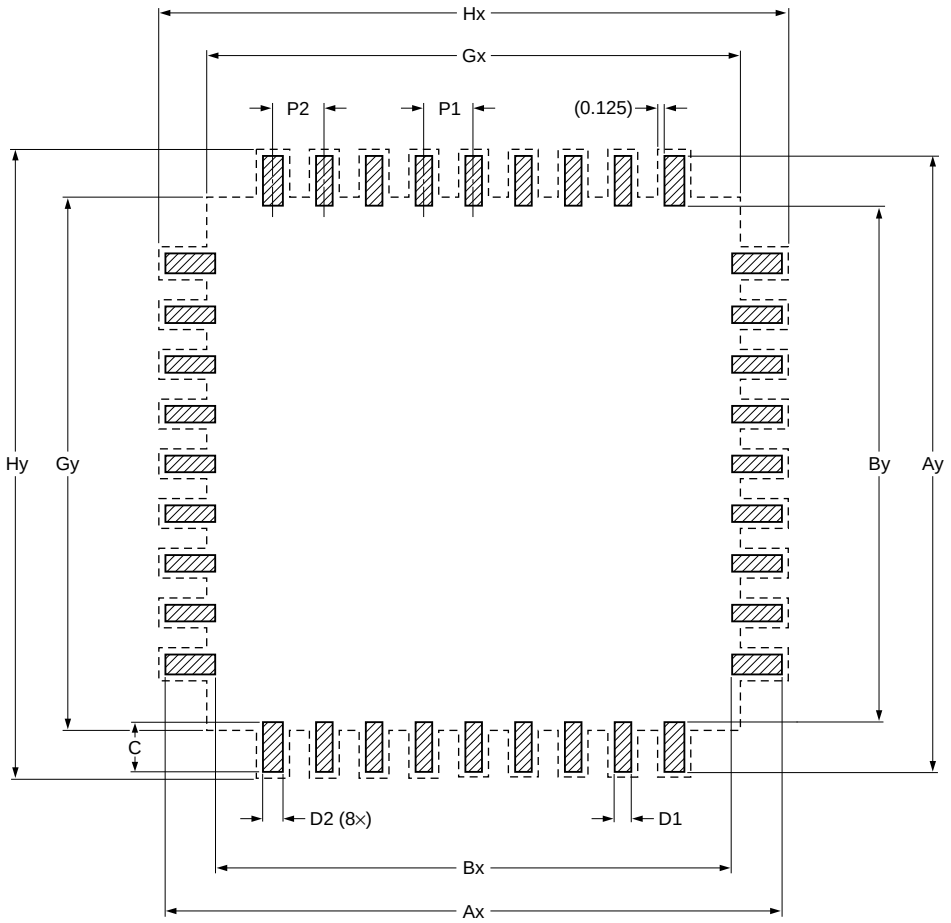


$V_{DD} = V_{DDA}$ 3.3 V; measured on matrix samples.

Fig 42. LLS fit of the temperature sensor output voltage

15. Soldering

Footprint information for reflow soldering of LQFP208 package **SOT459-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	31.300	31.300	28.300	28.300	1.500	0.280	0.400	28.500	28.500	31.550	31.550

sot459-1_fr

Fig 54. Reflow soldering of the LQFP208 package

18. Revision history

Table 60. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC546xx v.2.5	20180620	Product data sheet		LPC546xx v.2.4
Modifications:	• Updated Figure 14 “Typical CoreMark score (iterations/s/MHz) vs. Frequency (MHz) from flash and SRAMX” • Updated Table 14 “CoreMark score[1]”. • Updated Table 4 “Pin description”: Description of VREFN and VSSA. • Updated Table 5 “Termination of unused pins”: Added USB1_ID pin.			
LPC546xx v.2.4	20180524	Product data sheet	201805030I	LPC546xx v.2.3
Modifications:	• Added text to serial interfaces to Section 2 “Features and benefits”: USB 2.0 full-speed host/device controller with on-chip PHY and dedicated DMA controller supporting crystal-less operation in device mode using software library. See Technical note TN00032 for more details. • Added table note 2 of Section 6.2.2 “Pin states in different power modes”: If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage. • Added table note 3 to Table 18 “Static characteristics: Power consumption in deep power-down mode”: If VBAT> VDD, the external reset pin must be floating to prevent high VBAT leakage. • Added remark to Figure 16 “Deep-sleep mode: Typical supply current IDD versus temperature for different supply voltages VDD”: At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage. • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: I_{DD} supply current, Deep-sleep mode; Flash is powered down for SRAMX (32 KB) powered T_{amb} = 25 °C and T_{amb} = 105 °C; Max values: 69 μA and 1150 μA. Updated table note 3: Tested in production. VDD = 1.71 V. At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage. • Updated Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”: I_{DD} supply current, Deep-sleep mode; Flash is powered down for SRAMX (32 KB) powered T_{amb} = 25 °C; Max value: 69 μA.			
LPC546xx v.2.3	20180426	Product data sheet	-	LPC546xx v.2.2
Modifications:	• Updated Table 4 “Pin description”: VREFN and VSSA.			
LPC546xx v.2.2	20180417	Product data sheet	-	LPC546xx v.2.1
Modifications:	• Updated Table 25 “Dynamic characteristic: Typical wake-up times from low power modes”: Changed t_{wake} at typical for deep-sleep mode to 150 μs. Was 19 μs.			
LPC546xx v.2.1	20180206	Product data sheet	-	LPC546xx v.2.0
Modifications:	• Updated Figure 3 “LQFP100 package marking”. • Fixed Figure 4 “LPC546xx Block diagram” figure number identifier. • Fixed Figure 9 “LPC546xx Memory mapping” figure number identifier.			
LPC546xx v.2.0	20180126	Product data sheet	-	LPC546xx v.1.9

21. Contents

continued >>