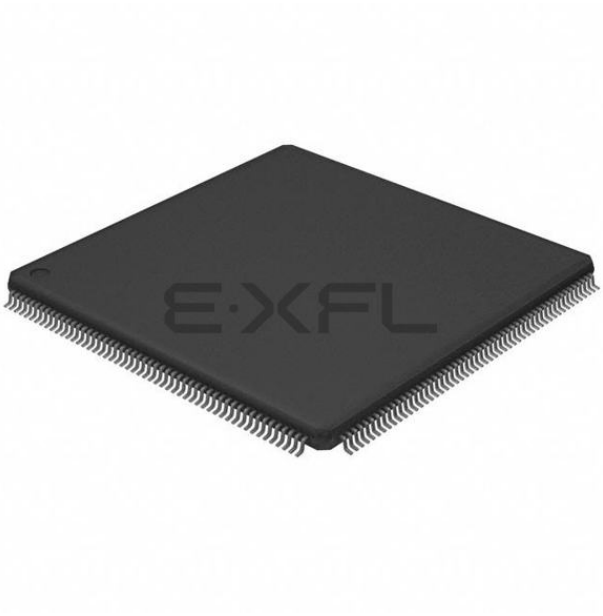

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	171
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54618j512bd208e

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC54605J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54605J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54605J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54605J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J256BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54606J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54606J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54606J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54607J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54607J256BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54608J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54608J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54616J256ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54616J512ET100	TFBGA100	plastic thin fine-pitch ball grid array package; 100 balls; body 9 × 9 × 0.7 mm	SOT926-1
LPC54616J512BD100	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1
LPC54616J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54618J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3
LPC54618J512BD208	LQFP208	plastic low profile quad flat package; 208 leads; body 28 × 28 × 1.4 mm	SOT459-1
LPC54628J512ET180	TFBGA180	thin fine-pitch ball grid array package; 180 balls; body 12 ´ 12 ´ 0.8 mm	SOT570-3

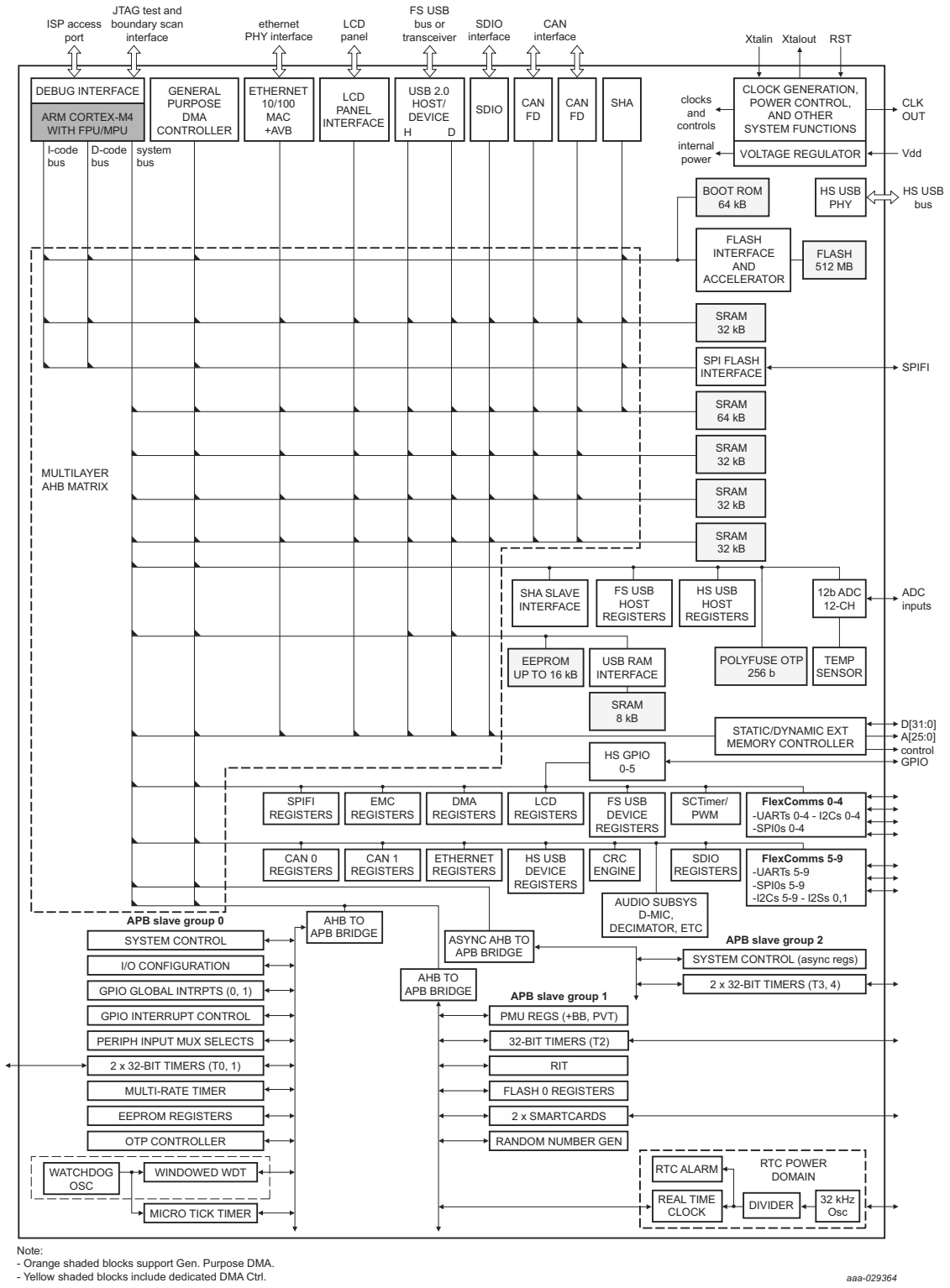


Fig 4. LPC546xx Block diagram

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_9	E10	G12	136	65	[2]	PU	I/O	**PIO0_9 —** General-purpose digital input/output pin.
							I/O	**FC3_SSEL2 —** Flexcomm 3: SPI slave select 2.
							O	**SD_POW_EN —** SD/MMC card power enable.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I/O	**SCI1_IO —** SmartCard Interface 1 data I/O.
							I/O	**EMC_D[7] —** External Memory interface data [7].
PIO0_10/ ADC0_0	J1	P2	50	23	[4]	PU	I/O; AI	**PIO0_10/ADC0_0 —** General-purpose digital input/output pin. ADC input channel 0 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_SCK —** Flexcomm 6: USART, SPI, or I2S clock.
							I	**CT2_CAP2 —** Capture input 2 to Timer 2.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**SWO —** Serial Wire Debug trace output.
PIO0_11/ ADC0_1	K1	L3	51	24	[4]	PU	I/O; AI	**PIO0_11/ADC0_1 —** General-purpose digital input/output pin. ADC input channel 1 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC6_RXD_SDA_MOSI_DATA —** Flexcomm 6: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
							O	**CT2_MAT2 —** Match output 2 from Timer 2.
							I	**FREQME_GPIO_CLK_A —** Frequency Measure pin clock input A.
								R — Reserved.
								R — Reserved.
							I	**SWCLK —** Serial Wire Debug clock. This is the default function after booting.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_12/ ADC0_2	J2	M3	52	25	[4]	PU	I/O; AI	**PIO0_12/ADC0_2 —** General-purpose digital input/output pin. ADC input channel 2 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC3_TXD_SCL_MISO —** Flexcomm 3: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
								R — Reserved.
							I/O	**SWDIO —** Serial Wire Debug I/O. This is the default function after booting.
PIO0_13	C10	F11	141	67	[3]	Z	I/O	**PIO0_13 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SDA function.
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0.
PIO0_14	D9	E13	144	69	[3]	Z	I/O	**PIO0_14 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 1 I2C SCL function.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**ENET_RXD1 —** Ethernet receive data 1.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_18	C9	C14	150	72	[2]	PU	I/O	**PIO0_18 —** General-purpose digital input/output pin.
							I/O	**FC4_CTS_SDA_SSEL0 —** Flexcomm 4: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							O	**SCT0_OUT1 —** SCTimer/PWM output 1.
							O	**SCI1_SCLK —** SmartCard Interface 1 clock.
							O	**EMC_A[0] —** External memory interface address 0.
PIO0_19	C5	C6	193	91	[2]	PU	I/O	**PIO0_19 —** General-purpose digital input/output pin.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
							O	**CT0_MAT2 —** Match output 2 from Timer 0.
							O	**SCT0_OUT2 —** SCTimer/PWM output 2.
								R — Reserved.
							O	**EMC_A[1] —** External memory interface address 1.
							I/O	**FC7_TXD_SCL_MISO_WS —** Flexcomm 7: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
PIO0_20	C8	D13	153	74	[2]	PU	I/O	**PIO0_20 —** General-purpose digital input/output pin.
							I/O	**FC3_CTS_SDA_SSEL0 —** Flexcomm 3: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**SCI0_IO —** SmartCard Interface 0 data I/O.
							O	**EMC_A[2] —** External memory interface address 2.
							I/O	**FC7_RXD_SDA_MOSI_DATA —** Flexcomm 7: USART receiver, I2C data I/O, SPI master-out/slave-in data, I2S data I/O.
PIO0_21	B9	C13	158	77	[2]	PU	I/O	**PIO0_21 —** General-purpose digital input/output pin.
							I/O	**FC3_RTS_SCL_SSEL1 —** Flexcomm 3: USART request-to-send, I2C clock, SPI slave select 1.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**SCI0_SCLK —** SmartCard Interface 0 clock.
							O	**EMC_A[3] —** External memory interface address 3.
							I/O	**FC7_SCK —** Flexcomm 7: USART, SPI, or I2S clock.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_2	-	C3	4	-	[2]	PU	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	-	C1	12	-	[2]	PU	I/O	**PIO2_5 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	-	F3	17	-	[2]	PU	I/O	**PIO2_6 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	-	J2	29	-	[2]	PU	I/O	**PIO2_7 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_D(1) —** SD/MMC data 1.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_5	-	E10	154	-	[2]	PU	I/O	**PIO4_5 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I	**SCT0_GPI6 —** Pin input 6 to SCTimer/PWM.
							O	**EMC_CKE[2] —** External memory interface SDRAM clock enable 2.
PIO4_6	-	D10	161	-	[2]	PU	I/O	**PIO4_6 —** General-purpose digital input/output pin.
								R — Reserved.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
							O	**EMC_CKE[3] —** External memory interface SDRAM clock enable 3.
PIO4_7	-	A14	166	-	[2][8]	PU	I/O	**PIO4_7 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CT4_CAP3 —** Capture input 3 to Timer 4.
							O	**USB0_PORTPWRN —** USB0 VBUS drive indicator (Indicates VBUS must be driven).
							O	**USB0_FRAME —** USB0 frame toggle signal.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
PIO4_8	-	B14	170	-	[2]	PU	I/O	**PIO4_8 —** General-purpose digital input/output pin.
							O	**ENET_TXD0 —** Ethernet transmit data 0.
							I/O	**FC2_SCK —** Flexcomm 2: USART or SPI clock.
							I	**USB0_OVERCURRENTN —** USB0 bus overcurrent indicator (active low).
							O	**USB0_LEDN —** USB0-configured LED indicator (active low).
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.

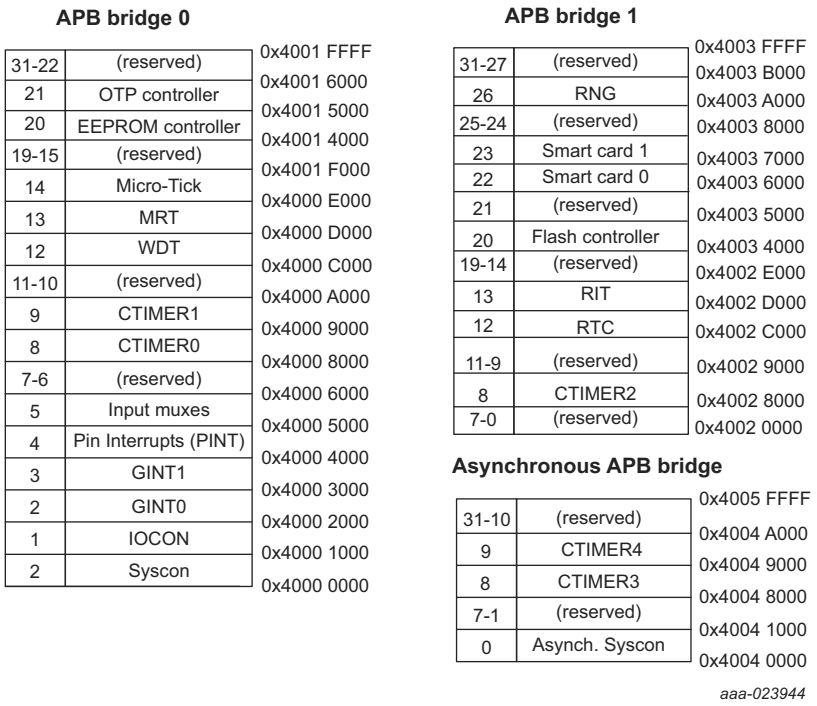


Fig 10. LPC546xx APB Memory map

7.12 System control

7.12.1 Clock sources

The LPC546xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.12.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.12.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

7.17.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.17.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC546xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

7.18.3.1 Features

- Read and write buffers to reduce latency and to improve performance.
- Low transaction latency.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- 8/16/32 data and 16/20/26 address lines wide static memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable Wait States.
  - Bus turnaround delay.
  - Output enable and write enable delays.
  - Extended wait.
- Dynamic memory interface support including single data rate SDRAM.
- 16 bit and 32 bit wide chip select SDRAM memory support.
- EMC bus width (bit) on LQFP100 and TFBGA100 packages supports up to 8/16 data line wide static memory, in addition to dynamic memories, such as, SDRAM (2 banks only) with an SDRAM clock of up to 100 MHz.
- Four chip selects for synchronous memory and four chip selects for static memory devices.
- Power-saving modes dynamically control EMC_CKE and EMC_CLK outputs to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2048 (A0 to A10), 4096 (A0 to A11), and 8192 (A0 to A12) row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

[9] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

[10] Dependent on package type.

[11] JEDEC (4.5 in × 4 in); still air.

[12] Single layer (4.5 in × 3 in); still air.

[13] 8-layer (4.5 in × 3 in); still air.

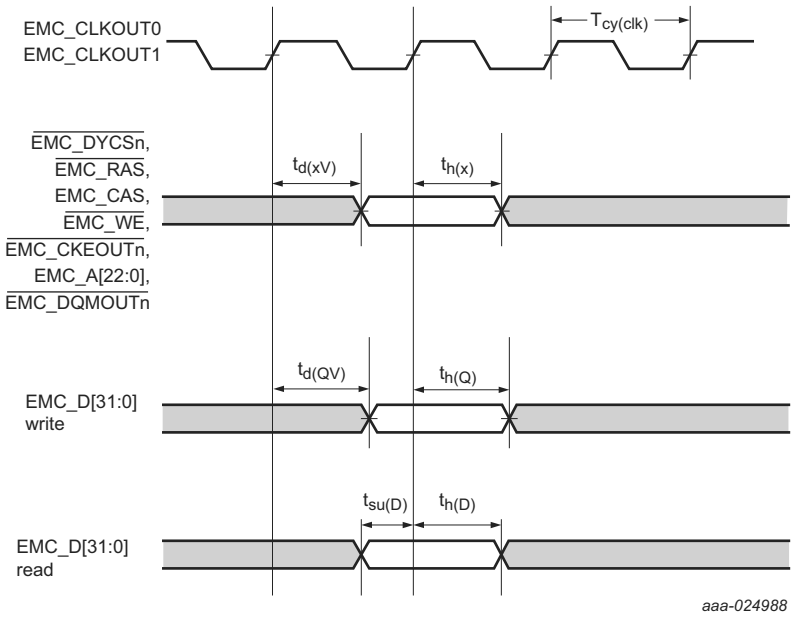


Fig 27. Dynamic external memory interface signal timing

Table 30. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY)

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}	delay time	b00000	0.41	0.66	0.77	ns
		b00001	0.52	0.85	1.03	ns
		b00010	0.69	1.11	1.3	ns
		b00011	0.8	1.3	1.56	ns
		b00100	0.95	1.53	1.77	ns
		b00101	1.06	1.72	2.03	ns
		b00110	1.23	1.98	2.3	ns
		b00111	1.34	2.17	2.56	ns
		b01000	1.45	2.3	2.67	ns
		b01001	1.56	2.49	2.93	ns
		b01010	1.73	2.75	3.2	ns
		b01011	1.84	2.94	3.46	ns
		b01100	1.99	3.17	3.67	ns
		b01101	2.1	3.36	3.93	ns
		b01110	2.27	3.62	4.2	ns
		b01111	2.38	3.81	4.46	ns
		b10000	2.45	3.86	4.46	ns
		b10001	2.56	4.05	4.72	ns
		b10010	2.73	4.31	4.99	ns
		b10011	2.84	4.5	5.25	ns
		b10100	2.99	4.73	5.46	ns
		b10101	3.1	4.92	5.72	ns
		b10110	3.27	5.18	5.99	ns
		b10111	3.38	5.37	6.25	ns
		b11000	3.49	5.5	6.36	ns
		b11001	3.6	5.69	6.62	ns
		b11010	3.77	5.95	6.89	ns
		b11011	3.88	6.14	7.15	ns
		b11100	4.03	6.37	7.36	ns
		b11101	4.14	6.56	7.62	ns
		b11110	4.31	6.82	7.89	ns
		b11111	4.42	7.01	8.15	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC546xx. user manual* for details.

11.6 System PLL (PLL0)

Table 31. PLL lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL0 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]			96	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	2.0	mA
PLL0 configuration: input frequency 32 kHz; output frequency 100 MHz							
$t_{lock(PLL0)}$	PLL0 lock time		[1]	-	-	108	µs
$I_{DD(PLL0)}$	PLL0 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 32. Dynamic characteristics of the PLL0[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			32.768 kHz	-	25 MHz	
Clock output							
f_o	output frequency	for PLL0 clkout output	[2]	4.3	-	550	MHz
d_o	output duty cycle	for PLL0 clkout output		46	-	54	%
f_{CCO}	CCO frequency			275	-	550	MHz
Lock detector output							
$\Delta_{lock(PFD)}$	PFD lock criterion		[3]	1	2	4	ns
Dynamic parameters at f_{out} = f_{CCO} = 540 MHz; standard bandwidth settings							
$J_{rms\text{-}interval}$	RMS interval jitter	f_{ref} = 10 MHz	[4][5]	-	15	30	ps
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 10 MHz	[4][5]	-	40	80	ps

[1] Data based on characterization results, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] A phase difference between the inputs of the PFD (clkref and clkfb) smaller than the PFD lock criterion means lock output is HIGH.

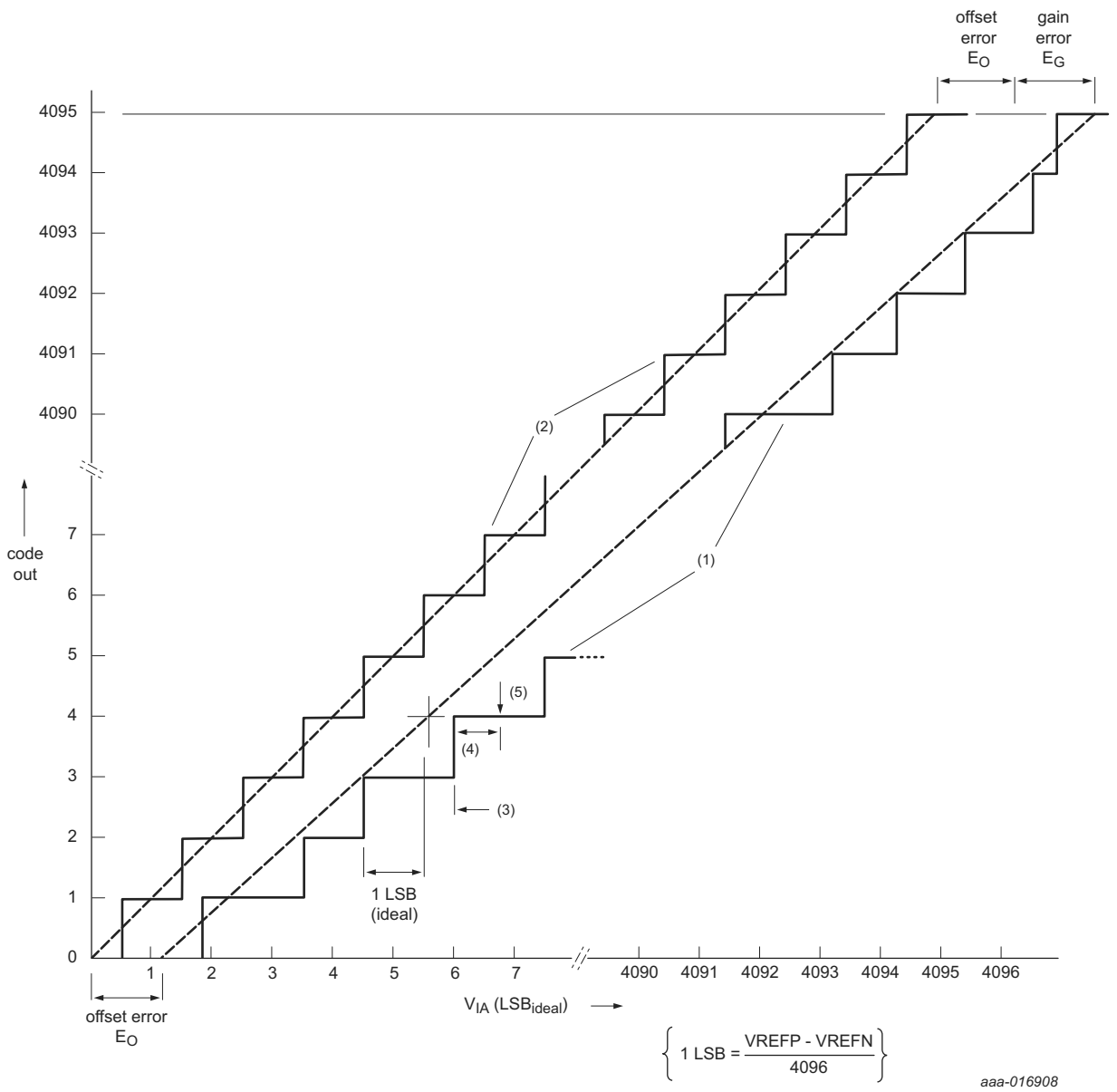
[4] Actual jitter dependent on amplitude and spectrum of substrate noise.

[5] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

[8] The full-scale error voltage or gain error (E_G) is the difference between the straight-line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 40.

[9] T_{amb} = 25 °C; maximum sampling frequency f_s = 5.0 Msamples/s and analog input capacitance C_{ia} = 5 pF.

[10] Input impedance Z_i is inversely proportional to the sampling frequency and the total input capacity including C_{ia} and C_{io}: $Z_i \propto 1 / (f_s \times C_i)$. See Table 21 for C_{io}. See Figure 41.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 40. 12-bit ADC characteristics

13.6 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 47.

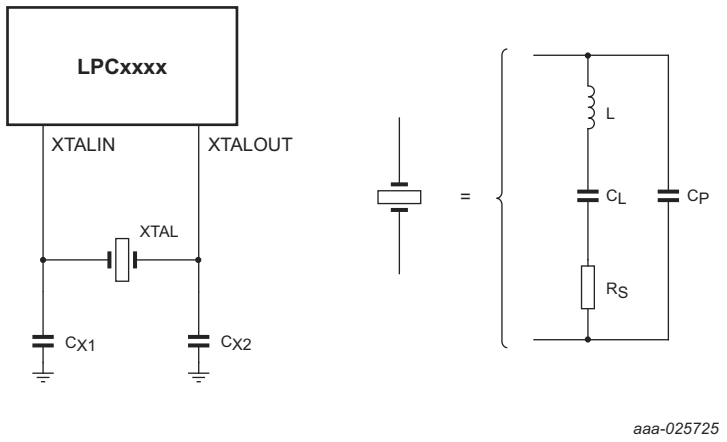


Fig 47. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

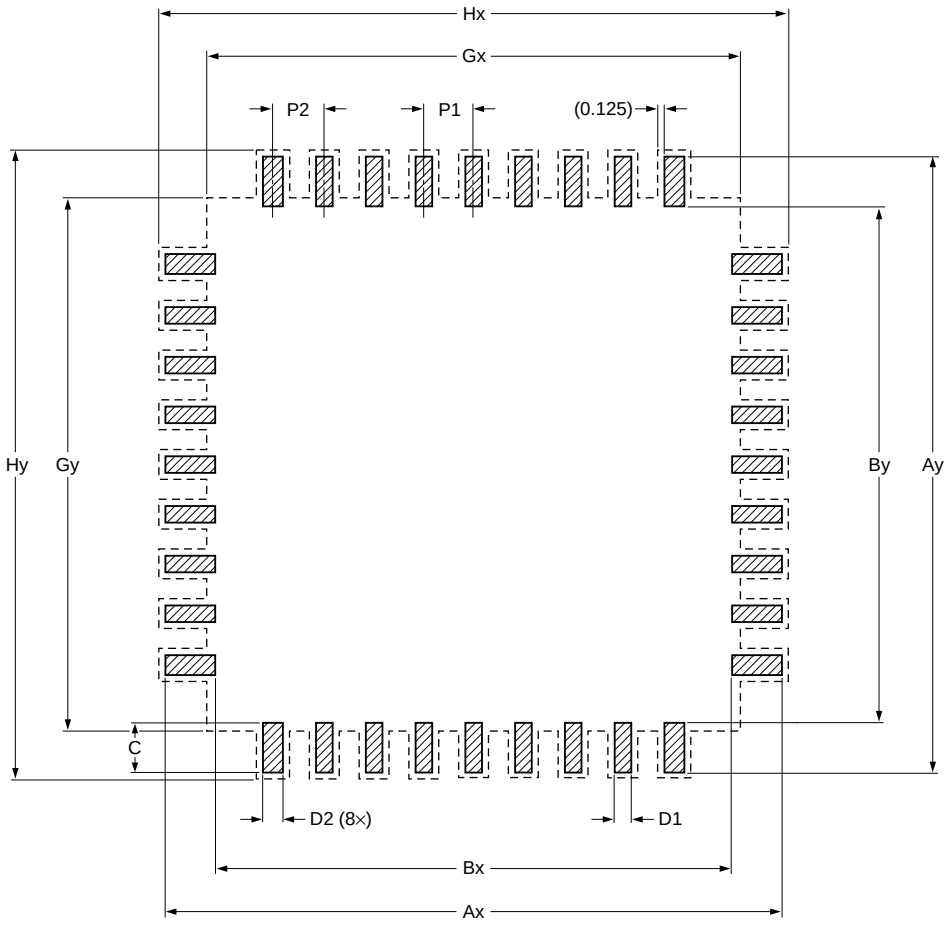
C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

Footprint information for reflow soldering of LQFP100 package **SOT407-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550

sot407-1

Fig 55. Reflow soldering of the LQFP100 package

16. Abbreviations

Table 59. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
API	Application Programming Interface
DMA	Direct Memory Access
FRO oscillator	Internal Free-Running Oscillator, tuned to the factory specified frequency
GPIO	General Purpose Input/Output
FRO	Free Running Oscillator
LSB	Least Significant Bit
MCU	MicroController Unit
PDM	Pulse Density Modulation
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
TCP/IP	Transmission Control Protocol/Internet Protocol
TTL	Transistor-Transistor Logic
USART	Universal Asynchronous Receiver/Transmitter

17. References

[1] LPC546xx. User manual UM10912.

[2] LPC546xx. Errata sheet.

[3] Technical note ADC design guidelines: http://www.nxp.com/documents/technical_note/TN00009.pdf

Table 60. Revision history *...continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC546xx v.1.5	20170331	Product data sheet	-	LPC546xx v.1.4
Modifications:	• Updated Table 51 “Dynamic characteristics: SD/MMC and SDIO”. The max clock frequency is 50 MHz. • Updated Section 7.18.2 “SD/MMC card interface”: Supports up to a maximum of 50 MHz of interface frequency. • Updated Table 41 “Dynamic characteristic: I2C-bus pins[1]” • Updated Figure 28 “I2S-bus timing (master)” and Figure 29 “I2S-bus timing (slave)”. • Updated Table 2 “Ordering options”. Parts LPC54618J512ET180 and LPC54618J512BD208 have Classic CAN. • Added Section 11.4 “Wake-up process”.			
LPC546xx v.1.4	20170307	Product data sheet	-	LPC5460x v.1.3
Modifications:	• Changed data sheet title to LPC546xx. • Updated Table 16 “Static characteristics: Power consumption in deep-sleep and deep power-down modes” and Table 17 “Static characteristics: Power consumption in deep-sleep and deep power-down modes”.			
LPC5460x v.1.3	20170224	Product data sheet	-	LPC5460x v.1.2
Modifications:	• Removed S parts. Data sheet title renamed to LPC5460x. • Removed AES-256 engine and SHA references throughout the document. • Security peripherals renamed to Security features. • Updated Section 4 “Marking”. • Updated Section 5 “Block diagram”. • Updated Figure 6 “LPC546xx Memory mapping”. • Updated Table 20 “Typical AHB/APB peripheral power consumption [3][4][5]”.			
LPC5460x v.1.2	20170206	Product data sheet	-	LPC5460x v.1.1
Modifications:	• Updated address range details and description of the address range: 0x8000 0000 to 0xDFFF FFFF: See Table 7 “Memory usage and details”: Static memory chip select: was 0x9000 0000 - 0x93 FFFF, now, 0x9000 0000 – 0x93FF FFFF. • Updated Figure 8 “LPC5460x clock generation”. • Updated Power control in Section 2 “Features and benefits”: Ultra-low power Micro-tick Timer, running from the Watchdog oscillator that can be used to wake up the device from low power modes. • Updated Table 4 “Pin description”: PIO0_26, USB0_IDVALUE, Type is Input (I). • Updated Section 7.18.1.1 “Features”. • Updated Table 31 “Dynamic characteristics of the PLL0[1]”: Input frequency, $F_{in,}$ Max value is 25 MHZ.			
LPC5460x v.1.1	20170124	Product data sheet	-	LPC5460x v.1

21. Contents

continued >>