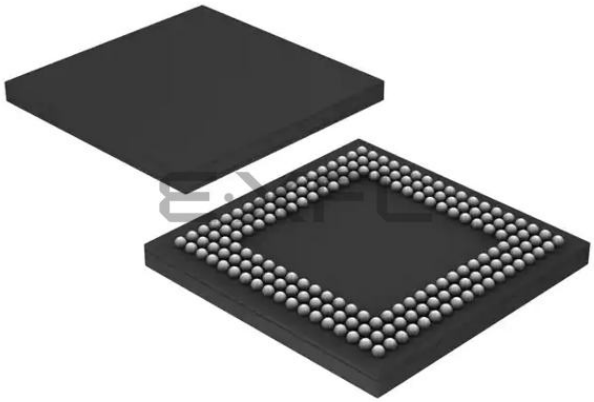


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	145
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54618j512et180e

5. Block diagram

Figure 4 shows the LPC546xx block diagram. In this figure, orange shaded blocks support general purpose DMA and yellow shaded blocks include dedicated DMA control.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_22	B8	B12	163	80	[2][8]	PU	I/O	**PIO0_22 —** General-purpose digital input/output pin.
							I/O	**FC6_TXD_SCL_MISO_WS —** Flexcomm 6: USART transmitter, I2C clock, SPI master-in/slave-out data I/O, I2S word-select/frame.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
								R — Reserved.
								R — Reserved.
							I	**USB0_VBUS —** Monitors the presence of USB0 bus power.
PIO0_23/ ADC0_11	K5	N7	71	35	[4]	PU	I/O; AI	**PIO0_23/ADC0_11 —** General-purpose digital input/output pin. ADC input channel 11 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							O	**CT3_MAT3 —** Match output 3 from Timer 3.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
								R — Reserved.
							I/O	**SPIFI_CSN —** SPI Flash Interface chip select (active low).
PIO0_24	J5	M7	76	38	[2]	PU	I/O	**PIO0_24 —** General-purpose digital input/output pin.
							I/O	**FC0_RXD_SDA_MOSI —** Flexcomm 0: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[0] —** SD/MMC data 0.
							I	**CT2_CAP0 —** Capture input 0 to Timer 2.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO0 —** Data bit 0 for the SPI Flash Interface.
PIO0_25	J6	K8	83	40	[2]	PU	I/O	**PIO0_25 —** General-purpose digital input/output pin.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[1] —** SD/MMC data 1.
							I	**CT2_CAP1 —** Capture input 1 to Timer 2.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
								R — Reserved.
							I/O	**SPIFI_IO1 —** Data bit 1 for the SPI Flash Interface.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO3_13	-	H4	75	-	[2]	PU	I/O	**PIO3_13 —** General-purpose digital input/output pin.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I/O	**FC9_CTS_SDA_SSEL0 —** Flexcomm 9: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
								R — Reserved.
								R — Reserved.
							I	**EMC_FBCK —** External memory interface feedback clock.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO3_14	-	E3	13	-	[2]	PU	I/O	**PIO3_14 —** General-purpose digital input/output pin.
							O	**SCT0_OUT4 —** SCTimer/PWM output 4.
							I/O	**FC9_RTS_SCL_SSEL1 —** Flexcomm 9: USART request-to-send, I2C clock, SPI slave select 1.
							O	**CT3_MAT1 —** Match output 1 from Timer 3.
								R — Reserved.
								R — Reserved.
								R — Reserved.
							O	**TRACEDATA[2] —** Trace data bit 2.
PIO3_15	-	D2	11	-	[2]	PU	I/O	**PIO3_15 —** General-purpose digital input/output pin.
							I/O	**FC8_SCK —** Flexcomm 8: USART or SPI clock.
							I	**SD_WR_PRT —** SD/MMC write protect.
PIO3_16	-	E1	19	-	[2]	PU	I/O	**PIO3_16 —** General-purpose digital input/output pin.
							I/O	**FC8_RXD_SDA_MOSI —** Flexcomm 8: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							I/O	**SD_D[4] —** SD/MMC data 4.
PIO3_17	-	K1	31	-	[2]	PU	I/O	**PIO3_17 —** General-purpose digital input/output pin.
							I/O	**FC8_TXD_SCL_MISO —** Flexcomm 8: USART transmitter, I2C clock, SPI master-in/slave-out data.
							I/O	**SD_D[5] —** SD/MMC data 5.
PIO3_18	-	M6	68	-	[2]	PU	I/O	**PIO3_18 —** General-purpose digital input/output pin.
							I/O	**FC8_CTS_SDA_SSEL0 —** Flexcomm 8: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[6] —** SD/MMC data 6.
							O	**CT4_MAT0 —** Match output 0 from Timer 4.
							O	**CAN0_TD —** Transmitter output for CAN 0.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_14	-	B5	194	-	[2]	PU	I/O	**PIO4_14 —** General-purpose digital input/output pin.
							I	**ENET_RX_CLK —** Ethernet Receive Clock (MII interface) or Ethernet Reference Clock (RMII interface).
							O	**CT4_MAT1 —** Match output 1 from Timer 4.
							I/O	**FC9_SCK —** Flexcomm 9: USART or SPI clock.
								R — Reserved.
							I	**SCT0_GPI7 —** Pin input 7 to SCTimer/PWM.
PIO4_15	-	A4	197	-	[2]	PU	I/O	**PIO4_15 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**CT4_MAT2 —** Match output 2 from Timer 4.
							I/O	**FC9_RXD_SDA_MOSI —** Flexcomm 9: USART receiver, I2C data I/O, SPI master-out/slave-in data.
PIO4_16	-	C4	203	-	[2]	PU	I/O	**PIO4_16 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**CT4_MAT3 —** Match output 3 from Timer 4.
							I/O	**FC9_TXD_SCL_MISO —** Flexcomm 9: USART transmitter, I2C clock, SPI master-in/slave-out data.
PIO4_17	-	-	6	-	[2]	PU	I/O	**PIO4_17 —** General-purpose digital input/output pin.
								R — Reserved.
							O	**CAN1_TD —** Transmitter output for CAN 1.
							I	**CT1_CAP2 —** Capture 2 input to Timer 1.
							I	**UTICK_CAP0 —** Micro-tick timer capture input 0.
								R — Reserved.
							O	**EMC_BLSN[2] —** External memory interface byte lane select 2 (active low).
PIO4_18	-	-	10	-	[2]	PU	I/O	**PIO4_18 —** General-purpose digital input/output pin.
								R — Reserved.
							I	**CAN1_RD —** Receiver input for CAN 1.
							I	**CT1_CAP3 —** Capture 3 input to Timer 1.
							I	**UTICK_CAP1 —** Micro-tick timer capture input 1.
								R — Reserved.
							O	**EMC_BLSN[3] —** External memory interface byte lane select 3 (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO4_23	-	-	42	-	[2]	PU	I/O	**PIO4_23 —** General-purpose digital input/output pin.
							I	**ENET_RXD0 —** Ethernet receive data 0.
							I	**SD_WR_PRT —** SD/MMC write protect.
							I/O	**FC2_CTS_SDA_SSEL0 —** Flexcomm 2: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT0 —** Match output 0 from Timer 1.
							I/O	**EMC_D[18] —** External Memory interface data [18].
PIO4_24	-	-	67	-	[2]	PU	I/O	**PIO4_24 —** General-purpose digital input/output pin.
							I	**ENET_RXD1 —** Ethernet receive data 1.
							I	**SD_CARD_INT_N —** Card interrupt line.
							I/O	**FC7_RTS_SCL_SSEL1 —** Flexcomm 7: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
							I/O	**EMC_D[19] —** External Memory interface data [19].
PIO4_25	-	-	69	-	[2]	PU	I/O	**PIO4_25 —** General-purpose digital input/output pin.
							I	**ENET_RXD2 —** Ethernet Receive Data 2 (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC7_CTS_SDA_SSEL0 —** Flexcomm 7: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
								R — Reserved.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
							I/O	**EMC_D[20] —** External Memory interface data [20].
PIO4_26	-	-	73	-	[2]	PU	I/O	**PIO4_26 —** General-purpose digital input/output pin.
							I	**ENET_RXD3 —** Ethernet Receive Data 3 (MII interface).
							I/O	**SD_D[1] —** SD/MMC data 1.
								R — Reserved.
							I	**UTICK_CAP2 —** Micro-tick timer capture input 2.
							O	**CT1_MAT3 —** Match output 3 from Timer 1.
							I/O	**EMC_D[21] —** External Memory interface data [21].

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO5_3	-	-	129	-	[2]	PU	I/O	**PIO5_3 —** General-purpose digital input/output pin.
							O	**ENET_MDC —** Ethernet management data clock.
							O	**SD_VOLT[2] —** SD/MMC card regulator voltage control [2].
							I	**CT3_CAP1 —** Capture input 1 to Timer 3.
							I/O	**FC4_RTS_SCL_SSEL1 —** Flexcomm 4: USART request-to-send, I2C clock, SPI slave select 1.
								R — Reserved.
							I/O	**EMC_D[30] —** External Memory interface data [30].
PIO5_4	-	-	135	-	[2]	PU	I/O	**PIO5_4 —** General-purpose digital input/output pin.
							I/O	**ENET_MDIO —** Ethernet management data I/O.
							O	**SD_BACKEND_PWR —** SD/MMC back-end power supply for embedded device.
							I	**CT3_CAP2 —** Capture input 2 to Timer 3.
							I/O	**FC4_SSEL2 —** Flexcomm 4: SPI slave select 2.
								R — Reserved.
							I/O	**EMC_D[31] —** External Memory interface data [31].
PIO5_5	-	-	145	-	[2]	PU	I/O	**PIO5_5 —** General-purpose digital input/output pin.
							I	**SCT0_GPI0 —** Pin input 0 to SCTimer/PWM.
							O	**PDM1_CLK —** Clock for PDM interface 1, for digital microphone.
							I	**CT3_CAP3 —** Capture input 3 to Timer 3.
							I/O	**FC4_SSEL3 —** Flexcomm 4: SPI slave select 3.
							O	**TRACECLK —** Trace clock.
							O	**EMC_A[21] —** External memory interface address 21.
PIO5_6	-	-	152	-	[2]	PU	I/O	**PIO5_6 —** General-purpose digital input/output pin.
							I	**SCT0_GPI1 —** Pin input 1 to SCTimer/PWM.
							I	**PDM1_DATA —** Data for PDM interface 1 (digital microphone).
							I/O	**FC5_SCK —** Flexcomm 5: USART or SPI clock.
							O	**SCT0_OUT5 —** SCTimer/PWM output 5.
							O	**TRACEDATA[0] —** Trace data bit 0.
							O	**EMC_A[22] —** External memory interface address 22.

Table 7. Memory usage and details *…continued*

Address range	General Use	Address range details and description	
0x8000 0000 to 0xDFFF FFFF	Off-chip Memory via the External Memory Controller	Four static memory chip selects:	
		0x8000 0000 - 0x83FF FFFF	Static memory chip select 0 (up to 64 MB)[1]
		0x8800 0000 - 0x8BFF FFFF	Static memory chip select 1 (up to 64 MB)[2]
		0x9000 0000 – 0x93FF FFFF	Static memory chip select 2 (up to 64 MB)
		0x9800 0000 - 0x9BFF FFFF	Static memory chip select 3 (up to 64 MB)
		Four dynamic memory chip selects:	
		0xA000 0000 - 0xA7FF FFFF	Dynamic memory chip select 0 (up to 256MB)
		0xA800 0000 - 0xAFFF FFFF	Dynamic memory chip select 1 (up to 256MB)
		0xB000 0000 - 0xB7FF FFFF	Dynamic memory chip select 2 (up to 256MB)
		0xB800 0000 - 0xBFFF FFFF	Dynamic memory chip select 3 (up to 256MB)
0xE000 0000 to 0xE00F FFFF	Cortex-M4 Private Peripheral Bus	0xE000 0000 - 0xE00F FFFF	Cortex-M4 related functions, includes the NVIC and System Tick Timer.

[1] Can be up to 256 MB, upper address 0x8FFF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *UM10912* LPC546xx *user manual*.

[2] Can be up to 128 MB, upper address 0x97FF FFFF, if the address shift mode is enabled. See the EMCSYSCTRL register bit 0 in the *UM10912* LPC546xx *user manual*.

Figure 9 shows the overall map of the entire address space from the user program viewpoint following reset.

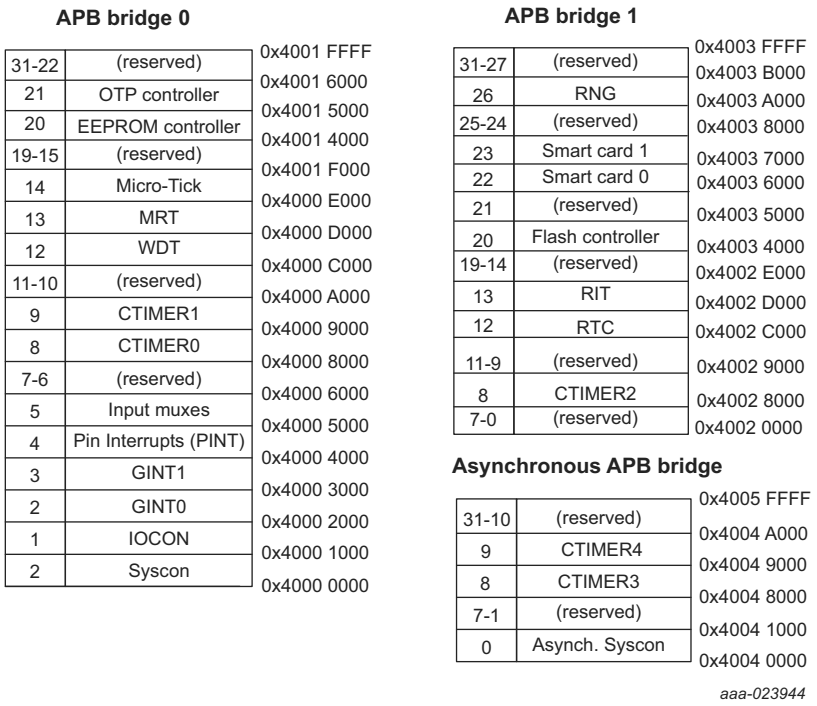


Fig 10. LPC546xx APB Memory map

7.12 System control

7.12.1 Clock sources

The LPC546xx supports one external and two internal clock sources:

- Free Running Oscillator (FRO).
- Watchdog oscillator (WDOSC).
- Crystal oscillator.

7.12.1.1 Free Running Oscillator (FRO)

The FRO 12 MHz oscillator provides the default clock at reset and provides a clean system clock shortly after the supply pins reach operating voltage.

- 12 MHz internal FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.
- Selectable 48 MHz or 96 MHz FRO oscillator, factory trimmed for accuracy, that can optionally be used as a system clock as well as other purposes.

7.12.1.2 Watchdog oscillator (WDOSC)

The watchdog oscillator is a low-power internal oscillator. The WDOSC can be used to provide a clock to the WWDT and to the entire chip. The low-power watchdog oscillator provides a selectable frequency in the range of 6 kHz to 1.5 MHz. The accuracy of this clock is limited to ± 40% over temperature, voltage, and silicon processing variations.

7.17.8.4 USART

Features

- Maximum bit rates of 6.25 Mbit/s in asynchronous mode.
- The maximum supported bit rate for USART master synchronous mode is 24 Mbit/s, and the maximum supported bit rate for USART slave synchronous mode is 12.5 Mbit/s.
- 7, 8, or 9 data bits and 1 or 2 stop bits.
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare.
- RS-485 transceiver output enable.
- Autobaud mode for automatic baud rate detection
- Parity generation and checking: odd, even, or none.
- Software selectable oversampling from 5 to 16 clocks in asynchronous mode.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator with auto-baud function.
- A fractional rate divider is shared among all USARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Loopback mode for testing of data and flow control.
- In synchronous slave mode, wakes up the part from deep-sleep mode.
- Special operating mode allows operation at up to 9600 baud using the 32.768 kHz RTC oscillator as the UART clock. This mode can be used while the device is in deep-sleep mode and can wake-up the device when a character is received.
- USART transmit and receive functions work with the system DMA controller.

7.17.8.5 I^2S-bus interface

The I^2S bus provides a standard communication interface for streaming data transfer applications such as digital audio or data collection. The I^2S bus specification defines a 3-wire serial bus, having one data, one clock, and one word select/frame trigger signal, providing single or dual (mono or stereo) audio data transfer as well as other configurations. In the LPC546xx, the I^2S function is included in Flexcomm Interface 6 and Flexcomm Interface 7. Each of the Flexcomm Interface implements four I^2S channel pairs.

The I^2S interface within one Flexcomm Interface provides at least one channel pair that can be configured as a master or a slave. Other channel pairs, if present, always operate as slaves. All of the channel pairs within one Flexcomm Interface share one set of I^2S

registers. All other blocks are disabled and no code accessing the peripheral is executed. The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, 96 MHz and 180MHz.

Table 19. Typical peripheral power consumption[1][2]

V_{DD} = 3.3 V; T_{amb} = 25 °C

Peripheral	I_{DD} in uA
FRO	100
WDT OSC	2.0
Flash	200
BOD	2.0
SYSOSC	247

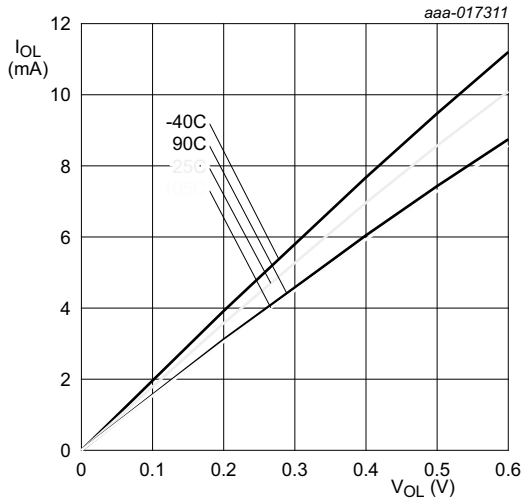
[1] The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using PDRUNCFG0/1 registers. All other blocks are disabled and no code accessing the peripheral is executed.

[2] Typical ratings are not guaranteed. Characterized through bench measurements using typical samples.

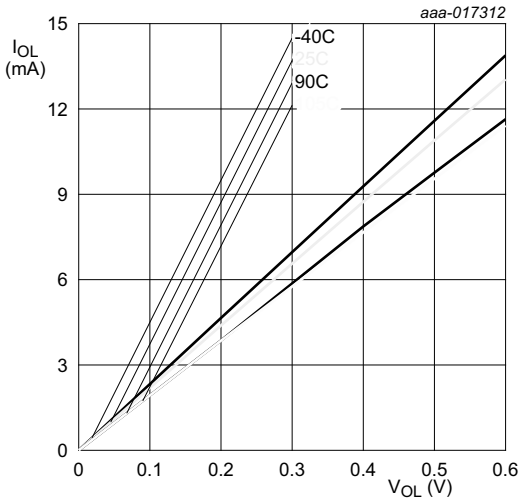
Table 20. Typical AHB/APB peripheral power consumption [3][4][5]

T_{amb} = 25 °C, V_{DD} = 3.3 V;

Peripheral		I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz	I_{DD} in uA/MHz
AHB peripheral		**CPU: 12 MHz, sync APB bus: 12 MHz**	**CPU: 48 MHz, sync APB bus: 48 MHz**	**CPU: 96 MHz, sync APB bus: 96 MHz**	**CPU: 180 MHz, sync APB bus: 180 MHz**	**CPU: 220 MHz, sync APB bus: 220 MHz**
USB0 device		0.3	0.3	0.3	0.4	0.5
USB1 device		4.4	4.4	4.4	5.0	6.5
DMIC		0.2	0.2	0.2	0.2	0.3
GPIO0	[1]	0.9	0.9	0.9	1.0	1.4
GPIO1	[1]	0.8	0.8	0.8	1.0	1.4
GPIO2	[1]	1.0	1.0	1.0	1.1	1.4
GPIO3	[1]	1.1	1.1	1.1	1.3	1.7
GPIO4	[1]	1.0	1.0	1.0	1.2	1.6
GPIO5	[1]	0.7	0.7	0.7	0.8	1.1
DMA		0.7	0.7	0.7	0.8	1.1
CRC		1.0	1.0	1.0	1.0	1.4
ADC0		1.6	1.6	1.6	1.9	2.6
SCTimer/PWM		4.5	4.5	4.5	5.3	7.0
Ethernet AVB		24.0	24.0	24.0	28.0	38.0
LCD		13.0	13.0	13.0	15.0	19.0
EEPROM		1.1	1.1	1.1	1.2	1.6
EMC		39.0	39.0	39.0	45.4	60.1
CAN0		10.8	10.8	10.8	12.6	16.5
CAN1		10.7	10.7	10.7	12.4	16.4
SD/MMC		7.9	7.9	7.9	9.3	12.3
Flexcomm Interface 0 (USART, SPI, I^2C)		1.6	1.6	1.6	1.9	2.5

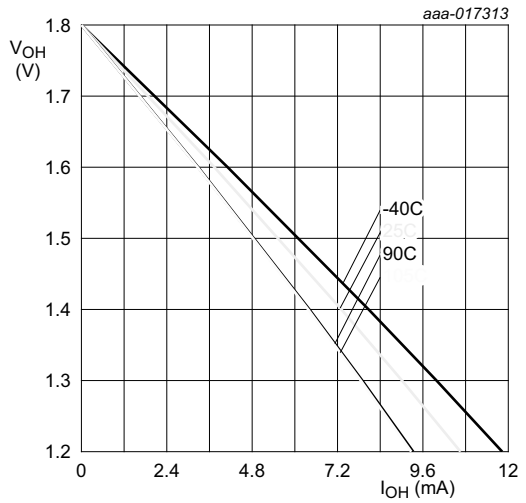


Conditions: V_{DD} = 1.8 V; on standard port pins.

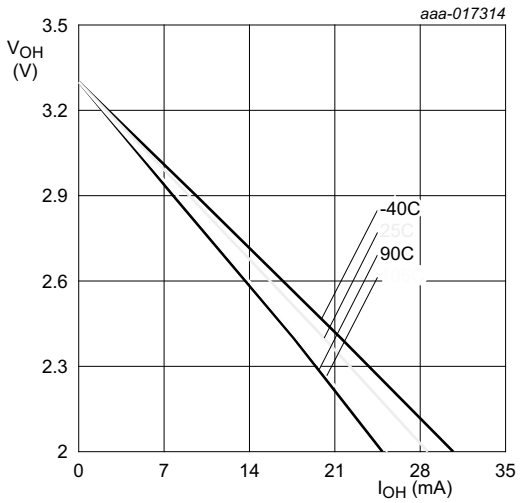


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 20. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 21. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

11. Dynamic characteristics

11.1 Flash memory

Table 22. Flash characteristics

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
N_{endu}	endurance	sector erase/program	[1]	10000	-	-	cycles
		page erase/program; page in a sector		1000	-	-	cycles
t_{ret}	retention time	powered		10	-	-	years
		unpowered		10	-	-	years
t_{er}	erase time	page, sector, or multiple consecutive sectors		-	100	-	ms
t_{prog}	programming time		[2]	-	1	-	ms

[1] Number of erase/program cycles.

[2] Programming times are given for writing 256 bytes from RAM to the flash.

11.2 EEPROM

Table 23. EEPROM characteristics

T_{amb} = −40 °C to +85 °C; V_{DD} = 1.71 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency			800	1500	1600	kHz
N_{endu}	endurance			100000	-	-	cycles
t_{ret}	retention time	T_{amb} = −40 °C to +85 °C		20	-	-	years
t_a	access time	read		-	100	-	ns
		erase/program; f_{clk} = 1500 kHz		-	1.99	-	ms
		erase/program; f_{clk} = 1600 kHz		-	1.87	-	ms
t_{wait}	wait time	read; RPHASE1	[1]	70	-	-	ns
		read; RPHASE2	[1]	35	-	-	ns
		write; PHASE1	[1]	20	-	-	ns
		write; PHASE2	[1]	40	-	-	ns
		write; PHASE3	[1]	10	-	-	ns

[1] See the LPC546xx. user manual, UM10912 on how to program the wait states for the different read (RPHASEx) and erase/program phases (PHASEx).

Remark: EEPROM is not accessible in deep-sleep and deep power-down modes

11.3 I/O pins

Table 24. Dynamic characteristic: I/O pins[1]

T_{amb} = −40 °C to +105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Standard I/O pins - normal drive strength							
t_r	rise time	pin configured as output; SLEW = 1 (Fast-mode);	[2][3]				
		2.7 V ≤ V_{DD} <= 3.6 V		1.0	-	2.5	ns
		1.71 V ≤ V_{DD} <= 1.98 V		1.6	-	3.8	ns
t_f	fall time	pin configured as output; SLEW = 1 (Fast-mode);	[2][3]				
		2.7 V ≤ V_{DD} <= 3.6 V		0.9	-	2.5	ns
		1.71 V ≤ V_{DD} <= 1.98 V		1.7	-	4.1	ns
t_r	rise time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.3	ns
		1.71 V ≤ V_{DD} ≤ 1.98 V		2.9	-	7.8	ns
t_f	fall time	pin configured as output; SLEW = 0 (standard mode);	[2][3]				
		2.7 V ≤ V_{DD} ≤ 3.6 V		1.9	-	4.0	ns
		1.71 V ≤ V_{DD} ≤ 1.98 V		2.7	-	6.7	ns
t_r	rise time	pin configured as input	[4]	0.3	-	1.3	ns
t_f	fall time	pin configured as input	[4]	0.2	-	1.2	ns

[1] Simulated data, not tested in production.

[2] Simulated using 10 cm of 50 Ω PCB trace with 5 pF receiver input. Rise and fall times measured between 80 % and 20 % of the full output signal level.

[3] The slew rate is configured in the IOCON block the SLEW bit. See the LPC546xx user manual.

[4] C_L = 20 pF. Rise and fall times measured between 90 % and 10 % of the full input signal level.

Table 30. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY)

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}	delay time	b00000	0.41	0.66	0.77	ns
		b00001	0.52	0.85	1.03	ns
		b00010	0.69	1.11	1.3	ns
		b00011	0.8	1.3	1.56	ns
		b00100	0.95	1.53	1.77	ns
		b00101	1.06	1.72	2.03	ns
		b00110	1.23	1.98	2.3	ns
		b00111	1.34	2.17	2.56	ns
		b01000	1.45	2.3	2.67	ns
		b01001	1.56	2.49	2.93	ns
		b01010	1.73	2.75	3.2	ns
		b01011	1.84	2.94	3.46	ns
		b01100	1.99	3.17	3.67	ns
		b01101	2.1	3.36	3.93	ns
		b01110	2.27	3.62	4.2	ns
		b01111	2.38	3.81	4.46	ns
		b10000	2.45	3.86	4.46	ns
		b10001	2.56	4.05	4.72	ns
		b10010	2.73	4.31	4.99	ns
		b10011	2.84	4.5	5.25	ns
		b10100	2.99	4.73	5.46	ns
		b10101	3.1	4.92	5.72	ns
		b10110	3.27	5.18	5.99	ns
		b10111	3.38	5.37	6.25	ns
		b11000	3.49	5.5	6.36	ns
		b11001	3.6	5.69	6.62	ns
		b11010	3.77	5.95	6.89	ns
		b11011	3.88	6.14	7.15	ns
		b11100	4.03	6.37	7.36	ns
		b11101	4.14	6.56	7.62	ns
		b11110	4.31	6.82	7.89	ns
		b11111	4.42	7.01	8.15	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC546xx. user manual* for details.

11.14 I²S-bus interface

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Common to master and slave							
t_{WH}	pulse width HIGH	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
t_{WL}	pulse width LOW	on pins I2Sx_TX_SCK and I2Sx_RX_SCK[5]					
		CCLK ≤ 100 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
		100 MHz < CCLK ≤ 180 MHz		$(T_{cyc}/2)-1$	-	$(T_{cyc}/2)+1$	ns
Master; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		26.0	-	40.3	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.0	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		26.0	-	41.0	ns
		100 MHz < CCLK ≤ 180 MHz		25.0	-	39.6	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		6.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		6.4	-	-	ns
Slave; 1.71 V ≤ VDD < 2.7 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		18.8	-	37.1	ns
		100 MHz < CCLK ≤ 180 MHz		18.0	-	35.5	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.8	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.4	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		3.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.2	-	-	ns

Table 42. Dynamic characteristics: I²S-bus interface pins [1][4]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1.0 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
Master; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		21.4	-	30.4	ns
		100 MHz < CCLK ≤ 180 MHz		20.6	-	28.7	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		21.1	-	29	ns
		100 MHz < CCLK ≤ 180 MHz		20.3	-	28.3	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		1.3	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.0	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		2.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		3.3	-	-	ns
Slave; 2.7 V ≤ VDD ≤ 3.6 V							
$t_{v(Q)}$	data output valid time	on pin I2Sx_TX_SDA	[2]				
		CCLK ≤ 100 MHz		13.8	-	23.6	ns
		100 MHz < CCLK ≤ 180 MHz		13	-	21.9	ns
$t_{su(D)}$	data input set-up time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		4.7	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.2	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		0.9	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0.7	-	-	ns
$t_{h(D)}$	data input hold time	on pin I2Sx_RX_SDA	[2]				
		CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
		on pin I2Sx_WS					
		CCLK ≤ 100 MHz		1.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.3	-	-	ns

[1] Based on characterization; not tested in production.

[2] Clock Divider register (DIV) = 0x0.

[3] Typical ratings are not guaranteed.

[4] The Flexcomm Interface function clock frequency should not be above 48 MHz. See the data rates section in the I²S chapter (UM10912) to calculate clock and sample rates.

[5] Based on simulation. Not tested in production.

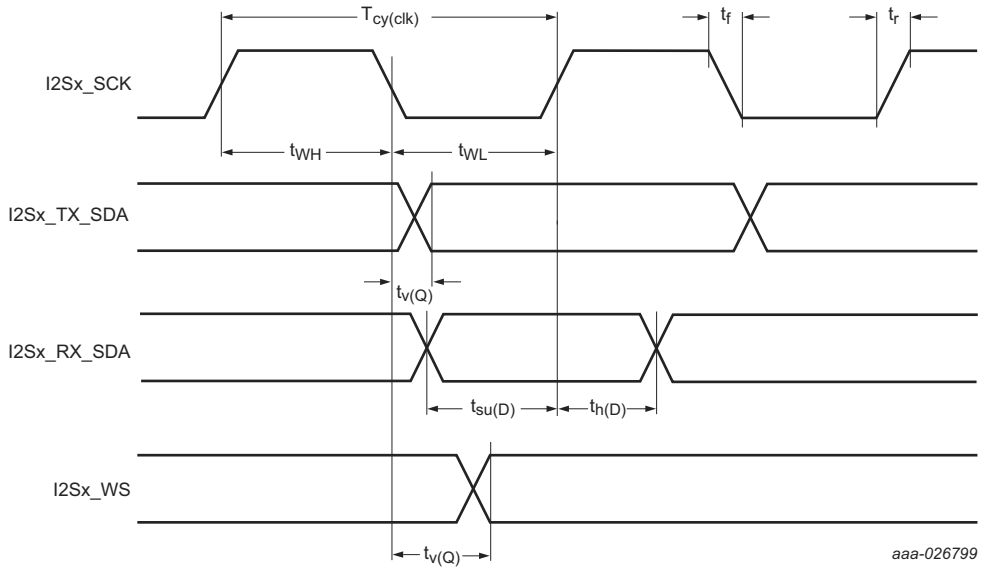


Fig 29. I²S-bus timing (master)

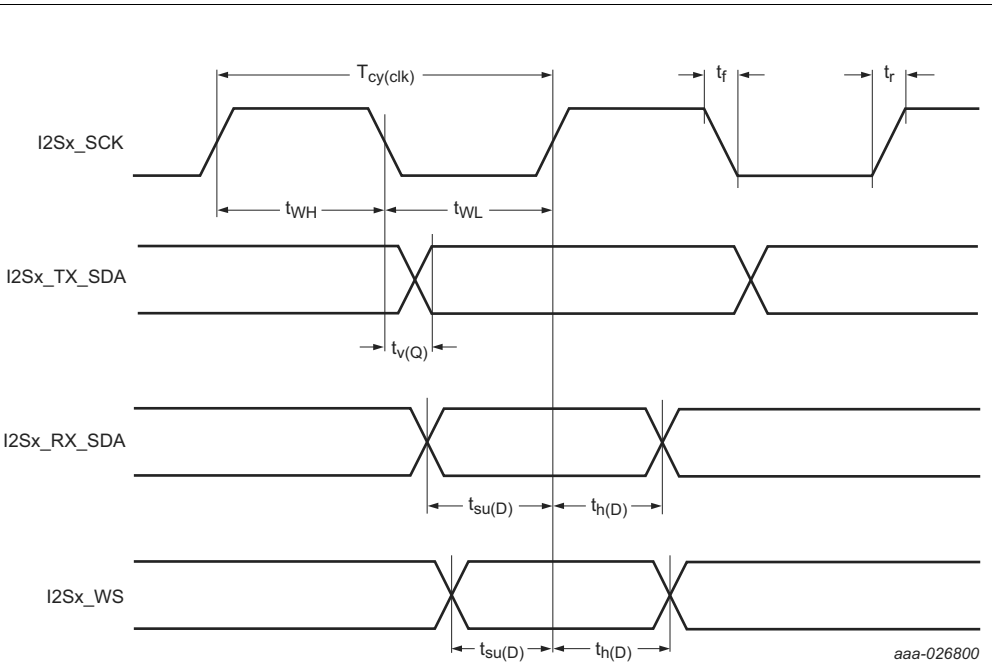


Fig 30. I²S-bus timing (slave)

11.18 Smart card interface

Table 46. Dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; V_{DD} = 1.71 V to 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins; Parameters sampled at the 90 % and 10 % level of the rising or falling edge.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
2.7 V ≤ VDD ≤ 3.6 V						
t_{DS}	data set-up time	CCLK ≤ 100 MHz	2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	2.1	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz	0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz	11.0	-	22.5	ns
		100 MHz < CCLK ≤ 180 MHz	11.0	-	22.5	ns

[1] Based on simulated values. V_{DD} = 2.7 V - 3.6 V.

Table 55. ADC sampling times[1]

-40 °C ≤ T_{amb} <= 85 °C; 1.71 V ≤ V_{DDA} ≤ 3.6 V; 1.71 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	20	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		23	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		26	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		31	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		47	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		75	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 10 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	15	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		18	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		20	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		24	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		38	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		62	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 8 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	12	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		13	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		15	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		19	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		30	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		48	-	-	ns
ADC inputs ADC_5 to ADC_0 (fast channels); ADC resolution = 6 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	9	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		10	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		11	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		13	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		22	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		36	-	-	ns
ADC inputs ADC_11 to ADC_6 (slow channels); ADC resolution = 12 bit							
t_s	sampling time	Z_o < 0.05 kΩ	[3]	43	-	-	ns
		0.05 kΩ <= Z_o < 0.1 kΩ		46	-	-	ns
		0.1 kΩ <= Z_o < 0.2 kΩ		50	-	-	ns
		0.2 kΩ <= Z_o < 0.5 kΩ		56	-	-	ns
		0.5 kΩ <= Z_o < 1 kΩ		74	-	-	ns
		1 kΩ <= Z_o < 5 kΩ		105	-	-	ns

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.