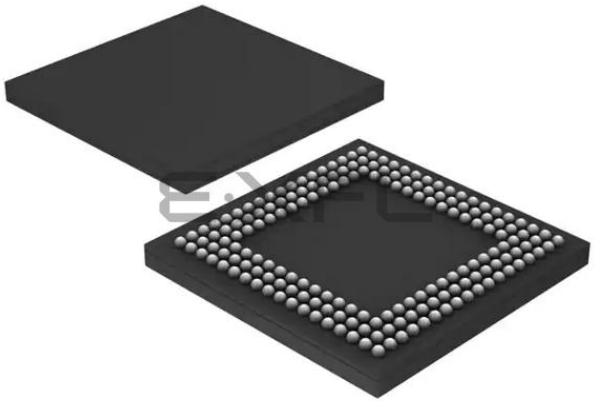

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	220MHz
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	145
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc54628j512et180e

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO0_30	A2	A2	200	95	[2]	PU	I/O	**PIO0_30 —** General-purpose digital input/output pin. **Remark:** In ISP mode, this pin is set to the Flexcomm 0 USART TXD function.
							I/O	**FC0_TXD_SCL_MISO —** Flexcomm 0: USART transmitter, I2C clock, SPI master-in/slave-out data.
								R — Reserved.
							O	**CT0_MAT0 —** Match output 0 from Timer 0.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							O	**TRACEDATA[1] —** Trace data bit 1.
PIO0_31/ ADC0_5	K3	M5	55	28	[4]	PU	I/O; AI	**PIO0_31/ADC0_5 —** General-purpose digital input/output pin. ADC input channel 5 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_CTS_SDA_SSEL0 —** Flexcomm 0: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							I/O	**SD_D[2] —** SD/MMC data 2.
							O	**CT0_MAT1 —** Match output 1 from Timer 0.
							O	**SCT0_OUT3 —** SCTimer/PWM output 3.
							O	**TRACEDATA[0] —** Trace data bit 0.
PIO1_0/ ADC0_6	J3	N3	56	29	[4]	PU	I/O; AI	**PIO1_0/ADC0_6 —** General-purpose digital input/output pin. ADC input channel 6 if the DIGIMODE bit is set to 0 in the IOCON register for this pin.
							I/O	**FC0_RTS_SCL_SSEL1 —** Flexcomm 0: USART request-to-send, I2C clock, SPI slave select 1.
							I/O	**SD_D[3] —** SD/MMC data 3.
							I	**CT0_CAP2 —** Capture 2 input to Timer 0.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							O	**TRACECLK —** Trace clock.
PIO1_1	J10	K12	109	55	[2]	PU	I/O	**PIO1_1/ —** General-purpose digital input/output pin.
							I/O	**FC3_RXD_SDA_MOSI —** Flexcomm 3: USART receiver, I2C data I/O, SPI master-out/slave-in data.
								R — Reserved.
							I	**CT0_CAP3 —** Capture 3 input to Timer 0.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
								R — Reserved.
							I	**USB1_OVERCURRENTN —** USB1 bus overcurrent indicator (active low).

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO2_2	-	C3	4	-	[2]	PU	I/O	**PIO2_2 —** General-purpose digital input/output pin.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface) or Ethernet Carrier Sense/Data Valid (RMII interface).
							I/O	**FC3_SSEL3 —** Flexcomm 3: SPI slave select 3.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**CT1_MAT1 —** Match output 1 from Timer 1.
PIO2_3	-	B1	7	-	[2]	PU	I/O	**PIO2_3 —** General-purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							O	**SD_CLK —** SD/MMC clock.
							I/O	**FC1_RXD_SDA_MOSI —** Flexcomm 1: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**CT2_MAT0 —** Match output 0 from Timer 2.
PIO2_4	-	D3	9	-	[2]	PU	I/O	**PIO2_4 —** General-purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							I/O	**SD_CMD —** SD/MMC card command I/O.
							I/O	**FC1_TXD_SCL_MISO —** Flexcomm 1: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**CT2_MAT1 —** Match output 1 from Timer 2.
PIO2_5	-	C1	12	-	[2]	PU	I/O	**PIO2_5 —** General-purpose digital input/output pin.
							O	**ENET_TX_ER —** Ethernet Transmit Error (MII interface).
							O	**SD_POW_EN —** SD/MMC card power enable
							I/O	**FC1_CTS_SDA_SSEL0 —** Flexcomm 1: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**CT1_MAT2 —** Match output 2 from Timer 1.
PIO2_6	-	F3	17	-	[2]	PU	I/O	**PIO2_6 —** General-purpose digital input/output pin.
							I	**ENET_TX_CLK —** Ethernet Transmit Clock (MII interface).
							I/O	**SD_D[0] —** SD/MMC data 0.
							I/O	**FC1_RTS_SCL_SSEL1 —** Flexcomm 1: USART request-to-send, I2C clock, SPI slave select 1.
							I	**CT0_CAP0 —** Capture input 0 to Timer 0.
PIO2_7	-	J2	29	-	[2]	PU	I/O	**PIO2_7 —** General-purpose digital input/output pin.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							I/O	**SD_D(1) —** SD/MMC data 1.
							I	**FREQME_GPIO_CLK_B —** Frequency Measure pin clock input B.
							I	**CT0_CAP1 —** Capture input 1 to Timer 0.

Table 4. Pin description *…continued*

Symbol	100-pin, TFBGA	180-pin, TFBGA	208-pin, LQFP	100-pin, LQFP		Reset state [1]	Type	Description
PIO5_7	-	-	171	-	[2]	PU	I/O	**PIO5_7 —** General-purpose digital input/output pin.
							I	**SCT0_GPI2 —** Pin input 2 to SCTimer/PWM.
							I/O	**MCLK —** MCLK input or output for I2S and/or digital microphone.
							I/O	**FC5_RXD_SDA_MOSI —** Flexcomm 5: USART receiver, I2C data I/O, SPI master-out/slave-in data.
							O	**SCT0_OUT6 —** SCTimer/PWM output 6.
							O	**TRACEDATA[1] —** Trace data bit 1.
							O	**EMC_A[23] —** External memory interface address 23.
PIO5_8	-	-	175	-	[2]	PU	I/O	**PIO5_8 —** General-purpose digital input/output pin.
							I	**SCT0_GPI3 —** Pin input 3 to SCTimer/PWM.
							O	**PDM0_CLK —** Clock for PDM interface 0, for digital microphone.
							I/O	**FC5_TXD_SCL_MISO —** Flexcomm 5: USART transmitter, I2C clock, SPI master-in/slave-out data.
							O	**SCT0_OUT7 —** SCTimer/PWM output 7.
							O	**TRACEDATA[2] —** Trace data bit 2.
							O	**EMC_A[24] —** External memory interface address 24.
PIO5_9	-	-	179	-	[2]	PU	I/O	**PIO5_9 —** General-purpose digital input/output pin.
							I	**SCT0_GPI4 —** Pin input 4 to SCTimer/PWM.
							I	**PDM0_DATA —** Data for PDM interface 0 (digital microphone).
							I/O	**FC5_CTS_SDA_SSEL0 —** Flexcomm 5: USART clear-to-send, I2C data I/O, SPI Slave Select 0.
							O	**SCT0_OUT8 —** SCTimer/PWM output 8.
							O	**TRACEDATA[3] —** Trace data bit 3.
							O	**EMC_A[25] —** External memory interface address 25.
PIO5_10	-	-	168	-	[2]	PU	I/O	**PIO5_10 —** General-purpose digital input/output pin.
							I	**SCT0_GPI5 —** Pin input 5 to SCTimer/PWM.
								R — Reserved.
							I/O	**FC5_RTS_SCL_SSEL1 —** Flexcomm 5: USART request-to-send, I2C clock, SPI slave select 1.
							O	**SCT0_OUT9 —** SCTimer/PWM output 9.
							I	**UTICK_CAP3 —** Micro-tick timer capture input 3.
USB1_AVSSC	D1	F2	20	6				USB1 analog 3.3 V ground.
USB1_REXT	B1	F1	21	7				USB1 analog signal for reference resistor, 12.4 kΩ +/-1%
USB1_ID	C1	G1	22	8				Indicates to the transceiver whether connected as an A-device (USB1_ID LOW) or B-device (USB1_ID HIGH).
USB1_VBUS	D3	G2	23	9	[6][8]		I/O	VBUS pin (power on USB cable).

[1] PU = input mode, pull-up enabled (pull-up resistor pulls up pin to V_{DD}). Z = high impedance; pull-up or pull-down disabled, AI = analog input, I = input, O = output, F = floating. Reset state reflects the pin state at reset without boot code operation. For pin states in the different power modes, see Section 6.2.2 “Pin states in different power modes”. For termination on unused pins, see Section 6.2.1 “Termination of unused pins”.

[2] 5 V tolerant pad with programmable glitch filter (5 V tolerant if V_{DD} present; if V_{DD} not present, do not exceed 3.6 V); provides digital I/O functions with TTL levels and hysteresis; normal drive strength. See Figure 44. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 16 ns (simulated value).

[3] True open-drain pin. I2C-bus pins compliant with the I2C-bus specification for I2C standard mode, I2C Fast-mode, and I2C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I2C lines. Open-drain configuration applies to all functions on this pin.

[4] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.

[5] Reset pad.5 V tolerant pad with glitch filter with hysteresis. Pulse width of spikes or glitches suppressed by input filter is from 3 ns to 20 ns (simulated value)

[6] 5 V tolerant transparent analog pad.

[7] The oscillator input pin (XTALIN) cannot be driven by an external clock. Must connect a crystal between XTALIN and XTALOUT.

[8] VBUS must be connected to supply voltage when using the USB peripheral.

6.2.1 Termination of unused pins

Table 5 shows how to terminate pins that are **not** used in the application. In many cases, unused pins should be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin’s IOCON register.

In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 5. Termination of unused pins

Pin	Default state[1]	Recommended termination of unused pins
$\overline{\text{RESET}}$	I; PU	The $\overline{\text{RESET}}$ pin can be left unconnected if the application does not use it.
all PIOn_m (not open-drain)	I; PU	Can be left unconnected if driven LOW and configured as GPIO output with pull-up disabled by software.
PIOn_m (I2C open-drain)	IA	Can be left unconnected if driven LOW and configured as GPIO output by software.
RTCXIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
RTCXOUT	-	Can be left unconnected.
XTALIN	-	Connect to ground. When grounded, the RTC oscillator is disabled.
XTALOUT	-	Can be left unconnected.
VREFP	-	Tie to VDD.
VREFN	-	Tie to VSS.
VDDA	-	Tie to VDD.
VSSA	-	Tie to VSS.
VBAT	-	Tie to VDD.
USBn_DP	F	Can be left unconnected. If USB interface is not used, pin can be left unconnected except in deep power-down mode where it must be externally pulled low. When the USB PHY is disabled, the pins are floating.

7.17.1.2 USB0 host controller

The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies with the Open Host Controller Interface (OHCI) specification.

Features

- OHCI compliant.
- Two downstream ports.

7.17.2 High-speed USB Host/Device interface (USB1)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

7.17.2.1 USB1 device controller

The device controller enables 480 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

Features

- Fully compliant with *USB 2.0 Specification* (high speed).
- Supports 8 physical (16 logical) endpoints with up to 8 kB endpoint buffer RAM.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint Maximum packet size selection (up to USB maximum specification) by software at run time.
- While USB is in the Suspend mode, the LPC546xx can enter one of the reduced power modes and wake up on USB activity.
- Double buffer implementation for Bulk and Isochronous endpoints.

7.17.2.2 USB1 host controller

The host controller enables high speed data exchange with USB devices attached to the bus. It consists of register interface and serial interface engine. The register interface complies with the Enhanced Host Controller Interface (EHCI) specification.

Features

- EHCI compliant.
- Two downstream ports.
- Supports per-port power switching.

7.18.1.1 Features

- AHB master interface to access frame buffer.
- Setup and control via a separate AHB slave interface.
- Dual 16-deep programmable 64-bit wide FIFOs for buffering incoming display data.
- Supports single and dual-panel monochrome Super Twisted Nematic (STN) displays with 4-bit or 8-bit interfaces.
- Supports single and dual-panel color STN displays.
- Supports Thin Film Transistor (TFT) color displays.
- Programmable display resolution including, but not limited to: 320 × 200, 320 × 240, 640 × 200, 640 × 240, 640 × 480, 800 × 600, and 1024 × 768.
- Hardware cursor support for single-panel displays.
- 15 gray-level monochrome, 3375 color STN, and 32 K color palettized TFT support.
- 1, 2, or 4 bits-per-pixel (bpp) palettized displays for monochrome STN.
- 1, 2, 4, or 8 bpp palettized color displays for color STN and TFT.
- 16 bpp true-color non-palettized for color STN and TFT.
- 24 bpp true-color non-palettized for color TFT.
- Programmable timing for different display panels.
- 256 entry, 16-bit palette RAM, arranged as a 128 × 32-bit RAM.
- Frame, line, and pixel clock signals.
- AC bias signal for STN, data enable signal for TFT panels.
- Supports little and big-endian, and Windows CE data formats.
- LCD panel clock may be generated from the peripheral clock, or from a clock input pin.

7.18.2 SD/MMC card interface

The SD/MMC card interface supports the following modes to control:

7.18.2.1 Features

- Secure Digital memory (SD version 1.1).
- Secure Digital I/O (SDIO version 2.0).
- Consumer Electronics Advanced Transport Architecture (CE-ATA version 1.1).
- MultiMedia Cards (MMC version 4.1).
- Supports up to a maximum of 50 MHz of interface frequency.

7.18.3 External memory controller

The LPC546xx EMC is an ARM PrimeCell MultiPort Memory Controller peripheral offering support for asynchronous static memory devices such as RAM, ROM, and flash. In addition, it can be used as an interface with off-chip memory-mapped devices and peripherals. The EMC is an Advanced Microcontroller Bus Architecture (AMBA) compliant peripheral.

7.23.2 SHA-1 and SHA-2

The Hash peripheral is used to perform SHA-1 and SHA-2 (256) based hashing. A hash takes an arbitrarily large message or image and forms a relatively small fixed size “unique” number called a digest. The data is fed by words from the processor, DMA, or hosted access; the words are converted from little-endian (ARM standard) to big-endian (SHA standard) by the block.

7.23.2.1 Features

- Used with an HMAC to support a challenge/response or to validate a message.
- Can be used to verify external memory that has not been compromised.

7.24 Code security (enhanced Code Read Protection - eCRP)

eCRP is a mechanism that allows the user to enable different features in the security system. The features are specified using a combination of OTP and flash values. Some levels are only controlled by either flash or OTP, but the majority have dual control. The overlap allows higher security by specifying access using OTP bits, which cannot be changed (except to increase security) while allowing customers who are less concerned about security the ability to change levels in the flash image.

eCRP is calculated by reading the ECRP from the flash boot sector (offset 0x0000 0020) and then masking it with the value read from OTP. The OTP bits are more restrictive (that is, disable access) than equivalent values in flash. Certain aspects of eCRP are only specified in the OTP (that is, Mass Erase disable), while others are only specified in flash (that is, Sector Protection count).

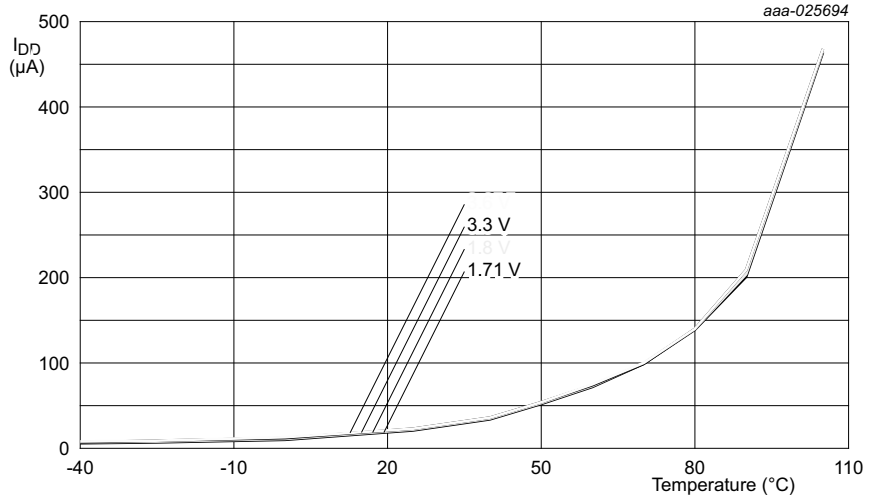
For Dual Enhanced images, eCRP is calculated by reading the eCRP from the bootable image sector. The bootable image is defined as the highest revision image that passes the required validation methods.

7.25 Emulation and debugging

Debug and trace functions are integrated into the ARM Cortex-M4. Serial wire debug and trace functions are supported. The ARM Cortex-M4 is configured to support up to eight breakpoints and four watch points.

The ARM SYSREQ reset is supported and causes the processor to reset the peripherals, execute the boot code, restart from address 0x0000 0000, and break at the user entry point.

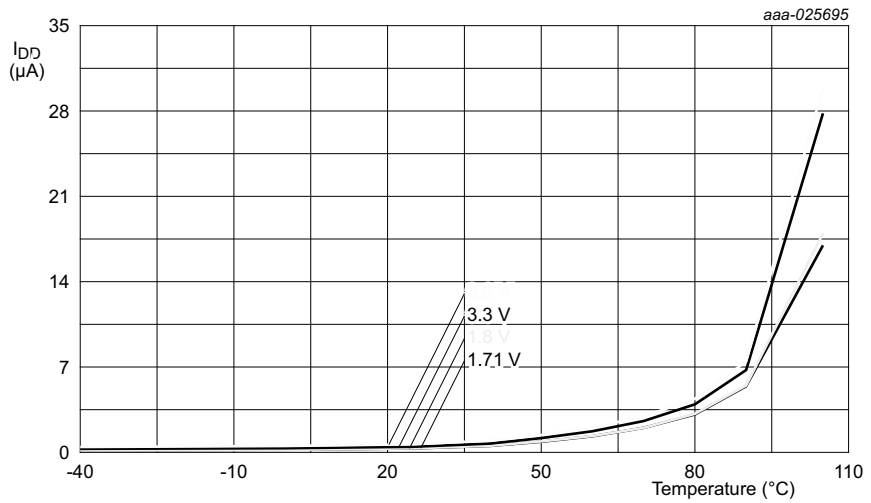
The SWD pins are multiplexed with other digital I/O pins. On reset, the pins assume the SWD functions by default.



Conditions: BOD disabled; all oscillators and analog blocks disabled; all SRAM disabled except 32 KB SRAMX.

Remark: At hot temperature and below 2.0 V, the supply current could increase slightly because of reduction of available RBB (reverse body bias) voltage.

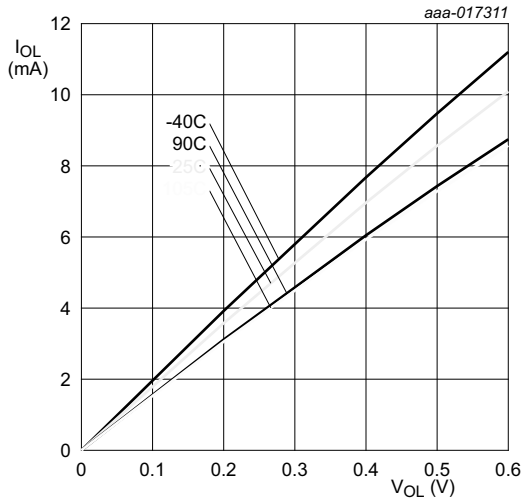
Fig 16. Deep-sleep mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}



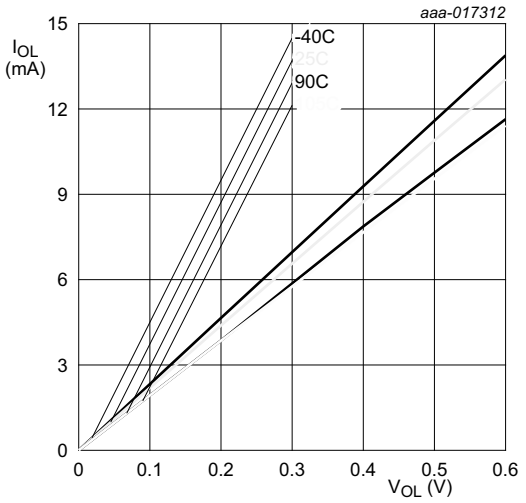
RTC disabled (RTC oscillator input grounded).

Fig 17. Deep power-down mode: Typical supply current I_{DD} versus temperature for different supply voltages V_{DD}

Table 19 shows the typical peripheral power consumption measured on a typical sample at Tamb = 25 °C and VDD = 3.3 V. The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled using ASYNCAPBCLKCTRL, AHBCLKCTRL0/1/2, and PDRUNCFG0/1

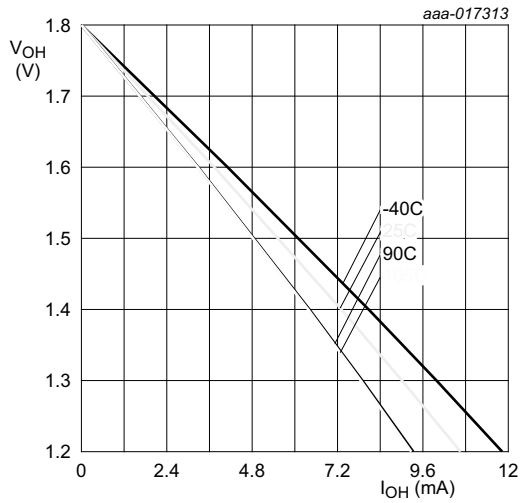


Conditions: V_{DD} = 1.8 V; on standard port pins.

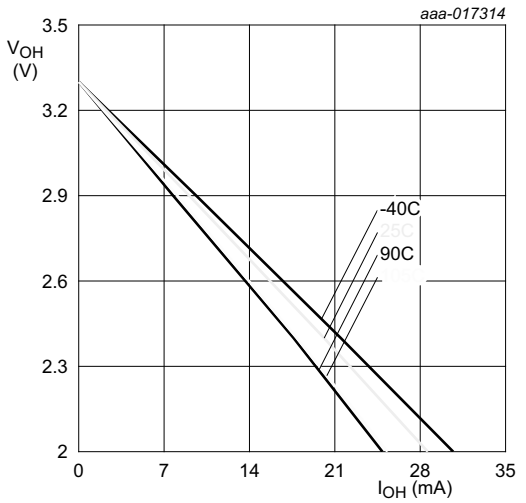


Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 20. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 1.8 V; on standard port pins.



Conditions: V_{DD} = 3.3 V; on standard port pins.

Fig 21. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}

[2] $T_{cy(clk)}$ = 1/EMC_CLK (see *UM10912* LPC546xx *manual*).

[3] Latest of address valid, $\overline{\text{EMC\_CSx}}$ LOW, $\overline{\text{EMC\_OE}}$ LOW, $\overline{\text{EMC\_BLSx}}$ LOW (PB = 1).

[4] After End Of Read (EOR): Earliest of $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_OE}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1), address invalid.

[5] End Of Write (EOW): Earliest of address invalid, $\overline{\text{EMC\_CSx}}$ HIGH, $\overline{\text{EMC\_BLSx}}$ HIGH (PB = 1).

[6] The byte lane state bit, PB, enables different types of memory to be connected (see *the STATICCONFIG[0:3] register in the UM10912* LPC546xx *manual*).

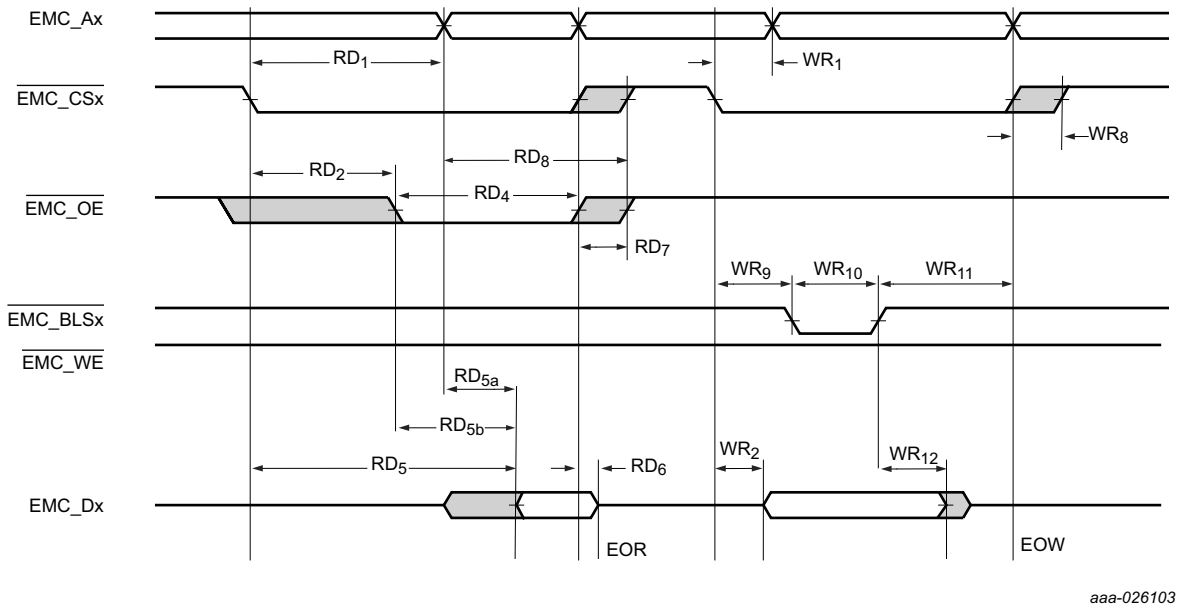


Fig 24. External static memory read/write access (PB = 0)

Table 30. Dynamic characteristics: Dynamic external memory interface programmable clock delays (CMDDLY, FBCLKDLY)

T_{amb} = −40 °C to 105 °C, V_{DD} = 2.7 V to 3.6 V.Values guaranteed by design. t_{cmddly} is programmable delay value for EMC command outputs in command delayed mode; t_{fbdly} is programmable delay value for the feedback clock that controls input data sampling.

Symbols	Parameter	Five bit value for each delay in EMCDLYCTL[1]	Min	Typ	Max	Unit
t_{cmddly}, t_{fbdly}	delay time	b00000	0.41	0.66	0.77	ns
		b00001	0.52	0.85	1.03	ns
		b00010	0.69	1.11	1.3	ns
		b00011	0.8	1.3	1.56	ns
		b00100	0.95	1.53	1.77	ns
		b00101	1.06	1.72	2.03	ns
		b00110	1.23	1.98	2.3	ns
		b00111	1.34	2.17	2.56	ns
		b01000	1.45	2.3	2.67	ns
		b01001	1.56	2.49	2.93	ns
		b01010	1.73	2.75	3.2	ns
		b01011	1.84	2.94	3.46	ns
		b01100	1.99	3.17	3.67	ns
		b01101	2.1	3.36	3.93	ns
		b01110	2.27	3.62	4.2	ns
		b01111	2.38	3.81	4.46	ns
		b10000	2.45	3.86	4.46	ns
		b10001	2.56	4.05	4.72	ns
		b10010	2.73	4.31	4.99	ns
		b10011	2.84	4.5	5.25	ns
		b10100	2.99	4.73	5.46	ns
		b10101	3.1	4.92	5.72	ns
		b10110	3.27	5.18	5.99	ns
		b10111	3.38	5.37	6.25	ns
		b11000	3.49	5.5	6.36	ns
		b11001	3.6	5.69	6.62	ns
		b11010	3.77	5.95	6.89	ns
		b11011	3.88	6.14	7.15	ns
		b11100	4.03	6.37	7.36	ns
		b11101	4.14	6.56	7.62	ns
		b11110	4.31	6.82	7.89	ns
		b11111	4.42	7.01	8.15	ns

[1] The programmable delay blocks are controlled by the EMCDLYCTL register in the EMC register block. All delay times are incremental delays for each element starting from delay block 0. See the *LPC546xx. user manual* for details.

11.7 USB PLL (PLL1)

Table 33. PLL1 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL1 configuration: input frequency 12 MHz; output frequency 48 MHz							
$t_{lock(PLL1)}$	PLL1 lock time		[1]	-	7.4	-	μs
$I_{DD(PLL1)}$	PLL1 current	When locked	[1][2]	-	260	-	μA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

Table 34. Dynamic characteristics of the PLL1[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reference clock input							
F_{in}	input frequency			1	-	25	MHz
Clock output							
f_o	output frequency	for PLL1 clkout output	[2]	9.75	-	160	MHz
d_o	output duty cycle	for PLL1 clkout output		45	-	55	%
f_{CCO}	CCO frequency			156	-	320	MHz
Dynamic parameters at f_{out} = f_{CCO} = 320 MHz; standard bandwidth settings							
$J_{pp\text{-}period}$	peak-to-peak, period jitter	f_{ref} = 4 MHz	[3][4]	-	-	300	ps

[1] Data based on simulation, not tested in production.

[2] Excluding under- and overshoot which may occur when the PLL is not in lock.

[3] Actual jitter dependent on amplitude and spectrum of substrate noise.

[4] Input clock coming from a crystal oscillator with less than 250 ps peak-to-peak period jitter.

11.8 Audio PLL (PLL2)

Table 35. PLL2 lock times and current

T_{amb} = −40 °C to +105 °C, unless otherwise specified. V_{DD} = 1.71 V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	96	μs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	2.0	mA
PLL2 configuration: input frequency 12 MHz; output frequency 100 MHz							
$t_{lock(PLL2)}$	PLL2 lock time		[1]	-	-	108	μs
$I_{DD(PLL2)}$	PLL2 current	when locked	[1][2]	-	-	1.6	mA

[1] Data based on characterization results, not tested in production.

[2] PLL current measured using lowest CCO frequency to obtain the desired output frequency.

11.15 SPI interfaces

The actual SPI bit rate depends on the delays introduced by the external trace, the external device, system clock (CCLK), and capacitive loading. Excluding delays introduced by external device and PCB, the maximum supported bit rate for SPI master mode is 48 Mbit/s, and the maximum supported bit rate for SPI slave mode is 14 Mbit/s.

Table 43. SPI dynamic characteristics[1]

T_{amb} = −40 °C to 105 °C; 1.71 V ≤ V_{DD} ≤ 3.6 V; C_L = 30 pF balanced loading on all pins; Input slew = 1 ns, SLEW setting = standard mode for all pins;. Parameters sampled at the 50 % level of the rising or falling edge.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI master 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		6.3	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		6.7	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		2.6	-	5.0	ns
		100 MHz < CCLK ≤ 180 MHz		0.3	-	4.7	ns
SPI slave 1.71 V ≤ V_{DD} ≤ 2.7 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0.9	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		2.1	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		2.2	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		18.8	-	37.0	ns
		100 MHz < CCLK ≤ 180 MHz		18.0	-	36.0	ns
SPI master 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		2.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		2.2	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		4.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		4.5	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		1.8	-	4.6	ns
		100 MHz < CCLK ≤ 180 MHz		1.7	-	4.0	ns
SPI slave 2.7 V ≤ V_{DD} ≤ 3.6 V							
t_{DS}	data set-up time	CCLK ≤ 100 MHz		1.2	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		1.0	-	-	ns
t_{DH}	data hold time	CCLK ≤ 100 MHz		0	-	-	ns
		100 MHz < CCLK ≤ 180 MHz		0	-	-	ns
$t_{v(Q)}$	data output valid time	CCLK ≤ 100 MHz		14	-	23.9	ns
		100 MHz < CCLK ≤ 180 MHz		13.3	-	22.2	ns

[1] Based on characterization; not tested in production.

11.24 SD/MMC and SDIO

Table 51. Dynamic characteristics: SD/MMC and SDIO

T_{amb} = −40 °C to +105 °C, V_{DD} = 2.7 V to 3.6 V; C_L = 20 pF. SAMPLE_DELAY = 0, DRV_DELAY = 0 in the SDDELAY register, SDIOCLKCTRL = 0x84, sampled at 90 % and 10 % of the signal level, SLEW = 1 ns for SD_CLK pin, SLEW = 1 ns for SD_DATn and SD_CMD pins. Simulated values in high-speed mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin SD_CLK; data transfer mode	-	-	50	MHz
$t_{su(D)}$	data input set-up time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	14.4	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	14.4	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	14.4	-	-	ns
$t_{h(D)}$	data input hold time	on pins SD_DATn as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
		on pins SD_CMD as inputs				
		CCLK ≤ 100 MHz	1.5	-	-	ns
		100 MHz < CCLK ≤ 180 MHz	1.5	-	-	ns
$t_{v(Q)}$	data output valid time	on pins SD_DATn as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		100 MHz < CCLK ≤ 180 MHz	1.9	-	3.5	ns
		on pins SD_CMD as outputs				
		CCLK ≤ 100 MHz	1.9	-	3.5	ns
		100 MHz < CCLK ≤ 180 MHz	1.9	-	3.5	ns

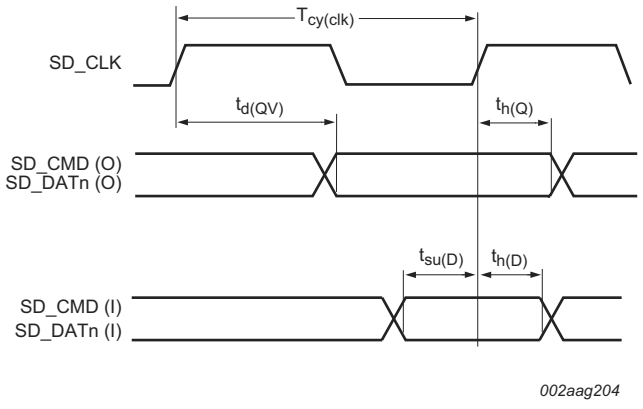


Fig 39. SD/MMC and SDIO timing

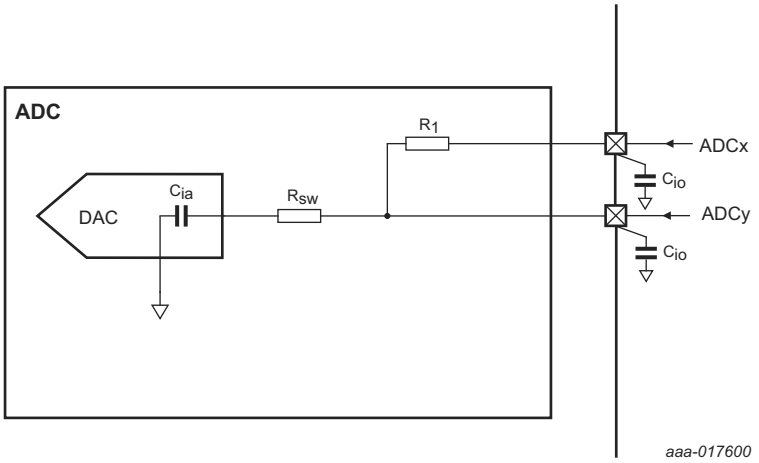


Fig 41. ADC input impedance

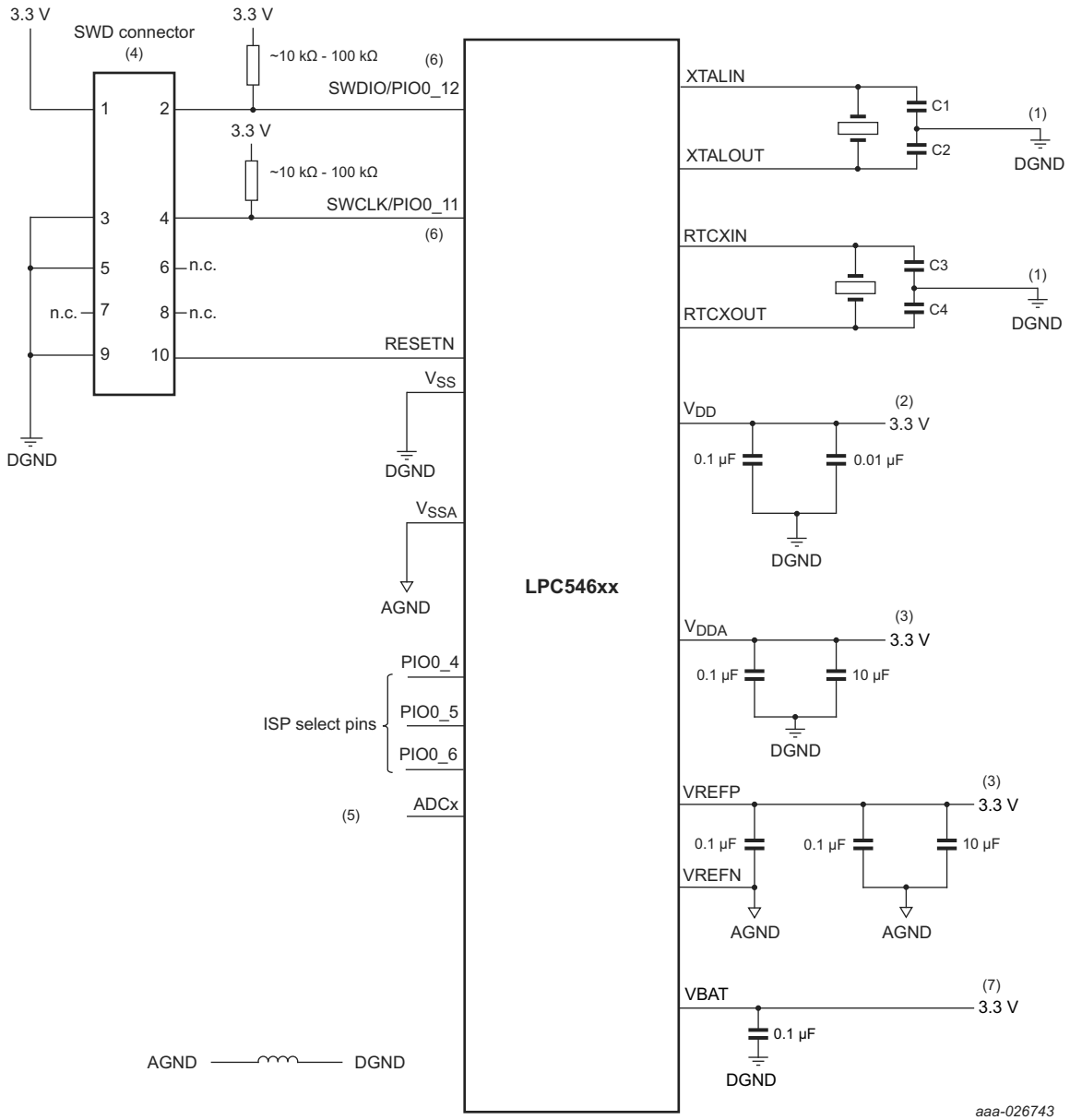
12.3 Temperature sensor

Table 56. Temperature sensor static and dynamic characteristics
$V_{DD} = V_{DDA} = 1.71$ V to 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DT_{sen}	sensor temperature accuracy	T_{amb} = −40 °C to +105 °C	[1]	-		3.7	°C
E_L	linearity error	T_{amb} = −40 °C to +105 °C		-	-	3.7	°C
$t_{s(pu)}$	power-up settling time	to 99% of temperature sensor output value	[2]	-	10.0	15.0	µs

[1] Absolute temperature accuracy.

[2] Based on simulation.



(1) See Section 13.6 “XTAL oscillator” for the values of C1, C2, C3, and C4.

(2) Position the decoupling capacitors of 0.1 µF and 0.01 µF as close as possible to the V_{DD} pin. Add one set of decoupling capacitors to each V_{DD} pin.

(3) Position the decoupling capacitors of 0.1 µF as close as possible to the VREFN and V_{DDA} pins. The 10 µF bypass capacitor filters the power line. Tie V_{DDA} and VREFP to V_{DD} if the ADC is not used. Tie VREFN to V_{SS} if ADC is not used.

(4) Uses the ARM 10-pin interface for SWD.

(5) When measuring signals of low frequency, use a low-pass filter to remove noise and to improve ADC performance. Also see Ref. 3.

(6) External pull-up resistors on SWDIO and SWCLK pins are optional because these pins have an internal pull-up enabled by default.

(7) Position the decoupling capacitor of 0.1 µF as close as possible to the V_{BAT} pin. Tie V_{BAT} to V_{DD} if not used.

Fig 45. Power, clock, and debug connections

13.5.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit should be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled in through the PCB and to keep the parasitics as small as possible.
- Lay out the ground (GND) pattern under crystal unit.
- Do not lay out other signal lines under crystal unit for multi-layered PCB.

13.6 XTAL oscillator

In the XTAL oscillator circuit, only the crystal (XTAL) and the capacitances C_{X1} and C_{X2} need to be connected externally on XTALIN and XTALOUT. See Figure 47.

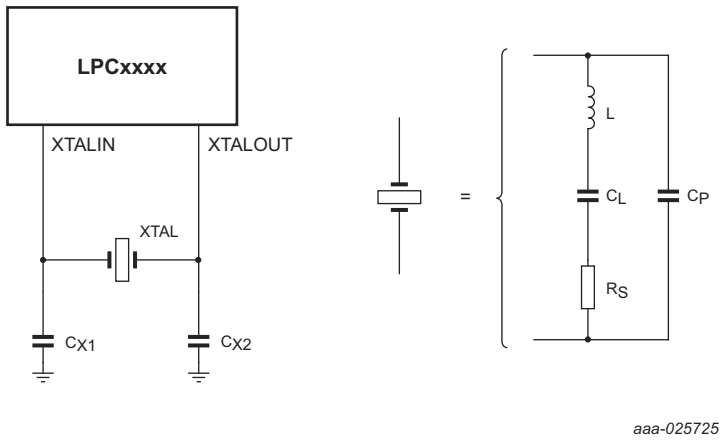


Fig 47. XTAL oscillator components

For best results, it is very critical to select a matching crystal for the on-chip oscillator. Load capacitance (CL), series resistance (RS), and drive level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTALIN and XTALOUT pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine tune the values of external load capacitors on actual hardware board to get the accurate clock frequency. For fine tuning, measure the clock on the XTALOUT pin and optimize the values of external load capacitors for minimum frequency deviation.

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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