Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia186xlplc68ir2

LIST OF TABLES

1. Introduction

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers are form, fit, and function replacements for the original Intel 80C186XL and 80C188XL 16-bit high-integration embedded processors.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures compatibility with the original device, including any "undocumented features." Additionally, the MILES™ process captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA186XL and IA188XL microcontrollers replace the obsolete Intel 80C186XL and 80C188XL devices, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

The Innovasic Semiconductor IA186XL and IA188XL microcontrollers have a set of base peripherals beneficial to many embedded applications and include a standard numeric interface, an interrupt control unit, a chip-select unit/Ready Generation Logic, a DRAM refresh control unit, a Power-Save Control unit, DMA and three 16-bit timer/counters.

The IA186XL and IA188XL microcontrollers operate at 5.0 volts ± 10%.

The following functional description describes the base architecture of the 80C186XL. The 80C186XL is a very high integration 16-bit microprocessor. It combines some of the most common microprocessor system components onto one chip. The 80C186XL is object-code compatible with the 8086/8088 microprocessors and adds ten new instruction types to the 8086/8088 instruction set.

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode, the 80C186XL is completely compatible with the 80186, with the exception of 8087 support. The Enhanced mode adds three new features to the system design. These are Power-Save control, Dynamic RAM refresh, and an asynchronous Numerics Coprocessor interface (80C186XL only).

1.2 Features

The primary features of the IA186XL and IA188XL microcontrollers are as follows:

- Form, fit, and function compatible version of the low power Intel 80C186XL/80C188XL
- Operation modes:
  - Enhanced mode
    - DRAM refresh control unit

2.1.2 IA188XL 68 PLCC Package

The pinout for the IA188XL 68 PLCC package is as shown in Figure 2. The corresponding pinout is provided in Table 2.

NOTE: The Innovasic 68-Lead PLCC package has both an ink mark and an indentation to indicate proper orientation. Pin 1 is designated by the ink mark, as shown in Figure 2.

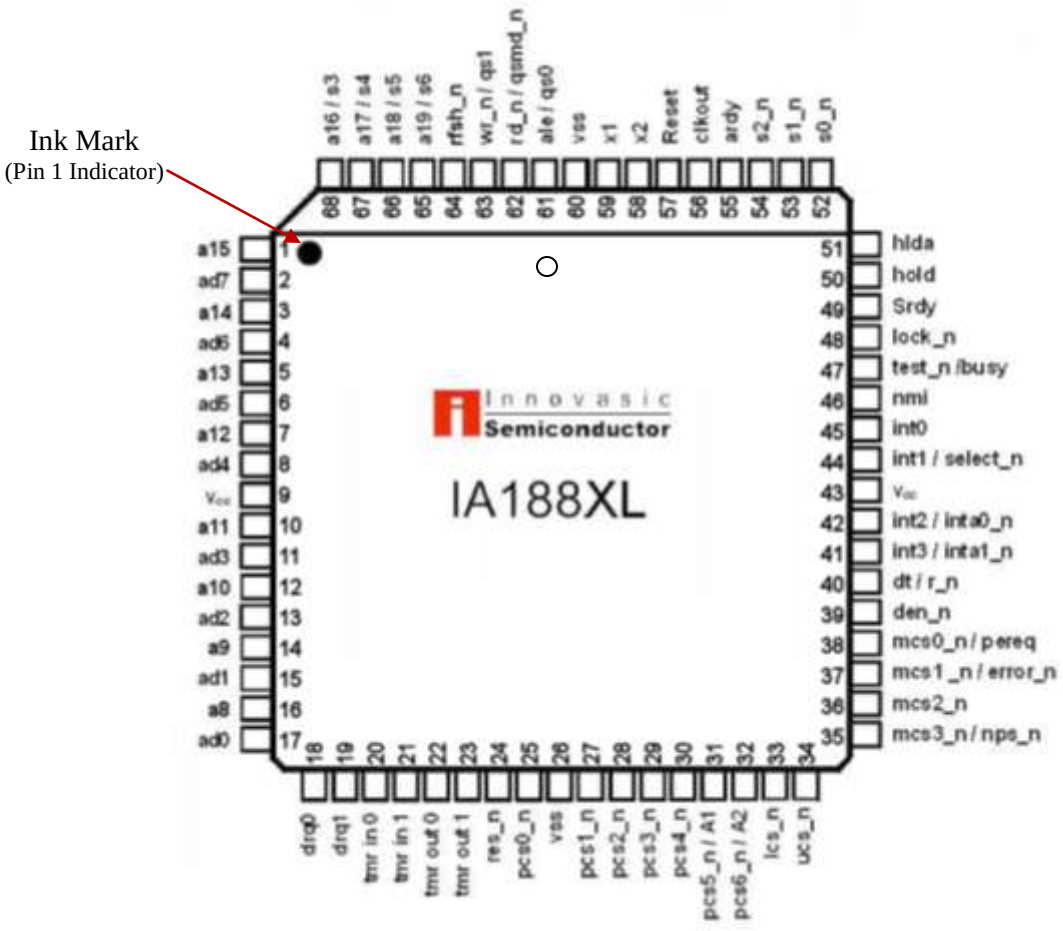

Figure 2. IA188XL 68-Lead PLCC Package Diagram

2.1.4 IA186XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 4. The corresponding pinout is provided in Table 3.

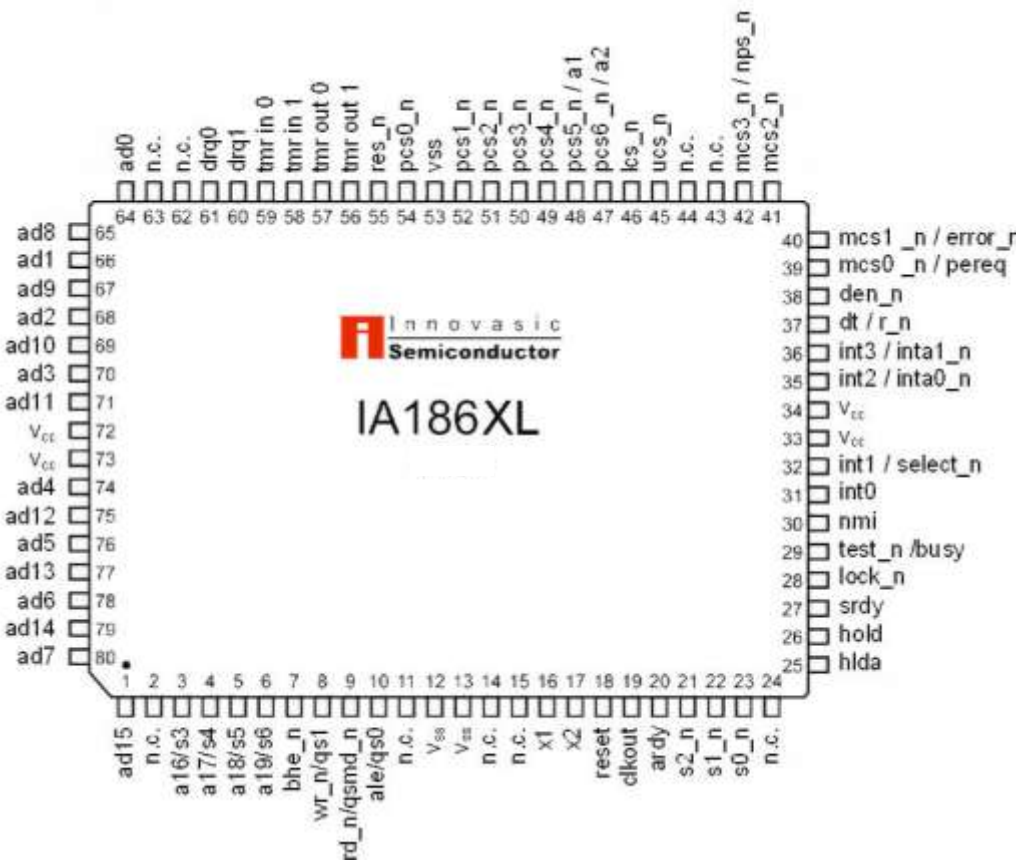

Figure 4. IA186XL 80-Lead PQFP Package Diagram

2.1.7 IA186XL 80 LQFP Package

The pinout for the IA186XL 80 LQFP package is as shown in Figure 7. The corresponding pinout is provided in Table 5.

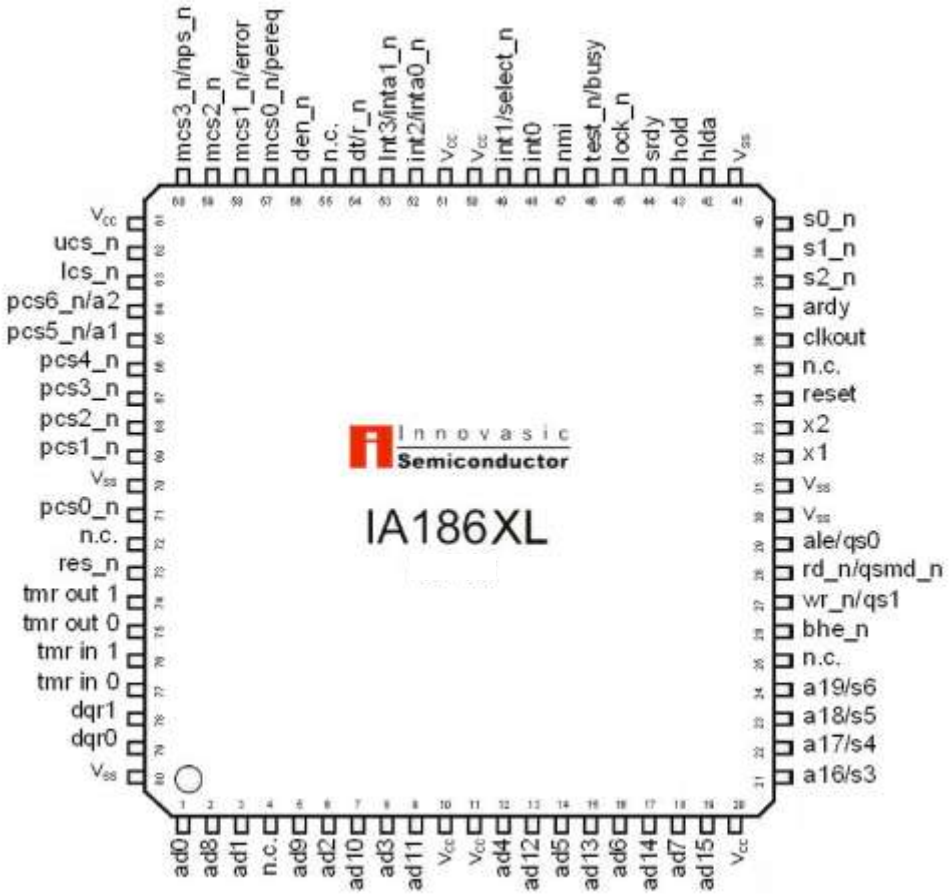

Figure 7. IA186XL 80-Lead LQFP Package Diagram

Table 5. IA186XL 80-Lead LQFP Pin Listing

Pin	Name
1	ad0
2	ad8
3	ad1
4	n.c.
5	ad9
6	ad2
7	ad10
8	ad3
9	ad11
10	v_{cc}
11	v_{cc}
12	ad4
13	ad12
14	ad5
15	ad13
16	ad6
17	ad14
18	ad7
19	ad15
20	v_{cc}

Pin	Name
21	a16/s3
22	a17/s4
23	a18/s5
24	a19/s6
25	n.c.
26	bhe_n
27	wr_n/qs1
28	rd_n/qsmd_n
29	ale/qs0
30	v_{ss}
31	v_{ss}
32	x1
33	x2
34	reset
35	n.c.
36	clkout
37	ardy
38	s2_n
39	s1_n
40	s0_n

Pin	Name
41	v_{ss}
42	hlda
43	hold
44	srdy
45	lock_n
46	test_n/busy
47	nmi
48	int0
49	int1/select_n
50	v_{cc}
51	v_{cc}
52	int2/inta0_n
53	int3/inta1_n
54	dt/r_n
55	n.c.
56	den_n
57	mcs0_n/pereq
58	mcs1_n/error
59	mcs2_n
60	mcs3_n/nps_n

Pin	Name
61	v_{cc}
62	ucs_n
63	lcs_n
64	pcs6_n/a2
65	pcs5_n/a1
66	pcs4_n
67	pcs3_n
68	pcs2_n
69	pcs1_n
70	v_{ss}
71	pcs0_n
72	n.c.
73	res_n
74	tmr out 1
75	tmr out 0
76	tmr in 1
77	tmr in 0
78	dqr1
79	dqr0
80	v_{ss}

2.2 IA186XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA186XL microcontroller are provided in Table 7.

Several of the IA186XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 7, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, PQFP, and LQFP packages are provided in the "Pin" column. Signals not used in a specific package type are designated "NA."

Table 7. IA186XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit a1. Output.
a2	pcs6_n/a2	32	47	64	Latched address bit a2. Output.
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Output. These pins provide the four most-significant bits of the Address Bus during T_1 only. During T_2, T_3, T_W and T_4 they provide bus status.
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **0**–**15**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA186XL bus cycle, Address Bits [0–15] are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the bus cycle, data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
ad8	ad8	16	65	2	
ad9	ad9	14	67	5	
ad10	ad10	12	69	7	
ad11	ad11	10	71	9	
ad12	ad12	7	75	13	
ad13	ad13	5	77	15	
ad14	ad14	3	79	17	
ad15	ad15	1	1	19	

2.3 IA188XL Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA188XL microcontroller are provided in Table 8.

Several of the IA188XL pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 8, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for the PLCC, QFP, and LQFP packages are provided in the "Pin" column.

Table 8. IA188XL Pin/Signal Descriptions

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
a1	pcs5_n/a1	31	48	65	Latched address bit **a1.** Output.
a2	pcs6_n/a2	32	47	64	Latched address bit **a2.** Output.
a16	a16/s3	68	3	21	**a**ddress bits **16**–**19**. Output. These pins provide the four most-significant bits of the Address Bus during T_1 only. During T_2, T_3, T_W and T_4 they provide bus status.
a17	a17/s4	67	4	22	
a18	a18/s5	66	5	23	
a19	a19/s6	65	6	24	
ad0	ad0	17	64	1	**a**ddress/**d**ata bits **0 - 15**. Input/Output. These pins provide the multiplexed Address Bus and Data Bus. During the address portion of the IA188XL bus cycle, address bits 0 through 15 are presented on the bus and can be latched using the ale signal (see next table entry). During the data portion of the IA188XL bus cycle, data are present on these lines.
ad1	ad1	15	66	3	
ad2	ad2	13	68	6	
ad3	ad3	11	70	8	
ad4	ad4	8	74	12	
ad5	ad5	6	76	14	
ad6	ad6	4	78	16	
ad7	ad7	2	80	18	
a8	a8	16	65	2	valid address information is provided for the entire bus cycle
a9	a9	14	67	5	
a10	a10	12	69	7	
a11	a11	10	71	9	
a12	a12	7	75	13	
a13	a13	5	77	15	
a14	a14	3	79	17	
a15	a15	1	1	19	

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
hlda	hlda	51	25	42	**h**o**ld a**cknowledge. Output. Active High. When **hlda** is asserted (high), it indicates that the IA188XL has relinquished control of the local bus to another bus master in response to a HOLD request (see next table entry). When **hlda** is asserted, the IA188XL data bus and control signals are floated allowing another bus master to drive the signals directly.
hold	hold	50	26	43	**hold**. Input. Active High. This signal is a request indicating that an external bus master wishes to gain control of the local bus. The IA188XL will relinquish control of the local bus between instruction boundaries not conditioned by a LOCK prefix.
int0	int0	45	31	48	**int**errupt N (N = **03**). Input. Active High. These maskable inputs interrupt program flow and cause execution to continue at an interrupt vector of a specific interrupt type as follows: • **int0**: Type 12 • **int1**: Type 13 • **int2**: Type 14 • **int3**: Type 15 To allow interrupt expansion, **int0** and **int1** can be used with the interrupt acknowledge signals **inta0_n** and **inta1_n** (see next table entries).
int1	int1	44	32	49	
int2	int2/inta0_n	42	35	52	
int3	int3/inta1_n	41	36	53	
inta 0_n	int2/inta0_n	42	35	52	**int**errupt **a**cknowledge**.** Output. Active low. When used with external interrupt controllers.
inta 1_n	int3/inta1_n	41	36	53	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress cannot be interrupted. While **lock_n** is active, the IA188XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect. Output.
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt .
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6.** Output.
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
qs0	ale/qs0	61	10	29	**q**ueue **s**tatus **0**, **q**ueue **s**tatus **1.** Output. QS1 QS0 0 0 No Queue operations 0 1 First byte of opcode pulled from Queue 1 1 Additional bytes pulled from Queue 1 0 Queue is flushed
qs1	wr_n/qs1	63	8	27	
qsmd_n	rd_n/qsmd_n	62	9	28	**q**ueue **s**tatus **mod**e. Input. Sampled at reset.
rd_n	rd_n/qsmd_n	62	9	28	**rea**d. output. Active Low. When asserted (low), **rd_n** indicates that the accessed memory or I/O device must drive data from the location being accessed onto the data bus.

Table 8. IA188XL Pin/Signal Descriptions *(Continued)*

Signal	Pin Name	Pin PLCC	Pin PQFP	Pin LQFP	Description
res_n	res_n	24	55	73	**res_n**. Input. Forces the processor to terminate its present activity, reset the internal logic, and enter a dormant state until res_n goes high.
reset	reset	57	18	34	**reset** is an output signal indicating the CPU is being reset. It can be used as a system reset.
rfsh_n	rfsh_n	64	7	26	**refresh.** Output. **rfsh_n** is asserted low to indicate a refresh bus cycle.
s0_n	s0_n	52	23	40	**s**tatus [**2**:**0**]_**n** are outputs. During a bus cycle the status (i.e., type) of cycle is encoded on these lines as follows: **s2_n s1_n s0_n** Bus Cycle Status 0 0 0 Interrupt Acknowledge 0 0 1 Read I/O 0 1 0 Write I/O 0 1 1 Processor HALT 1 0 0 Queue Instruction Fetch 1 0 1 Read Memory 1 1 0 Write Memory 1 1 1 No Bus Activity
s1_n	s1_n	53	22	39	
s2_n	s2_n	54	21	38	
s3	a16/s3	68	3	21	**s**tatus [**6**:**3**] are outputs. Bus Cycle A19/s6 A18/s5 A17/s4 A16/s3 T_1 A19 A18 A17 A16 T_2 N 0 0 0 T_3 N 0 0 0 T_w N 0 0 0 T_4 N 0 0 0 N = 0 for CPU bus cycle. N = 1 for DMA or refresh cycle.
s4	a17/s4	67	4	22	
s5	a18/s5	66	5	23	
s6	a19/s6	65	6	24	
srdy	srdy	49	27	44	**s**ynchronous **rea**d**y.** Input.
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA188XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**timer 0 in**put. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
tmr in 1	tmr in 1	21	58	76	**timer 1 in**put. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.

The rd_n/qsmd_n, ucs_n, lcs_n, mcs0_n/pereq, mcs1_n/error_n, and test_n/busy pins include internal pull-ups that are active while res_n is applied. The state of these pins during reset controls invoking various alternative operating modes as described below:

1 ONCE Mode – ucs_n and lcs_n driven low.
2 Enhanced Mode – test_n/busy driven low then high.
3 Queue Status Mode – rd_n/qsmd_n driven low.

4.1.2 Clock Generator

The IA186XL/IA188XL uses an on-chip clock generator to supply internal and external clocks. The clock generator makes use of a crystal oscillator and includes a divide-by-two counter.

Figure 11 shows the various operating modes of the clock circuit. The clock circuit can use either a parallel resonant fundamental mode crystal network (A) or a third-overtone mode crystal network (B), or it can be driven by an external clock source (C).

The following parameters are recommended when choosing a crystal:

- Temperature Range: Application Specific
- ESR (Equivalent Series Resistance): 60Ω max
- C0 (Shunt Capacitance of Crystal): 7.0 pF max
- CL (Load Capacitance): 20 pF ± 2 pF
- Drive Level: 2 mW max

4.1.3 Interrupt Control Unit

The IA186XL operates with several interrupt sources. A separate Interrupt Control Unit manages all sources based on priority to be individually handled by the CPU. The DMA and Timers produce internally generated requests. There are five externally generated interrupts - a single NMI and 4 others.

4.1.4 Timer/Counter Unit

There are three programmable internal timers in the IA186XL. Two are very flexible and can be configured for many tasks. Each of these has a single input used for either control or clocking, and a single output to generate waveforms. The third timer is simpler and can only be clocked from an internal source. It can be used for simple timing applications. It can also be used as a prescaler to the other two timers or as a trigger for DMA requests.

4.2 Operating Modes

During reset the IA186XL can be configured to enable special operating modes described as follows.

4.2.1 Enhanced Mode

If Enhanced Mode is enabled, the IA186XL has DRAM refresh, Power-Save and coprocessor support available in addition to the normal features available in Compatible Mode. Enhanced Mode will be invoked automatically if a coprocessor is attached. It can also be entered by tying the reset output to the test_n/busy input. An internal pull-up keeps the part from entering Enhanced mode during normal operation.

When not in Enhanced Mode, none of the Enhanced Mode registers can be accessed. Queue-Status functions, except for the coprocessor support, will be available when not in Enhanced Mode.

4.2.2 Queue Status Mode

When Queue Status Mode is enabled, information about the instruction queue is output on the ale/qs0 and wr_n/qs1 pins. To enter Queue Status Mode, the rd_n input should be tied low. It is sampled at reset, and if low, Queue Status Mode is entered. An internal pull-up keeps the part from entering Queue Status mode during normal operation.

4.2.3 ONCE Mode

ONCE mode is a special test mode where all pins are set to a high impedance state. ONCE mode is entered by forcing lcs_n and ucs_n low during reset. These pins are sampled on the rising edge of res but should be held low for at least a full clock cycle after res goes high. ONCE mode is exited by reseting the part with lcs_n and ucs_n high. Internal pull-ups keep the part from entering ONCE mode during normal operation.

4.2.4 Math Coprocessor (IA186XL Only)

When Enhanced mode is enabled, the IA186XL is configured to interface with a math coprocessor via three of the middle chip select pins. Pin mcs0/pereq is used for Processor Extension Request. Pin mcs1/error is used for coprocessor error indication. Pin mcs3/nps is used for Numeric Processor Select.

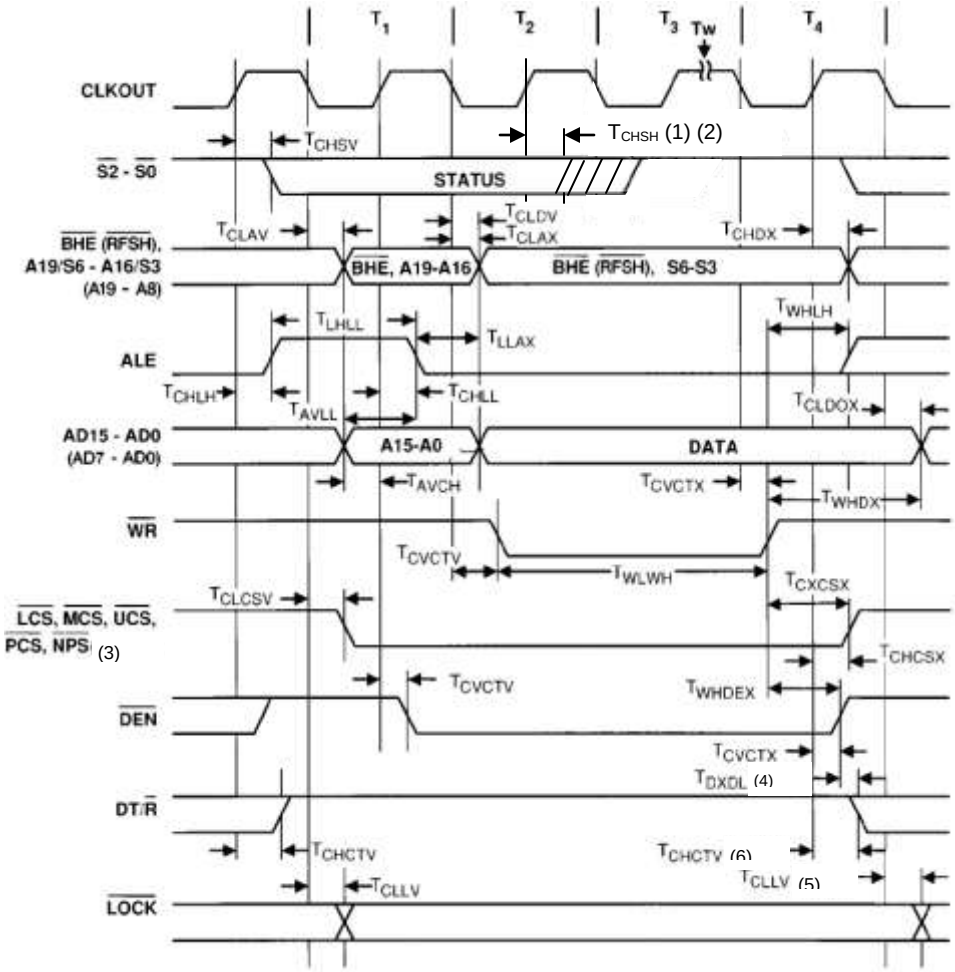

Figure 13. Write Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) Only TCLCSV is applicable if latched A1 and A2 are selected instead of PCS5 and PCS6.
(4) This applies when a write cycle is followed by a read cycle.
(5) This is T1 of next bus cycle.
(6) This changes in the T-state preceding the next bus cycle if followed by a read, INTA or halt.

5.3 Major Cycle Timings – Interrupt Acknowledge Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 15. Major Cycle Timings – Interrupt Acknowledge Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{DVCL}	Data in Setup (A/D)	8		ns	
T_{CLDX}	Data in Hold (A/D)	3		ns	
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold to ALE Inactive	T_{CHCL} - 10		ns	Equal Loading
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	ns	
T_{CVCTV}	Control Active Delay 1	3	17	ns	
T_{CVCTX}	Control Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	ns	
T_{CVDEX}	DEN Inactive Delay (Non-Write Cycles)	3	17	ns	
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	

5.4 Software Halt Cycle Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 16. Software Halt Cycle Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{DXDL}	DEN Inactive to DT/R Low		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	ns	

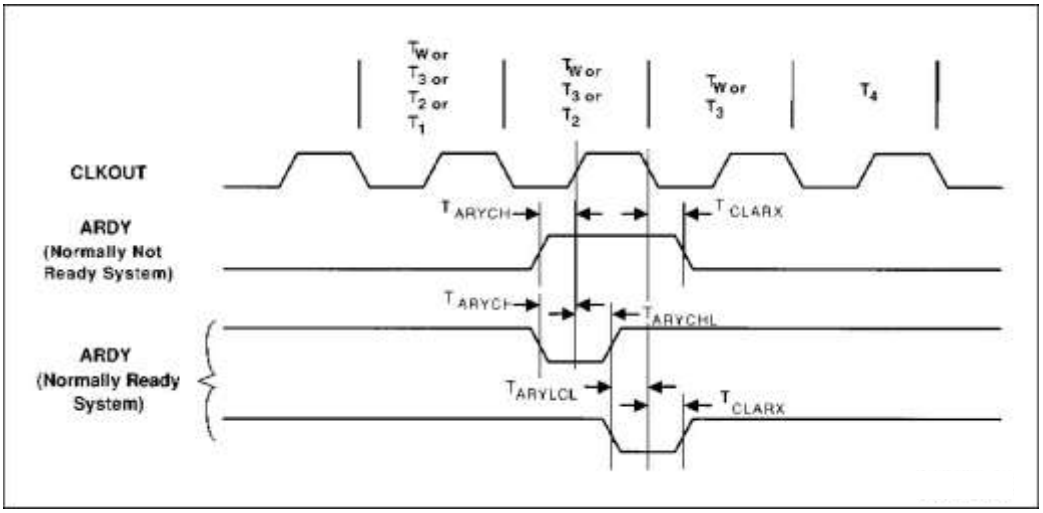

Figure 19. Asynchronous Ready (ARDY) Waveforms

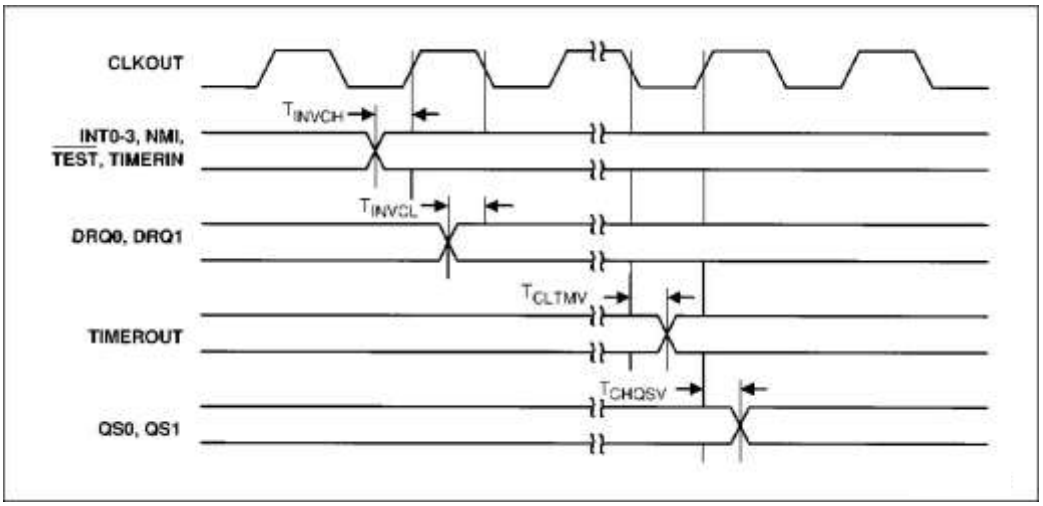

Figure 20. Peripheral and Queue Status Waveforms

Table 23. Innovasic Part Number Cross-Reference for the LQFP (Special Order only)

Innovasic Part Number	Intel Part Number	Package Type	Temperature Range
IA186XLPLQ80IR1 (lead free–RoHS)	SB80C186XL25 SB80C186XL20 SB80C186XL12 YW80C186XL25 YW80C186XL20	80-Lead LQFP	Industrial
IA188XLPLQ80IR1 (lead free–RoHS)	SB80C188XL25 SB80C188XL20 SB80C188XL12 YW80C188XL25 YW80C188XL20	80-Lead LQFP	Industrial

Workaround: When using external interrupts in cascade mode, do not program other interrupts to have a high priority (except DMAs). When using both IRQ0 and IRQ1 in Cascade Mode they must be programmed to have the same priority level.

Errata No. 4

Problem:
Memory->Memory moves interrupted by two DMA cycles can corrupt data.

Description:

This problem occurs if Memory->Memory operation is interrupted by
2 DMA cycles with the following sequence:

1. The instruction reads data from memory.
2. The first DMA cycle occurs.
3. The second DMA request occurs between 1 and 4 clocks after the falling edge of ALE for the deposit phase of the first DMA.
4. An instruction fetch occurs (this will be the data that shows up later).
5. The second DMA cycle occurs.
6. The write phase of the instruction happens with bad data (from step 4).

If the second DMA request occurs earlier than 1 clock after ALE for the first DMA's deposit phase, step 4 will be preempted by the second DMA, and operation is correct.

If the second DMA request occurs later than 4 clocks after ALE for the first DMA's deposit phase, the write phase will follow step 4 immediately, and operation is correct.

Of the total 163 instructions, the following 8 are impacted by this issue, with both the 8 & 16 bit versions of the first 7 on the list being affected.

1. MOVS
2. PUSH mem
3. POP mem
4. INS
5. IN
6. OUTS
7. OUT
8. ENTER

Workaround: If the conditions described above occur, there is no workaround. However, this DMA issue will be corrected in Revision 1 of the device.

Errata No. 5

Problem:
Bit 15 of RELREG (offset 0xFE) behaves differently than Intel device.

Description: For both 188 and 186 devices, an ESC opcode will generate a type 7 interrupt only when RELREG[15] is a 0.

Workaround: Initialize RELREG[15] to 0 if a type 7 interrupt is desired.

Errata No. 6

Problem:
Enhanced mode makes bit 15 of RELREG (offset 0xFE) read-only.

Description: If the device comes out of reset in enhanced mode, RELREG[15] will be set to a 1.

Workaround: Avoid enhanced mode if a type 7 interrupt is desired.

Errata No. 7

Problem:
Sbus deasserts on the wrong edge of CLKOUT.

Description: The sbus goes inactive (high) at the end of a bus cycle on the falling edge of CLKOUT. It should be on the rising edge of CLKOUT.

Workaround: None.

Errata No. 8

Problem:
Timer2 count register must be written to enable counting.

Description: If timer 2 count register is not explicitly written timer 2 will not count; this can also prevent timers 0 & 1 from counting if timer 2 is used as a prescaler.

Workaround: Write timer 2 count register before enabling timer 2.