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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	16-Bit
Speed	25MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	DMA
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.21x24.21)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ia188xlplc68ir2

LIST OF FIGURES

2.1.5 IA188XL 80 PQFP Package

The pinout for the IA186XL 80 PQFP package is as shown in Figure 5. The corresponding pinout is provided in Table 4.

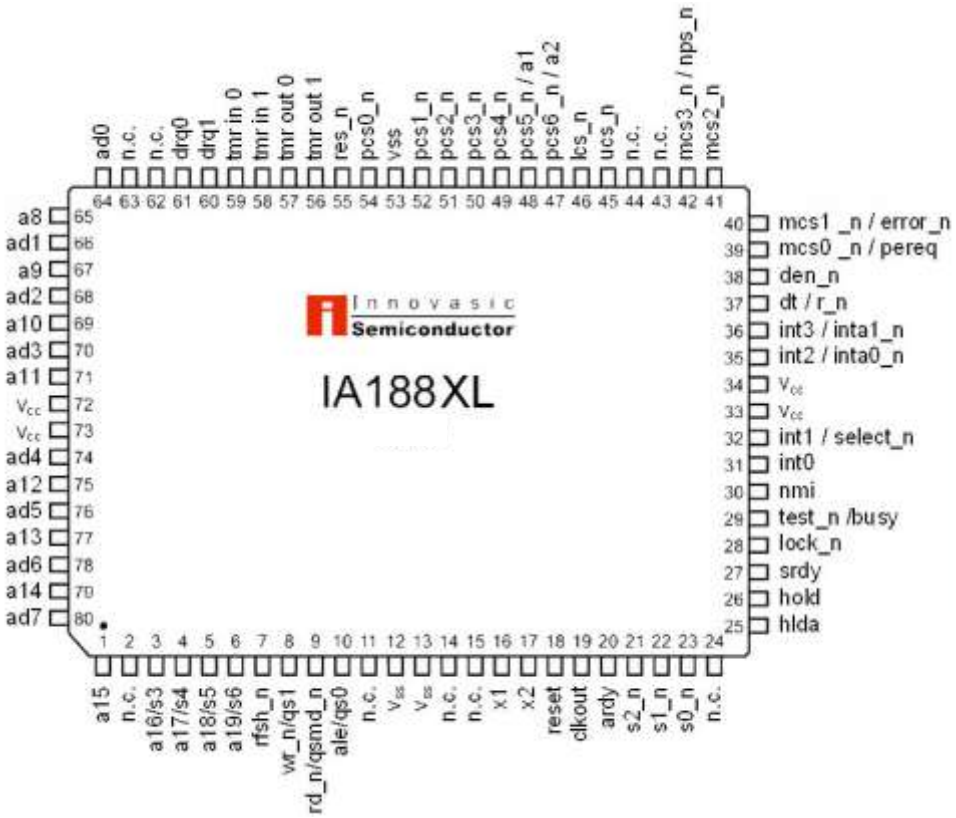
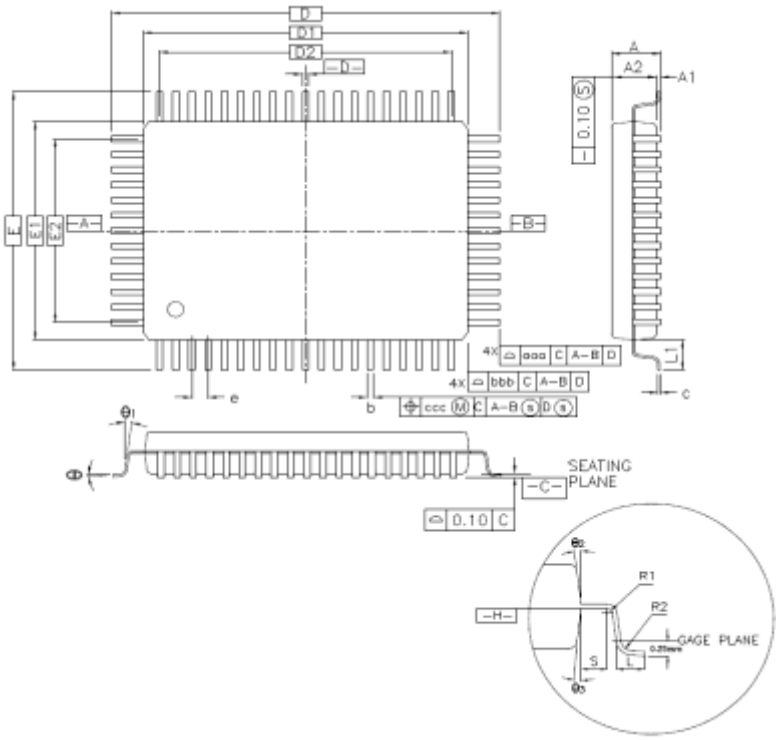


Figure 5. IA188XL 80-Lead PQFP Package Diagram

2.1.6 PQFP Physical Dimensions

The physical dimensions for the 80 PQFP are as shown in Figure 6.



Legend:

Symbol	Millimeter Min	Nom	Max	Inch Min	Nom	Max
A	–	–	3.40	–	–	0.134
A1	0.25	–	–	0.010	–	–
A2	2.55	2.72	3.05	0.100	0.107	0.120
D	23.90 Basic			0.941 Basic		
D1	20.00 Basic			0.787 Basic		
E	17.90 Basic			0.705 Basic		
E1	14.00 Basic			0.551 Basic		
R2	0.013	–	0.30	0.005	–	0.012
R1	0.013	–	–	0.005	–	–
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	–	–	0°	–	–
θ2, θ3[a]	7° REF			7° REF		
θ2, θ3[b]	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.95 REF			0.077 REF		
S	0.40	–	–	0.016	–	–
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC			0.031 BSC		
D2	18.40 REF			0.724		
E2	12.00 REF			0.472		
Tolerances of Form and Position						
aaa	0.25			0.010		
bbb	0.20			0.008		
ccc	0.20			0.008		

[a]Alloy 42 L/F.
[b]Copper L/F.

Notes:
1. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimension D1 and E1 do not include mold mismatch and are determined a datum plane –H–.
2. Dimension b does not include dambar protrusion. Allowable dambar protrusion will not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located on the lower radius of the lead foot.

Figure 6. PQFP Physical Package Dimensions

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
lcs_n	lcs_n	33	46	63	**l**ower **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
lock_n	lock_n	48	28	45	**lock**. Output. Active Low. When asserted (low), this signal indicates that the bus cycle in progress cannot be interrupted. While **lock_n** is active, the IA186XL will not service bus requests such as HOLD. When **resin_n** is active, this pin is weakly held high and must not be driven low.
mcs0_n	mcs0_n/pereq	38	39	57	**m**id-range memory **c**hip **s**elect. Output.
mcs1_n	mcs1_n/error_n	37	40	58	
mcs2_n	mcs2_n	36	41	59	
mcs3_n	mcs3_n/nps_n	35	42	60	
n.c.	n.c.	NA	2, 11, 14, 15, 24, 43, 44, 62, 63	4, 25, 35, 55, 72	**n**ot **c**onnected.
nmi	nmi	46	30	47	**n**on-**m**askable **i**nterrupt. Input. Active High. When the **nmi** signal is asserted (high) it causes a Type 2 interrupt.
nps_n	mcs3_n/nps_n	35	42	60	**n**umeric **p**rocessor **s**elect
pcs0_n	pcs0_n	25	54	71	**p**eripheral **c**hip **s**elect signals **0**–**6**. Output.
pcs1_n	pcs1_n	27	52	69	
pcs2_n	pcs2_n	28	51	68	
pcs3_n	pcs3_n	29	50	67	
pcs4_n	pcs4_n	30	49	66	
pcs5_n	pcs5_n/a1	31	48	65	
pcs6_n	pcs6_n/a2	32	47	64	
pereq	mcs0_n/pereq	38	39	57	numerics co**p**rocessor **e**xternal **req**uest. Input. Active High. When asserted (high), this signal indicates that a data transfer between an Intel 80C187 Numerics Coprocessor and the CPU is pending.

Table 7. IA186XL Pin/Signal Descriptions *(Continued)*

Signal	Pin				Description
	Name	PLCC	PQFP	LQFP	
test_n	test_n/busy	47	29	46	**test**. Input. Active Low. When the **test_n** input is high (i.e., not asserted), it causes the IA186XL to suspend operation during the execution of the WAIT instruction. Operation resumes when the pin is sampled low (asserted).
tmr in 0	tmr in 0	20	59	77	**timer 0 input**. Input. Depending on the Timer Mode programmed for Timer 0, this input is used either as clock input or a control signal.
tmr in 1	tmr in 1	21	58	76	**timer 1 input**. Input. Depending on the Timer Mode programmed for Timer 1, this input is used either as clock input or a control signal.
tmr out 0	tmr out 0	22	57	75	**timer 0 output**. Output. Depending on the Timer Mode programmed for Timer 0, this output can provide a single pulse or a repetitive waveform.
tmr out 1	tmr out 1	23	56	74	**timer 1 output**. Output. Depending on the Timer Mode programmed for Timer 1, this output can provide a single clock or a repetitive waveform.
ucs_n	ucs_n	34	45	62	**u**pper **c**hip **s**elect. Output. Active Low. This pin provides a chip select signal that will be asserted (low) whenever the address of a memory bus cycle is within the address space programmed for that output.
V_{CC}	V_{CC}	9, 43	33, 34, 72, 73	10, 11, 20, 50, 51, 61	Power (**V_{CC}**). This pin provides power for the IA186XL device. It must be connected to a +5V DC power source.
V_{SS}	V_{SS}	26, 60	12, 13, 53	30, 31, 41, 70, 80	Ground (**V_{SS}**). This pin provides the digital ground (0V) for the IA186XL. It must be connected to a V_{SS} board plane.
wr_n	wr_n/qs1	63	8	27	**wr**ite. Output. Active Low. When asserted (low), **wr_n** indicates that data available on the data bus are to be latched into the accessed memory or I/O device.
x1	x1	59	16	32	**x1** and **x2** are inputs for the crystal
x2	x2	58	17	33	

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA186XL and IA188XL microcontrollers, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 9 through 11, respectively.

Table 9. IA186XL and IA188XL Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40°C to +125°C
Supply Voltage with Respect to v_{ss}	−0.3V to +6.0V
Voltage on Pins other than Supply with Respect to v_{ss}	−0.3V to +(Vcc + 0.3)V

Table 10. IA186XL and IA188XL Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 85°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	68-Lead PLCC Package	32	°C/W
	80-Lead PQFP Package	46	
	80-Lead LQFP Package	52	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

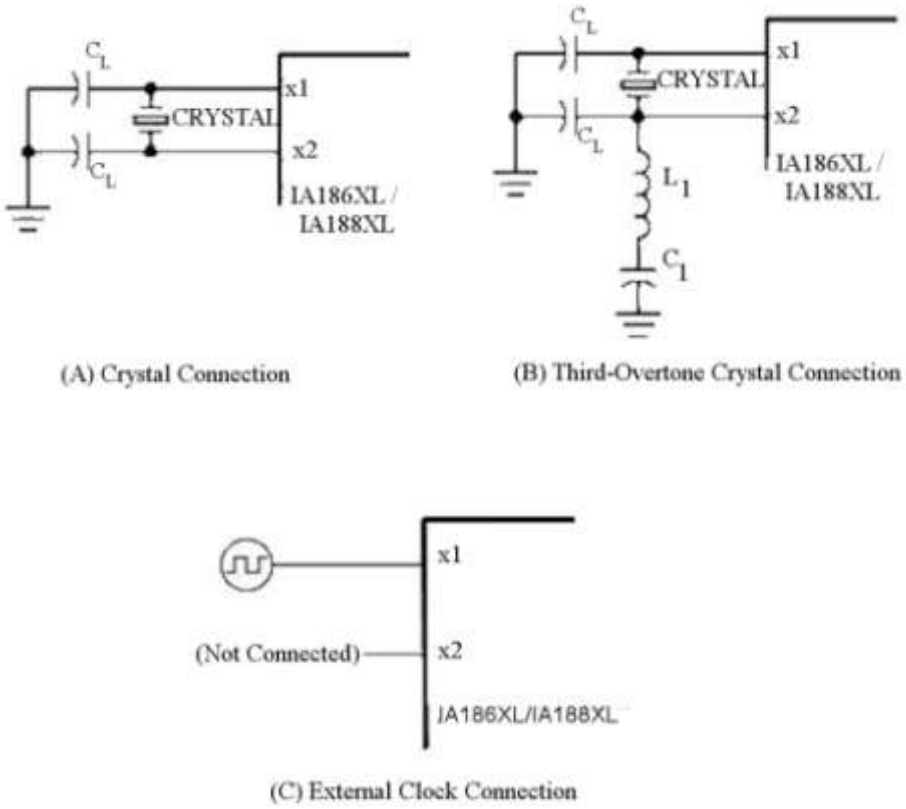


Figure 11. Clock Circuit Connection Options

4.1.5 Chip-Select/Ready Generation Logic

The IA186XL provides programmable chip-select generation for memories and peripherals. The chip can be programmed to provide READY or WAIT state generation. It can also provide latched address bits A1 and A2. Chip select behavior is the same whether the access is generated by the CPU or the DMA.

A total of 6 chip selects are dedicated for different memory ranges. A single select for upper memory (ucs_n), with a fixed end address of 0FFFFH, is good for use as system memory since the reset vector points to FFFF0H. A single select for lower memory (lcs_n), with a fixed start address of 0H, is good for interrupt vectors which reside beginning at address 00000H. There are also four selects for anywhere else (exclusive of ucs_n and lcs_n areas) in the 1 Mbyte memory in the user-locatable memory block. For the middle chip selects, the base address and block size are programmable, while only the block size for the upper and lower chip selects are programmable.

Seven additional chip selects can be programmed to access either peripherals or memory in seven contiguous fixed blocks of 128 bytes each. A single base address is programmable for these chip selects.

4.2 Operating Modes

During reset the IA186XL can be configured to enable special operating modes described as follows.

4.2.1 Enhanced Mode

If Enhanced Mode is enabled, the IA186XL has DRAM refresh, Power-Save and coprocessor support available in addition to the normal features available in Compatible Mode. Enhanced Mode will be invoked automatically if a coprocessor is attached. It can also be entered by tying the reset output to the test_n/busy input. An internal pull-up keeps the part from entering Enhanced mode during normal operation.

When not in Enhanced Mode, none of the Enhanced Mode registers can be accessed. Queue-Status functions, except for the coprocessor support, will be available when not in Enhanced Mode.

4.2.2 Queue Status Mode

When Queue Status Mode is enabled, information about the instruction queue is output on the ale/qs0 and wr_n/qs1 pins. To enter Queue Status Mode, the rd_n input should be tied low. It is sampled at reset, and if low, Queue Status Mode is entered. An internal pull-up keeps the part from entering Queue Status mode during normal operation.

4.2.3 ONCE Mode

ONCE mode is a special test mode where all pins are set to a high impedance state. ONCE mode is entered by forcing lcs_n and ucs_n low during reset. These pins are sampled on the rising edge of res but should be held low for at least a full clock cycle after res goes high. ONCE mode is exited by reseting the part with lcs_n and ucs_n high. Internal pull-ups keep the part from entering ONCE mode during normal operation.

4.2.4 Math Coprocessor (IA186XL Only)

When Enhanced mode is enabled, the IA186XL is configured to interface with a math coprocessor via three of the middle chip select pins. Pin mcs0/pereq is used for Processor Extension Request. Pin mcs1/error is used for coprocessor error indication. Pin mcs3/nps is used for Numeric Processor Select.

5. AC Specifications

5.1 Major Cycle Timings – Read Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 13. Major Cycle Timings – Read Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{DVCL}	Data in Setup (A/D)	8		ns	
T_{CLDX}	Data in Hold (A/D)	3		ns	
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 8		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLAZ}	Address Float Delay	T_{CLAX}	20	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CVCTV}	Control Active Delay 1	3	17	ns	
T_{CVDEX}	DEN Inactive Delay	3	17	ns	
T_{CHCTV}	Control Active Delay 2	3	20	ns	
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	
T_{AZRL}	Address Float to RD Active	0		ns	
T_{CLRL}	RD Active Delay	3	20	ns	
T_{RLRH}	RD Pulse Width	$2T_{CLCL}$ - 15		ns	
T_{CLRH}	RD Inactive Delay	3	20	ns	
T_{RHLH}	RD Inactive to ALE High	T_{CLCH} - 14		ns	Equal Loading

T_{RHAV}	RD Inactive to Address Active	T_{CLCL} - 15		ns	Equal Loading

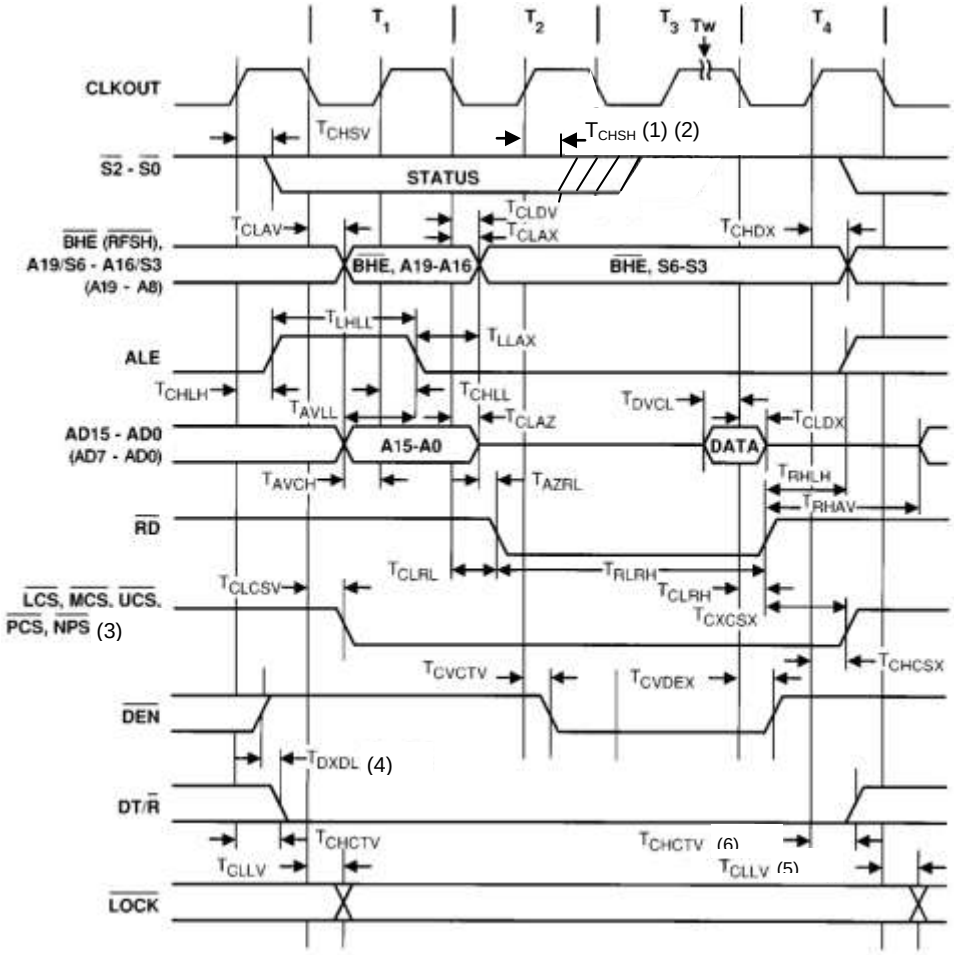


Figure 12. Read Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) Only TCLCSV is applicable if latched A1 and A2 are selected instead of PCS5 and PCS6.
(4) This applies when a write cycle is followed by read cycle.
(5) This is T1 of next bus cycle.
(6) This changes in the T-state preceding the next bus cycle if followed by a write.

5.2 Major Cycle Timings – Write Cycle

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 14. Major Cycle Timings – Write Cycle

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CLAX}	Address Hold	0		ns	
T_{CLDV}	Data Valid Delay	3	20	ns	
T_{CHDX}	Status Hold Time	10		ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{AVLL}	Address Valid to ALE Low	T_{CLCH} - 10		ns	Equal Loading
T_{LLAX}	Address Hold from ALE Inactive	T_{CHCL} - 10		ns	Equal Loading
T_{AVCH}	Address Valid to Clock High	0		ns	
T_{CLDOX}	Data Hold Time	3		ns	
T_{CVCTV}	Control Active Delay 1	3	20	ns	
T_{CVCTX}	Control Inactive Delay	3	17	ns	
T_{CLCSV}	Chip-Select Active Delay	3	20	ns	
T_{CXCSX}	Chip-Select Hold from Command Inactive	T_{CLCH} - 10		ns	Equal Loading
T_{CHCSX}	Chip-Select Inactive Delay	3	17	ns	
T_{DXDL}	DEN Inactive to DT/R Low	0		ns	Equal Loading
T_{CLLV}	LOCK Valid/Invalid Delay	3	17	ns	
T_{WLWH}	WR Pulse Width	2_{TCLCL} - 15		ns	
T_{WHLH}	WR Inactive to ALE High	T_{CLCH} - 14		ns	Equal Loading
T_{WHDX}	Data Hold after WR	T_{CLCL} - 10		ns	Equal Loading
T_{WHDEX}	WR Inactive to DEN Inactive	T_{CLCH} - 10		ns	Equal Loading

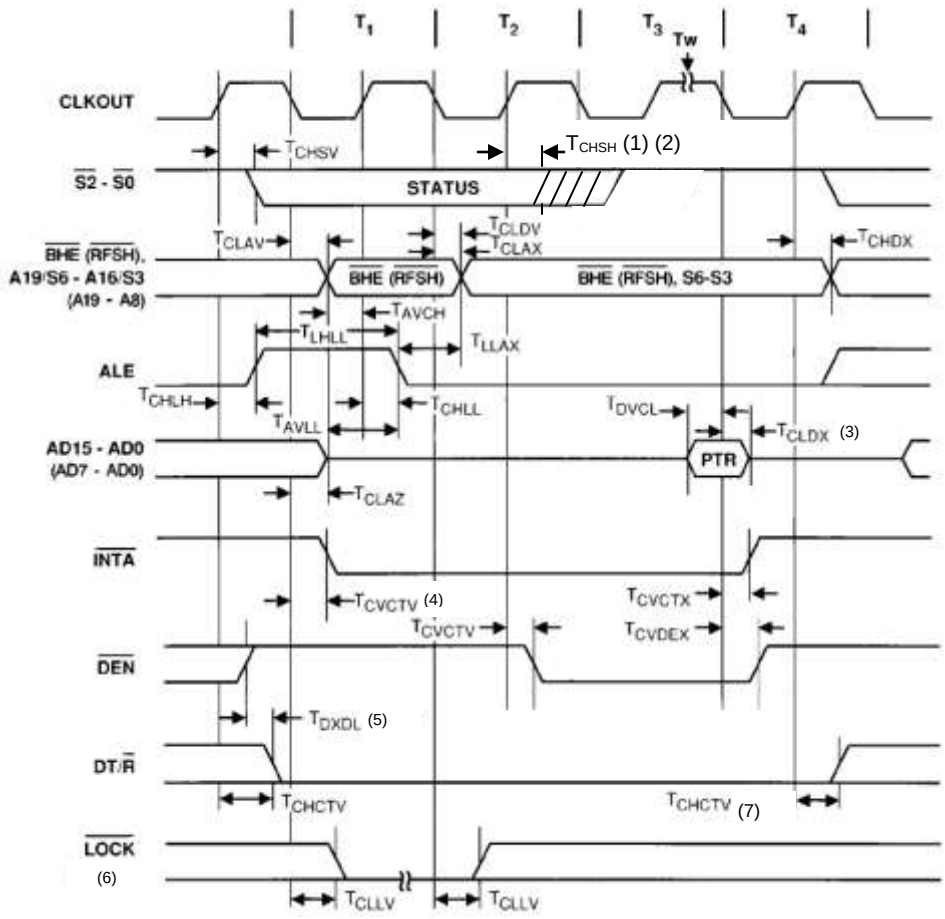


Figure 14. Interrupt Acknowledge Cycle Waveforms

Please note that pins indicated in the parentheses are for the IA188XL version.

Notes:

(1) The OEM part (80C186XL) operates differently in that it deasserts on the falling edge of CLKOUT.
(2) Status is inactive in the state preceding T4.
(3) The data hold time lasts only until INTA goes inactive, even if the INTA transition occurs prior to TCLDX (min).
(4) INTA occurs one clock later in Slave Mode.
(5) This applies when a write cycle is followed by an interrupt acknowledge cycle.
(6) LOCK is active upon T1 of the first interrupt acknowledge cycle, and inactive upon T2 of the second interrupt acknowledge cycle.
(7) Changes in T-state preceding next bus cycle if followed by write.

5.4 Software Halt Cycle Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 16. Software Halt Cycle Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CHSV}	Status Active Delay	3	20	ns	
T_{CHSH}	Status Inactive Delay	3	20	ns	
T_{CLAV}	Address Valid Delay	3	20	ns	
T_{CHLH}	ALE Active Delay		20	ns	
T_{LHLL}	ALE Width	T_{CLCL} - 15		ns	
T_{CHLL}	ALE Inactive Delay		20	ns	
T_{DXDL}	DEN Inactive to DT/R Low		0	ns	Equal Loading
T_{CHCTV}	Control Active Delay 2	3	20	ns	

5.5 Clock Timings

- T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
- All timings are measured at 1.5V and 50 pF loading on CLKOUT unless otherwise noted.
- All output test conditions are with C_L = 50 pF.
- For AC tests, input V_{IL} = 0.45V and V_{IH} = 2.4V except at X1 where $V_{IH} = V_{CC} – 0.5V$.

Table 17. Clock Timings

Symbol	Parameter	Values		Unit	Test Conditions
		Min	Max		
T_{CKIN}	CLKIN Period	20	∞	ns	
T_{CLCK}	CLKIN Low Time	8	∞	ns	1.5V(2)
T_{CHCK}	CLKIN High Time	8	∞	ns	1.5V(2)
T_{CKHL}	CLKIN Fall Time		5	ns	3.5 to 1.0V
T_{CKLH}	CLKIN Rise Time		5	ns	1.0 to 3.5V
T_{CICO}	CLKIN to CLKOUT Skew		17	ns	
T_{CLCL}	CLKOUT Period	40	∞	ns	
T_{CLCH}	CLKOUT Low Time	0.5 T_{CLCL} - 5		ns	C_L = 100 pF(3)
T_{CHCL}	CLKOUT High Time	0.5 T_{CLCL} - 5		ns	C_L = 100 pF(4)
T_{CH1CH2}	CLKOUT Rise Time		6	ns	1.0 to 3.5V
T_{CL2CL1}	CLKOUT Fall Time		6	ns	3.5 to 1.0V

NOTES:
1. External clock applied to X1 and X2 not connected.
2. T_{CLCK} and T_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of T_{CKIN}.
3. Tested under worst case conditions: V_{CC} = 5.5V. T_A = 70°C.
4. Tested under worst case conditions: V_{CC} = 4.5V. T_A = 0°C.

Table 20. Instruction Set Timing *(Continued)*

Instruction	Clock Cycles		Comments
	IA186XL	IA188XL	
JNS	3/5	3/5	Jump not taken/Jump taken
JNZ	3/5	3/5	
JO	3/5	3/5	
JP	3/5	3/5	
JPE	3/5	3/5	
JPO	3/5	3/5	
JS	3/5	3/5	
JZ	3/5	3/5	
LAHF	2	2	–
LDS	1/24	1/33	register/memory
LEA	3	3	–
LEAVE	12	12	–
LES	12	32	–
LOCK	1	1	–
LODS	8	12	–
LODS (repeated *n* times)	8+8*n*	12+12*n*	–
LOOP	3/4	3/4	Loop not taken/Loop taken
LOOPE	3/4	3/4	Loop not taken/Loop taken
LOOPNE	3/4	3/4	
LOOPNZ	3/4	3/4	
LOOPZ	3/4	3/4	
MOV Accumulator to memory	5	8/12	8-bit/16-bit
MOV Immediate to register	1	1	-
MOV Immediate to register/memory	1/5	1/12	register/memory
MOV Memory to accumulator	5	8/12	8-bit/16-bit
MOV Register to Register/Memory	2/5	2/20	register/memory
MOV Register/memory to register	2/5	2/20	
MOV Register/memory to segment register	2/5	2/20	
MOV Segment register to register/memory	2/5	2/20	
MOVS	24	32	–
MOVS (repeated *n* times)	24+24*n*	32+32*n*	–
MUL Memory-Byte	16	20	–
MUL Memory-Word	15	25	–
MUL Register-Byte	5	5	–
MUL Register-Word	5	5	–
NEG	1/32	1/15	register/memory
NOP	1	1	–
NOT	1/24	1/24	register/memory
OR Immediate to accumulator	1	1	–

Table 22. Innovasic Part Number Cross-Reference for the PQFP (Special Order only)

Innovasic Part Number	Intel Part Number	Package Type	Temperature Range
IA186XLPQF80IR1 (lead free–RoHS)	S80C186XL25 S80C186XL20 S80C186XL12 TS80C186XL25 TS80C186XL20 TS80C186XL12 EG80C186XL25 EG80C186XL20 ES80C186XL20	80-Lead PQFP	Industrial
IA188XLPQF80IR1 (lead free–RoHS)	S80C188XL25 S80C188XL20 S80C188XL12 TS80C188XL25 TS80C188XL20 TS80C188XL12 EG80C188XL25 EG80C188XL20 ES80C188XL20	80-Lead PQFP	Industrial

8. Errata

The following errata are associated with the IA186XL/IA188XL. A workaround to the identified problem has been provided where possible.

8.1 Summary

Table 24 presents a summary of errata.

Table 24. Summary of Errata

Errata No.	Problem	Ver. 0	Ver. 1	Ver. 2
1	Pin LOCK_n does not have an internal pullup and will float during reset and bus hold.	Exists	Exists	Exists
2	When the timer compare register for any of the timers is set to x0000, the max count is xFFFF instead of x10000 as in the OEM part.	Exists	Fixed	Fixed
3	When using external interrupts IRQ0 or IRQ1 in Cascade Mode, the acknowledge signal on INTA0 or INTA1 may be lost or truncated.	Exists	Fixed	Fixed
4	Memory->Memory moves interrupted by two DMA cycles can corrupt data.	Exists	Fixed	Fixed
5	Bit 15 of RELREG (offset 0xFE) behaves differently than Intel device.	Exists	Fixed	Fixed
6	Enhanced mode makes bit 15 of RELREG (offset 0xFE) read-only.	Exists	Fixed	Fixed
7	Sbus deasserts on the wrong edge of CLKOUT.	Exists	Fixed	Fixed
8	Timer2 count register must be written to enable counting.	Exists	Exists	Fixed
9	Non-maskable interrupt (NMI) can be pre-empted by maskable interrupt.	Exists	Exists	Fixed
10	DMA can hang.	Exists	Exists	Fixed

Errata No.	Problem	Ver. 0	Ver. 1	Ver. 2
11	MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.	Exists	Exists	Fixed
12	MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.	Exists	Exists	Fixed

8.2 Detail

Errata No. 1

Problem: Pin LOCK_n does not have an internal pullup.

Description: Because Pin LOCK_n does not have an internal pullup, it will float during reset and bus hold.

Workaround: An external pullup may be necessary if there is high external load on the signal.

Errata No. 2

Problem:
When the timer compare register for any of the timers is set to x0000, the max count is xFFFF instead of x10000 as in the OEM part.

Description: The timer output will change one count earlier than it should when the max count is set to x0000.

Workaround: The workaround is application dependent. Please contact Innovasic Technical Support if this erratum is an issue.

Errata No. 3

Problem:
When using external interrupts IRQ0 or IRQ1 in Cascade Mode, the acknowledge signal on INTA0 or INTA1 may be lost or truncated.

Description: The acknowledge for IRQ0 or IRQ1 will be lost or truncated in Cascade Mode if another interrupt, with a higher priority setting (as configured in the interrupt control registers), occurs just before or during the acknowledge. This does not apply to interrupts generated by the DMA. This also does not apply when using the inherent priority settings (all interrupts configured with the same priority).

Errata No. 5

Problem:
Bit 15 of RELREG (offset 0xFE) behaves differently than Intel device.

Description: For both 188 and 186 devices, an ESC opcode will generate a type 7 interrupt only when RELREG[15] is a 0.

Workaround: Initialize RELREG[15] to 0 if a type 7 interrupt is desired.

Errata No. 6

Problem:
Enhanced mode makes bit 15 of RELREG (offset 0xFE) read-only.

Description: If the device comes out of reset in enhanced mode, RELREG[15] will be set to a 1.

Workaround: Avoid enhanced mode if a type 7 interrupt is desired.

Errata No. 7

Problem:
Sbus deasserts on the wrong edge of CLKOUT.

Description: The sbus goes inactive (high) at the end of a bus cycle on the falling edge of CLKOUT. It should be on the rising edge of CLKOUT.

Workaround: None.

Errata No. 8

Problem:
Timer2 count register must be written to enable counting.

Description: If timer 2 count register is not explicitly written timer 2 will not count; this can also prevent timers 0 & 1 from counting if timer 2 is used as a prescaler.

Workaround: Write timer 2 count register before enabling timer 2.

Errata No. 9

Problem:
Non-maskable interrupt (NMI) can be pre-empted by maskable interrupt.

Description: When instruction execution unit is in Decode state for 2 or more consecutive cycles and an NMI is recognized, it could be pre-empted by a maskable interrupt.

Workaround: None.

Errata No. 10

Problem:
DMA can hang.

Description: DMA to a region of memory using destination synchronization and a chip select with extra wait states can hang.

Workaround: Do not use wait states and destination synchronization together.

Errata No. 11

Problem:
MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.

Description: MOVS/POP/PUSH instructions interrupted by both a DMA transaction and an instruction fetch bus cycle can corrupt data. *This affects the IA186XL only.*

Workaround: None.

Errata No. 12

Problem:
MOVS/POP/PUSH instructions interrupted by DMA can corrupt data.

Description: MOVS/PUSH/POP instructions with 16-bit, non-aligned destination address interrupted by DMA can corrupt data. *This affects the IA186XL only.*

Workaround: None.