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Details

Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	16MHz
Connectivity	SCI
Peripherals	PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3670fxv

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Table 2.3 Arithmetic Operations Instructions (1)

Instruction	Size*	Function
ADD SUB	B/W/L	$Rd \pm Rs \rightarrow Rd$, $Rd \pm \#IMM \rightarrow Rd$ Performs addition or subtraction on data in two general registers, or on immediate data and data in a general register (immediate byte data cannot be subtracted from byte data in a general register. Use the SUBX or ADD instruction.)
ADDX SUBX	B	$Rd \pm Rs \pm C \rightarrow Rd$, $Rd \pm \#IMM \pm C \rightarrow Rd$ Performs addition or subtraction with carry on byte data in two general registers, or on immediate data and data in a general register.
INC DEC	B/W/L	$Rd \pm 1 \rightarrow Rd$, $Rd \pm 2 \rightarrow Rd$ Increments or decrements a general register by 1 or 2. (Byte operands can be incremented or decremented by 1 only.)
ADDS SUBS	L	$Rd \pm 1 \rightarrow Rd$, $Rd \pm 2 \rightarrow Rd$, $Rd \pm 4 \rightarrow Rd$ Adds or subtracts the value 1, 2, or 4 to or from data in a 32-bit register.
DAA DAS	B	Rd decimal adjust $\rightarrow Rd$ Decimal-adjusts an addition or subtraction result in a general register by referring to the CCR to produce 4-bit BCD data.
MULXU	B/W	$Rd \times Rs \rightarrow Rd$ Performs unsigned multiplication on data in two general registers: either 8 bits $\times$ 8 bits $\rightarrow$ 16 bits or 16 bits $\times$ 16 bits $\rightarrow$ 32 bits.
MULXS	B/W	$Rd \times Rs \rightarrow Rd$ Performs signed multiplication on data in two general registers: either 8 bits $\times$ 8 bits $\rightarrow$ 16 bits or 16 bits $\times$ 16 bits $\rightarrow$ 32 bits.
DIVXU	B/W	$Rd \div Rs \rightarrow Rd$ Performs unsigned division on data in two general registers: either 16 bits $\div$ 8 bits $\rightarrow$ 8-bit quotient and 8-bit remainder or 32 bits $\div$ 16 bits $\rightarrow$ 16-bit quotient and 16-bit remainder.

Note: * Refers to the operand size.

B: Byte

W: Word

L: Longword

2.6.2 On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states or three states. The data bus width is 8 bits or 16 bits depending on the register. For description on the data bus width and number of accessing states of each register, refer to section 16.1, Register Addresses (Address Order). Registers with 16-bit data bus width can be accessed by word size only. Registers with 8-bit data bus width can be accessed by byte or word size. When a register with 8-bit data bus width is accessed by word size, access is completed in two cycles. In two-state access, the operation timing is the same as that for on-chip memory.

Figure 2.10 shows the operation timing in the case of three-state access to an on-chip peripheral module.

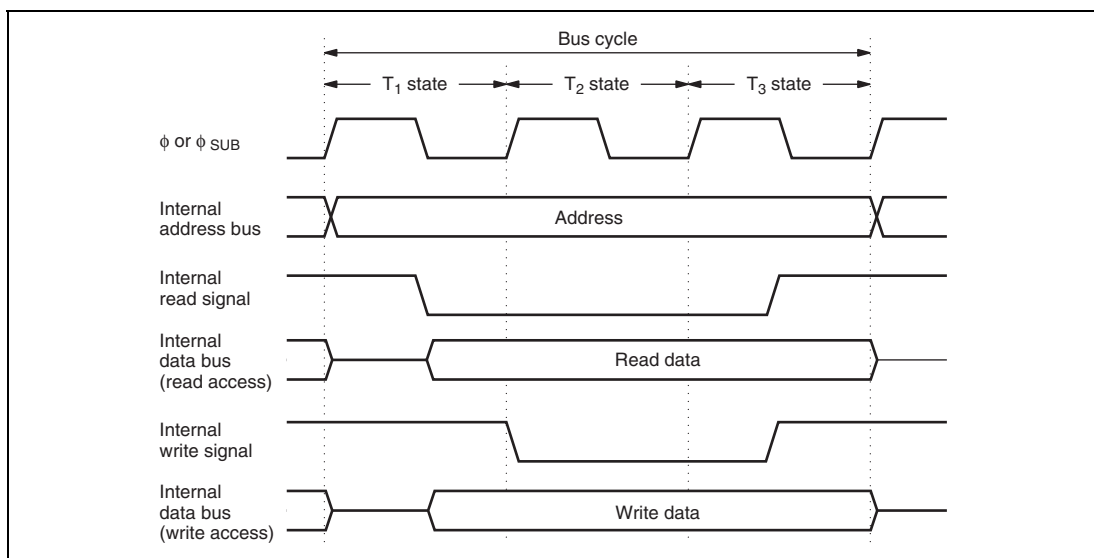


Figure 2.10 On-Chip Peripheral Module Access Cycle (3-State Access)

3.1 Exception Sources and Vector Address

Table 3.1 shows the vector addresses and priority of each exception handling. When more than one interrupt is requested, handling is performed from the interrupt with the highest priority.

Table 3.1 Exception Sources and Vector Address

Relative Module	Exception Sources	Vector Number	Vector Address	Priority	
RES pin	Reset	0	H'0000 to H'0001	High ↑ ↓ Low	
Watchdog timer					
—	Reserved for system use	1 to 6	H'0002 to H'000D		
External interrupt pin	NMI	7	H'000E to H'000F		
CPU	Trap instruction (#0)	8	H'0010 to H'0011		
	(#1)	9	H'0012 to H'0013		
	(#2)	10	H'0014 to H'0015		
	(#3)	11	H'0016 to H'0017		
Address break	Break conditions satisfied	12	H'0018 to H'0019		
CPU	Direct transition by executing the SLEEP instruction	13	H'001A to H'001B		
External interrupt pin	IRQ0	14	H'001C to H'001D		
	IRQ3	17	H'0022 to H'0023		
	WKP	18	H'0024 to H'0025		
—	Reserved for system use	20	H'0028 to H'0029		
Timer W	Input capture A/compare match A	21	H'002A to H'002B		
	Input capture B/compare match B				
	Input capture C/compare match C				
	Input capture D/compare match D				
	Timer W overflow				
Timer V	Timer V compare match A	22	H'002C to H'002D		
	Timer V compare match B				
	Timer V overflow				
SCI3	SCI3 receive data full	23	H'002E to H'002F		
	SCI3 transmit data empty				
	SCI3 transmit end				
	SCI3 receive error				
A/D converter	A/D conversion end	25	H'0032 to H'0033		

Section 4 Address Break

The address break simplifies on-board program debugging. It requests an address break interrupt when the set break condition is satisfied. The interrupt request is not affected by the I bit of CCR. Break conditions that can be set include instruction execution at a specific address and a combination of access and data at a specific address. With the address break function, the execution start point of a program containing a bug is detected and execution is branched to the correcting program. Figure 4.1 shows a block diagram of the address break.

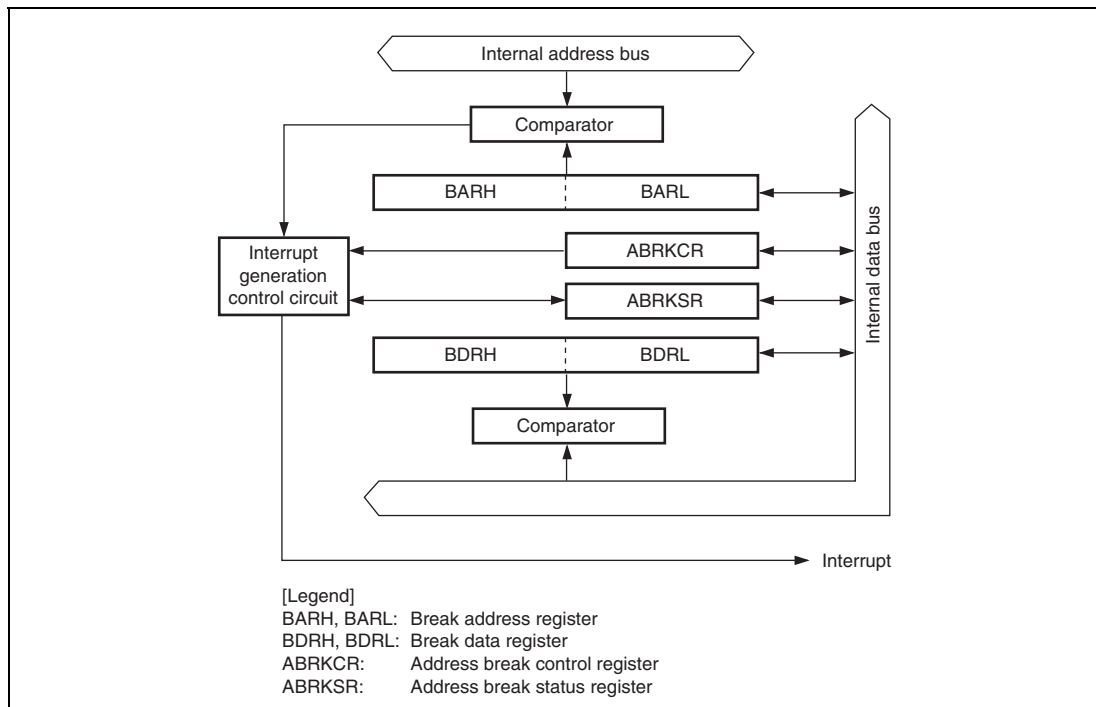


Figure 4.1 Block Diagram of Address Break

4.1 Register Descriptions

Address break has the following registers.

- Address break control register (ABRKCR)
- Address break status register (ABRKSR)
- Break address register (BARH, BARL)
- Break data register (BDRH, BDRL)

6.2 Mode Transitions and States of LSI

Figure 6.1 shows the possible transitions among these operating modes. A transition is made from the program execution state to the program halt state of the program by executing a SLEEP instruction. Interrupts allow for returning from the program halt state to the program execution state of the program. A direct transition from active mode to active mode changes the operating frequency. RES input enables transitions from a mode to the reset state. Table 6.2 shows the transition conditions of each mode after the SLEEP instruction is executed and a mode to return by an interrupt. Table 6.3 shows the internal states of the LSI in each mode.

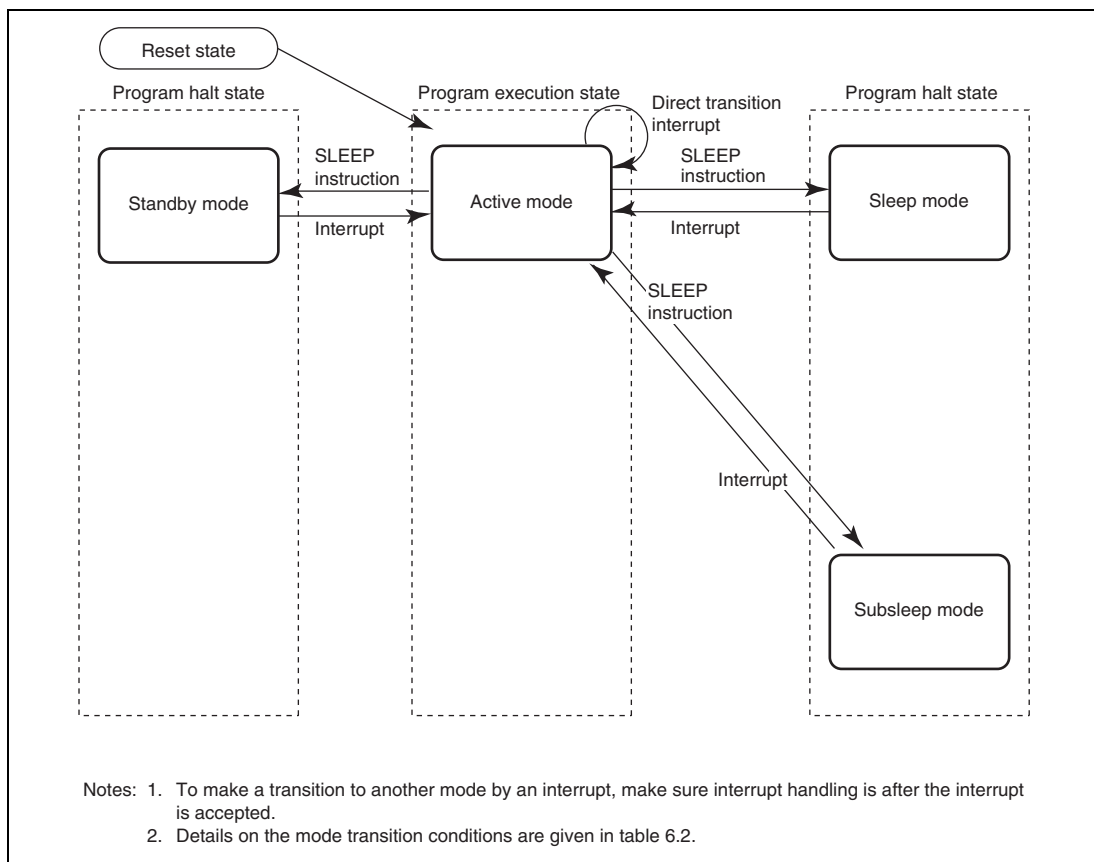
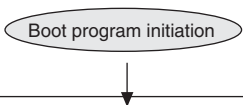


Figure 6.1 Mode Transition Diagram

Table 7.2 Boot Mode Operation

Item	Host Operation	Communication Contents	LSI Operation
	Processing Contents		Processing Contents
Boot mode initiation			Branches to boot program at reset-start. 
Bit rate adjustment	Continuously transmits data H'00 at specified bit rate. ↓ Transmits data H'55 when data H'00 is received error-free.	H'00, H'00 ... H'00 ↓ H'00 ↓ H'55	- Measures low-level period of receive data H'00. - Calculates bit rate and sets BRR in SCI3. - Transmits data H'00 to host as adjustment end indication. H'55 reception.
Flash memory erase	↓ Boot program erase error ↓ H'AA reception	H'FF ↓ H'AA	Checks flash memory data, erases all flash memory blocks in case of written data existing, and transmits data H'AA to host. (If erase could not be done, transmits data H'FF to host and aborts operation.)
Transfer of number of bytes of programming control program	Transmits number of bytes (N) of programming control program to be transferred as 2-byte data (low-order byte following high-order byte) ↓ Transmits 1-byte of programming control program (repeated for N times) ↓ H'AA reception	Upper bytes, lower bytes ↓ Echoback ↓ H'XX ↓ Echoback ↓ H'AA	Echobacks the 2-byte data received to host. ↓ Echobacks received data to host and also transfers it to RAM. (repeated for N times) ↓ Transmits data H'AA to host when data H'55 is received.
			Branches to programming control program transferred to on-chip RAM and starts execution.

5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower two bits are B'00. Verify data can be read in longwords from the address to which a dummy write was performed.
6. If the read data is not erased successfully, set erase mode again, and repeat the erase/erase-verify sequence as before. The maximum number of repetitions of the erase/erase-verify sequence is 100.

7.4.3 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including the $\overline{\text{NMI}}$ interrupt, are disabled while flash memory is being programmed or erased, or while the boot program is executing, for the following three reasons:

1. Interrupt during programming/erasing may cause a violation of the programming or erasing algorithm, with the result that normal operation cannot be assured.
2. If interrupt exception handling starts before the vector address is written or during programming/erasing, a correct vector cannot be fetched and the CPU malfunctions.
3. If an interrupt occurs during boot program execution, normal boot mode sequence cannot be carried out.

9.5.2 Port Data Register 8 (PDR8)

PDR8 is a general I/O port data register of port 8.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved
6	—	0	—	
5	—	0	—	
4	P84	0	R/W	PDR8 stores output data for port 8 pins.
3	P83	0	R/W	If PDR8 is read while PCR8 bits are set to 1, the value stored in PDR8 is read. If PDR8 is read while PCR8 bits are cleared to 0, the pin states are read regardless of the value stored in PDR8.
2	P82	0	R/W	
1	P81	0	R/W	
0	P80	0	R/W	

9.5.3 Pin Functions

The correspondence between the register specification and the port functions is shown below.

P84/FTIOD pin

Register	TIOR1			PCR8	
Bit Name	IOD2	IOD1	IOD0	PCR84	Pin Function
Setting Value	0	0	0	0	P84 input/FTIOD input pin
				1	P84 output/FTIOD input pin
	0	0	1	X	FTIOD output pin
	0	1	X	X	FTIOD output pin
	1	X	X	0	P84 input/FTIOD input pin
				1	P84 output/FTIOD input pin

Legend: X: Don't care.

10.2 Input/Output Pins

Table 10.1 shows the timer V pin configuration.

Table 10.1 Pin Configuration

Name	Abbreviation	I/O	Function
Timer V output	TMOV	Output	Timer V waveform output
Timer V clock input	TMCIV	Input	Clock input to TCNTV
Timer V reset input	TMRIV	Input	External input to reset TCNTV
Trigger input	TRGV	Input	Trigger input to initiate counting

10.3 Register Descriptions

Time V has the following registers.

- Timer counter V (TCNTV)
- Timer constant register A (TCORA)
- Timer constant register B (TCORB)
- Timer control register V0 (TCRV0)
- Timer control/status register V (TCSRv)
- Timer control register V1 (TCRV1)

10.3.1 Timer Counter V (TCNTV)

TCNTV is an 8-bit up-counter. The clock source is selected by bits CKS2 to CKS0 in timer control register V0 (TCRV0). The TCNTV value can be read and written by the CPU at any time. TCNTV can be cleared by an external reset input signal, or by compare match A or B. The clearing signal is selected by bits CCLR1 and CCLR0 in TCRV0.

When TCNTV overflows, OVF is set to 1 in timer control/status register V (TCSRv).

TCNTV is initialized to H'00.

10.6 Usage Notes

The following types of contention or operation can occur in timer V operation.

1. Writing to registers is performed in the T3 state of a TCNTV write cycle. If a TCNTV clear signal is generated in the T3 state of a TCNTV write cycle, as shown in figure 10.11, clearing takes precedence and the write to the counter is not carried out. If counting-up is generated in the T3 state of a TCNTV write cycle, writing takes precedence.
2. If a compare match is generated in the T3 state of a TCORA or TCORB write cycle, the write to TCORA or TCORB takes precedence and the compare match signal is inhibited. Figure 10.12 shows the timing.
3. If compare matches A and B occur simultaneously, any conflict between the output selections for compare match A and compare match B is resolved by the following priority: toggle output > output 1 > output 0.
4. Depending on the timing, TCNTV may be incremented by a switch between different internal clock sources. When TCNTV is internally clocked, an increment pulse is generated from the falling edge of an internal clock signal, that is divided system clock (ϕ). Therefore, as shown in figure 10.3 the switch is from a high clock signal to a low clock signal, the switchover is seen as a falling edge, causing TCNTV to increment. TCNTV can also be incremented by a switch between internal and external clocks.

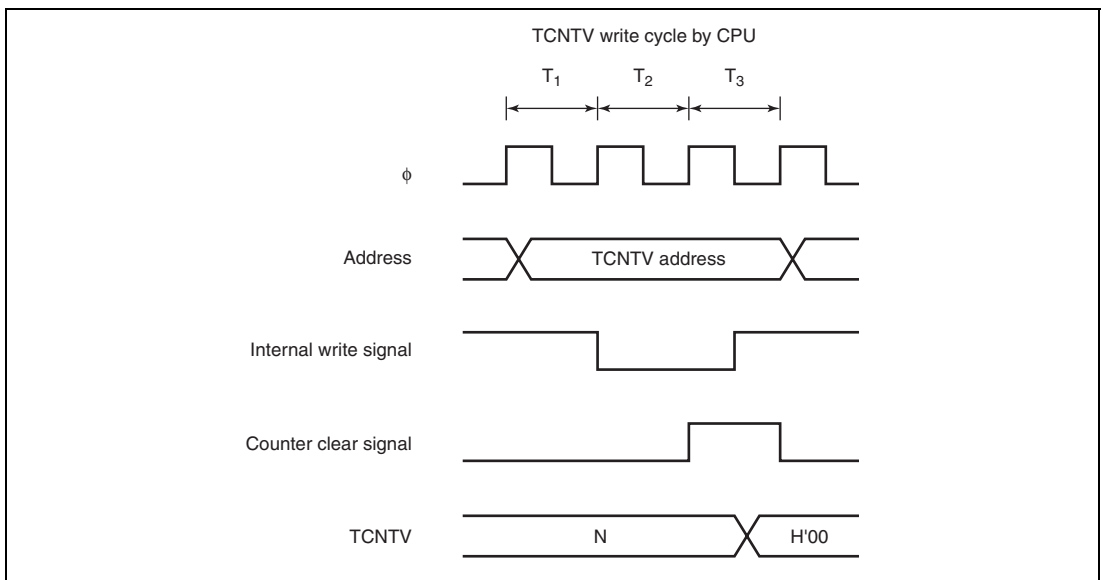


Figure 10.11 Contention between TCNTV Write and Clear

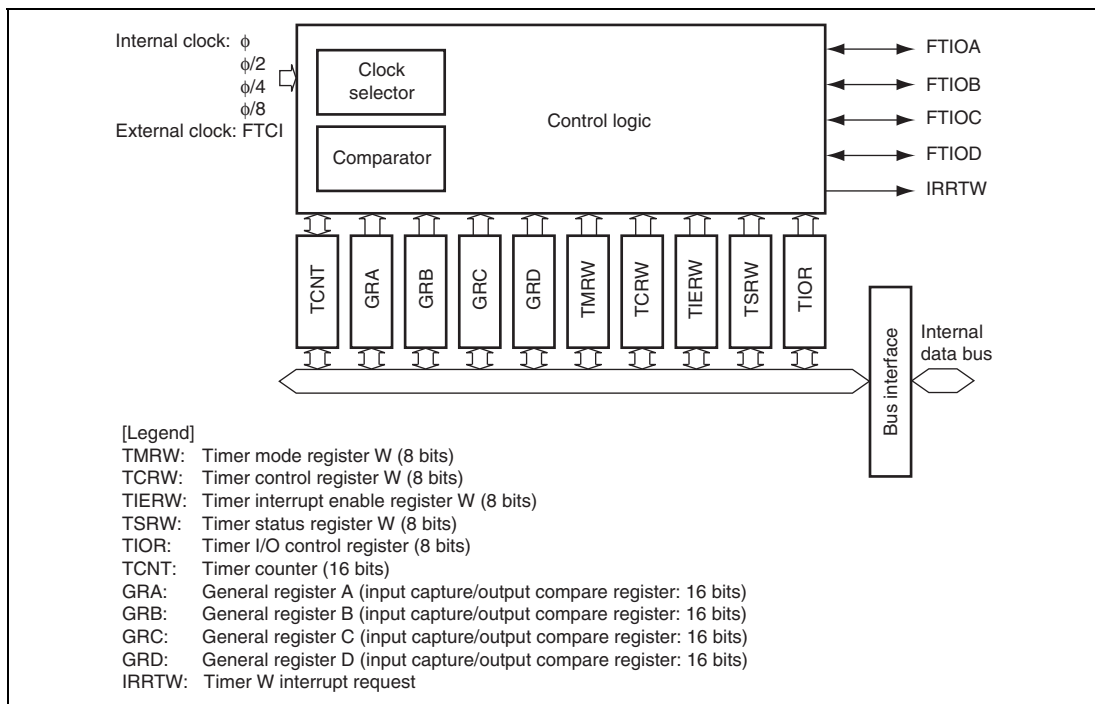


Figure 11.1 Timer W Block Diagram

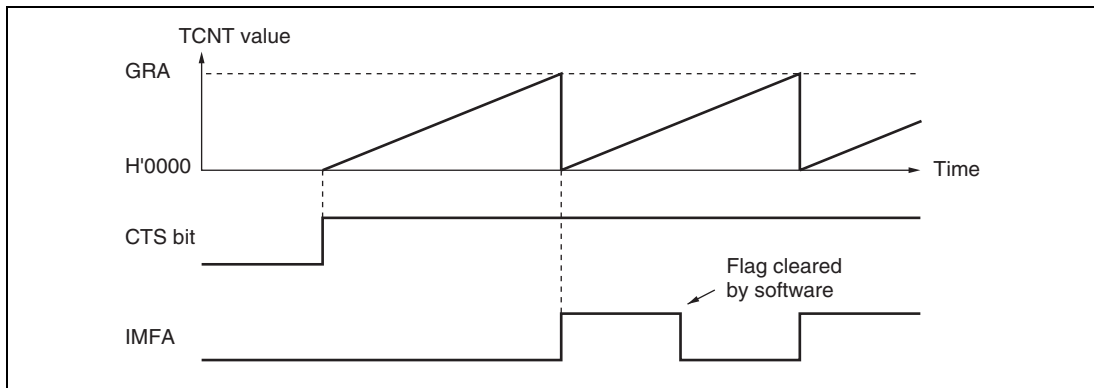


Figure 11.3 Periodic Counter Operation

By setting a general register as an output compare register, compare match A, B, C, or D can cause the output at the FTIOA, FTIOB, FTIOC, or FTIOD pin to output 0, output 1, or toggle. Figure 11.4 shows an example of 0 and 1 output when TCNT operates as a free-running counter, 1 output is selected for compare match A, and 0 output is selected for compare match B. When signal is already at the selected output level, the signal level does not change at compare match.

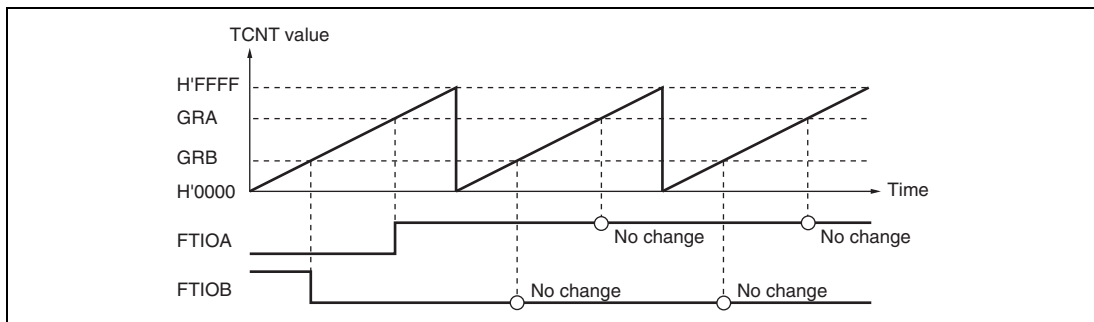
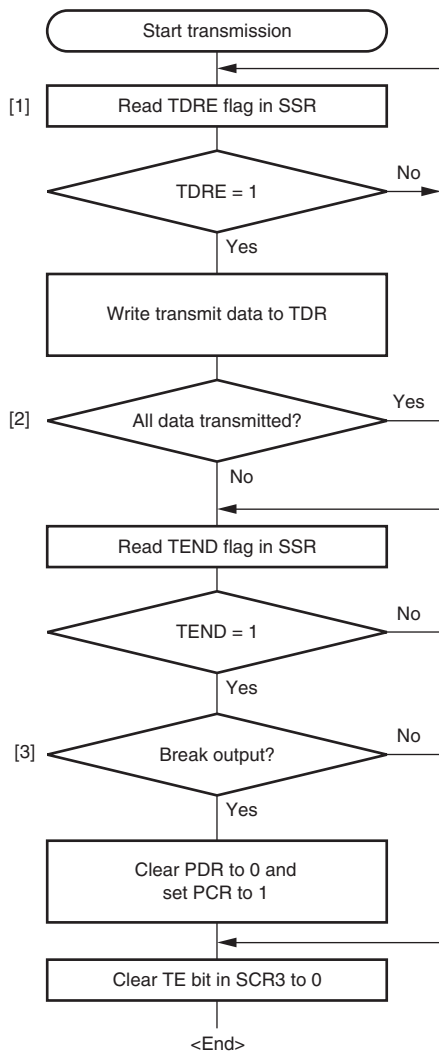


Figure 11.4 0 and 1 Output Example (TOA = 0, TOB = 1)

Figure 11.5 shows an example of toggle output when TCNT operates as a free-running counter, and toggle output is selected for both compare match A and B.



- [1] Read SSR and check that the TDRE flag is set to 1, then write transmit data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.
- [2] To continue serial transmission, read 1 from the TDRE flag to confirm that writing is possible, then write data to TDR. When data is written to TDR, the TDRE flag is automatically cleared to 0.
- [3] To output a break in serial transmission, after setting PCR to 1 and PDR to 0, clear TxD in PMR1 to 0, then clear the TE bit in SCR3 to 0.

Figure 13.6 Sample Serial Transmission Flowchart (Asynchronous Mode)

Section 14 A/D Converter

This LSI includes a successive approximation type 10-bit A/D converter that allows up to four analog input channels to be selected. The block diagram of the A/D converter is shown in figure 14.1.

14.1 Features

- 10-bit resolution
- Four input channels
- Conversion time: at least 4.4 μ s per channel (at 16 MHz operation)
- Two operating modes
 - Single mode: Single-channel A/D conversion
 - Scan mode: Continuous A/D conversion on 1 to 4 channels
- Four data registers
 - Conversion results are held in a 16-bit data register for each channel
- Sample and hold function
- Two conversion start methods
 - Software
 - External trigger signal
- Interrupt request
 - An A/D conversion end interrupt request (ADI) can be generated

Condition Code Notation

Symbol	Description
↕	Changed according to execution result
*	Undetermined (no guaranteed value)
0	Cleared to 0
1	Set to 1
—	Not affected by execution of the instruction
Δ	Varies depending on conditions, described in notes

Mnemonic		Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States ^{*1}	
			#xx	Rn	@ERn	@(d, ERn)	@-ERn/@ERn+	@aa	@(d, PC)	@@aa	I								Normal	Advanced
			I	H	N	Z	V	C												
JMP	JMP @ERn	—			2						PC ← ERn	—	—	—	—	—	4			
	JMP @aa:24	—					4				PC ← aa:24	—	—	—	—	—	6			
	JMP @@aa:8	—							2		PC ← @aa:8	—	—	—	—	—	8	10		
BSR	BSR d:8	—						2			PC → @-SP PC ← PC+d:8	—	—	—	—	—	6	8		
	BSR d:16	—						4			PC → @-SP PC ← PC+d:16	—	—	—	—	—	8	10		
JSR	JSR @ERn	—			2						PC → @-SP PC ← ERn	—	—	—	—	—	6	8		
	JSR @aa:24	—					4				PC → @-SP PC ← aa:24	—	—	—	—	—	8	10		
	JSR @@aa:8	—							2		PC → @-SP PC ← @aa:8	—	—	—	—	—	8	12		
RTS	RTS	—							2		PC ← @SP+	—	—	—	—	—	8	10		

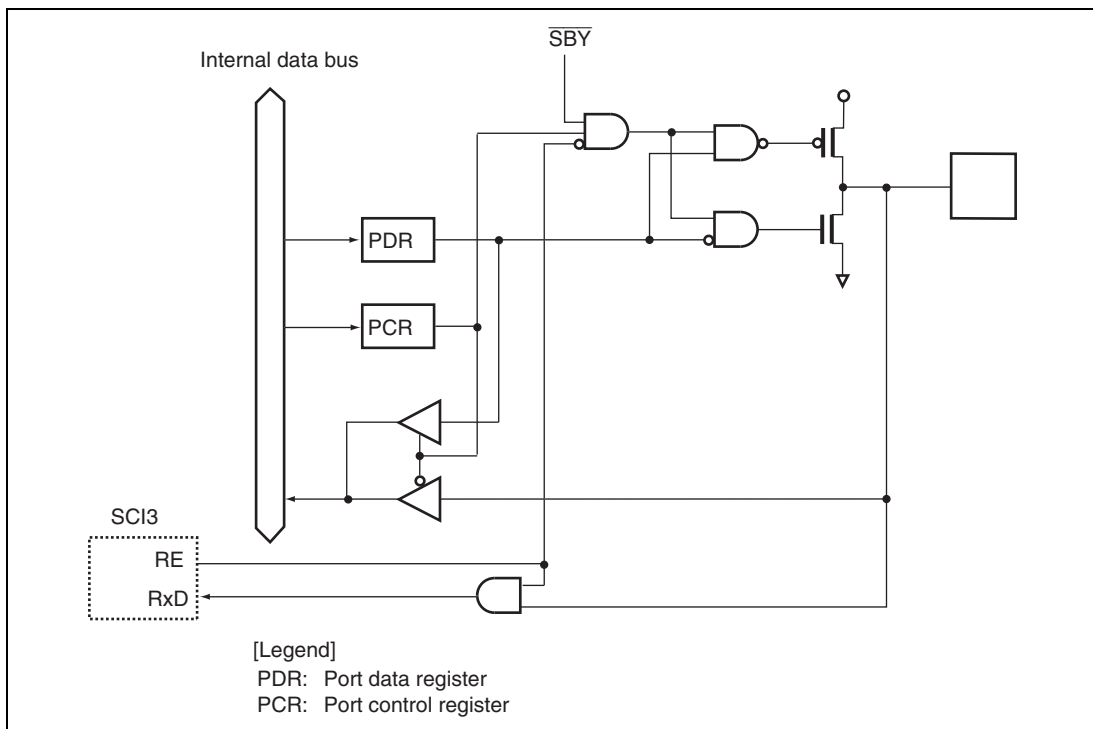


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R

Register

ABRCCR	56, 219, 222, 225
ABRKSR	57, 219, 222, 225
ADCR	208, 219, 222, 225
ADCSR	207, 219, 222, 225
ADDRA	206, 219, 222, 225
ADDRB	206, 219, 222, 225
ADDRC	206, 219, 222, 225
ADDRD	206, 219, 222, 225
BARH	58, 219, 222, 225
BARL.....	58, 219, 222, 225
BDRH	58, 219, 222, 225
BDRL.....	58, 219, 222, 225
BRR	172, 218, 221, 224
EBR1.....	82, 218, 221, 224
FENR	83, 218, 221, 224
FLMCR1	81, 218, 221, 224
FLMCR2.....	82, 218, 221, 224
GRA.....	141, 218, 221, 224
GRB.....	141, 218, 221, 224
GRC.....	141, 218, 221, 224
GRD.....	141, 218, 221, 224
IEGR1	43, 220, 223, 226
IEGR2.....	44, 220, 223, 226
IENR1	45, 220, 223, 226
IRR1.....	46, 220, 223, 226
IWPR	47, 220, 223, 226
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PCR1.....	97, 220, 223, 225
PCR2.....	100, 220, 223, 225
PCR5.....	104, 220, 223, 225
PCR7.....	108, 220, 223, 225
PCR8.....	110, 220, 223, 225
PDR1.....	97, 219, 222, 225
PDR2.....	101, 219, 222, 225
PDR5.....	104, 219, 222, 225
PDR7.....	108, 219, 222, 225
PDR8.....	111, 219, 222, 225
PDRB.....	114, 220, 223, 225