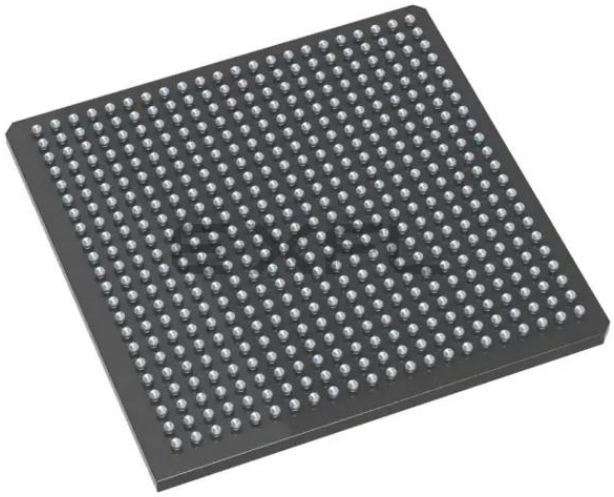

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Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	64KB
Peripherals	DDR
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 5K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s005s-1fgg484t2

Table 3 • **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Notes
Tj	Operating Junction Temperature	Automotive Grade 2	-40	25	125	°C	–
	Programming Junction Temperature	–	0	25	85	°C	–
		–	-40	25	100	°C	1
VDD	DC core supply voltage. Must always power this pin.	–	1.14	1.2	1.26	V	–
VPP	Power Supply for Charge Pumps (for Normal Operation and Programming) for 010 and 025 Devices	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
	Power Supply for Charge Pumps (for Normal Operation and Programming) for 090 devices	3.3 V Range	3.15	3.3	3.45	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0-5	2.5 V Range	2.375	2.5	2.625	V	–
		3.3 V Range	3.15	3.3	3.45	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V Range	2.375	2.5	2.625	V	2
		3.3 V Range	3.15	3.3	3.45	V	2

Table 15 • **Timing Model Parameters (continued)**

Index	Parameter	Description	Speed Grade –1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 38 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 28 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading

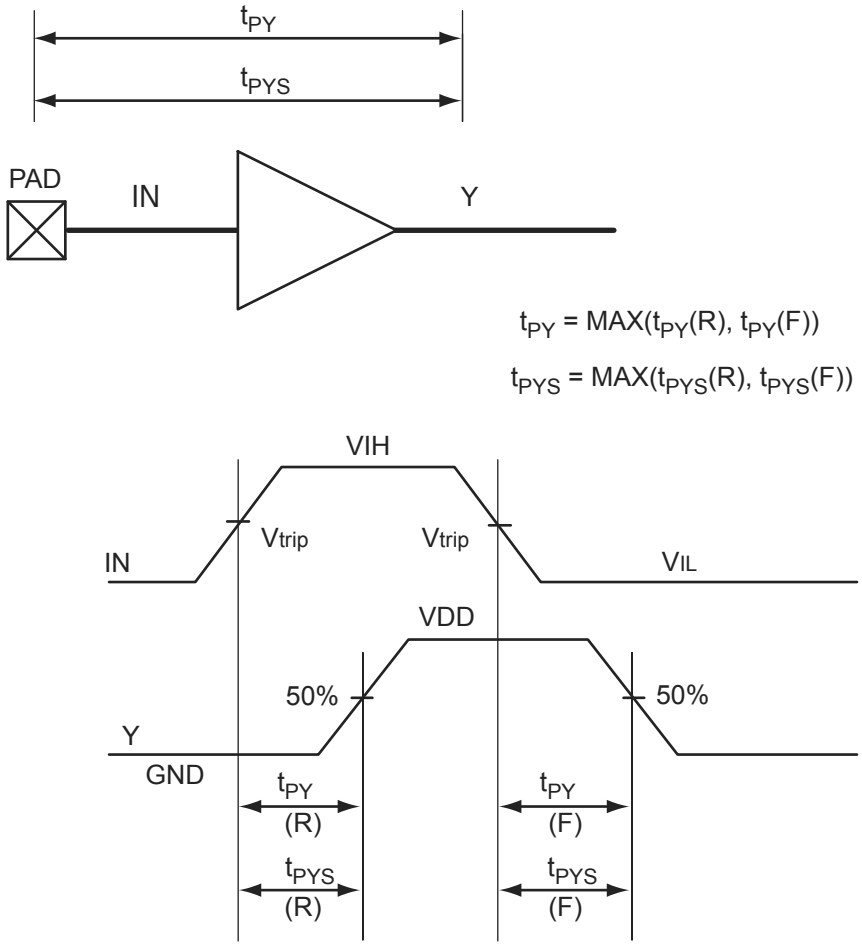

Figure 2 • **Input Buffer AC Loading**

8.2. Output Buffer and AC Loading

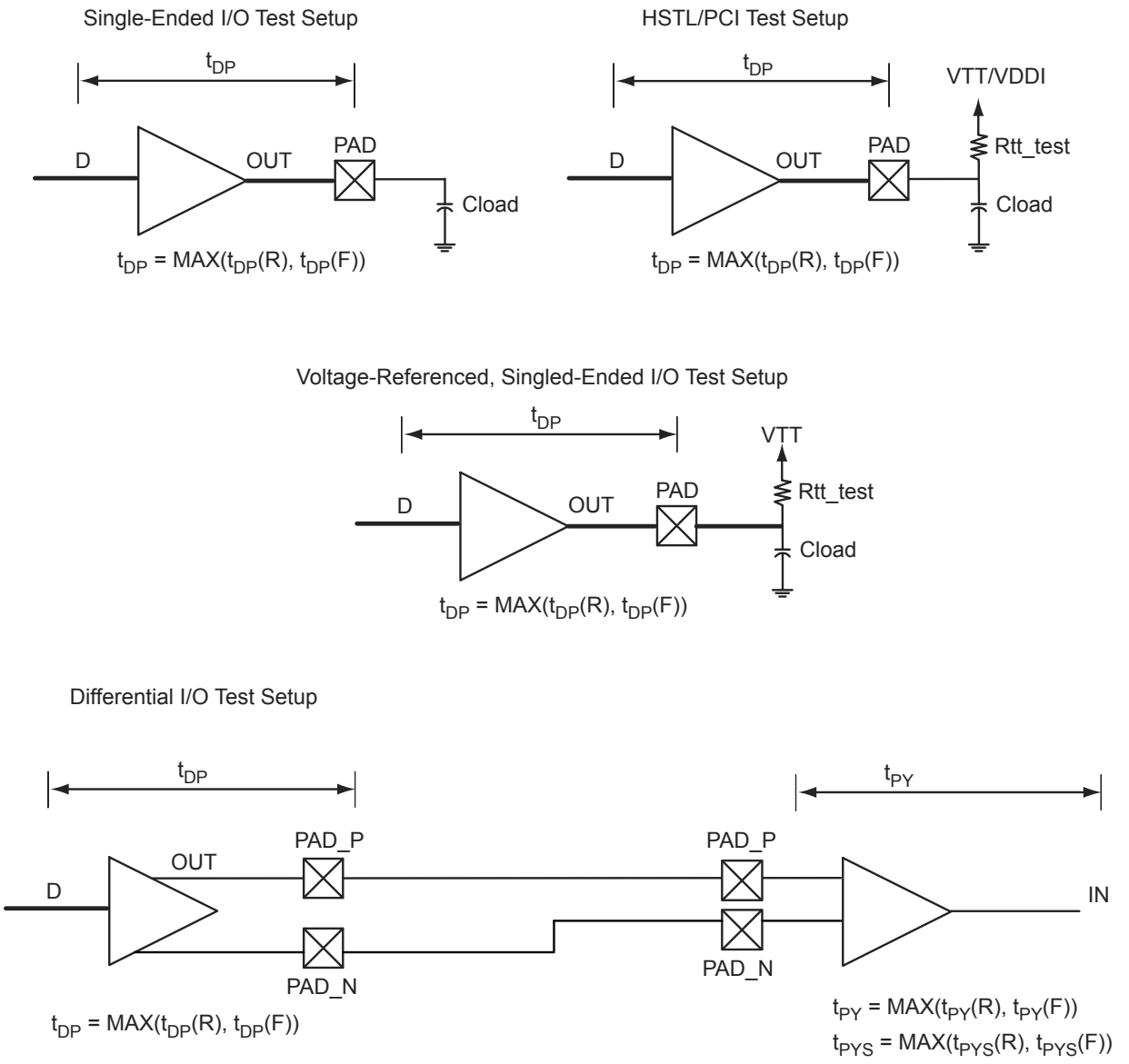

***Figure 3* • Output Buffer AC Loading**

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

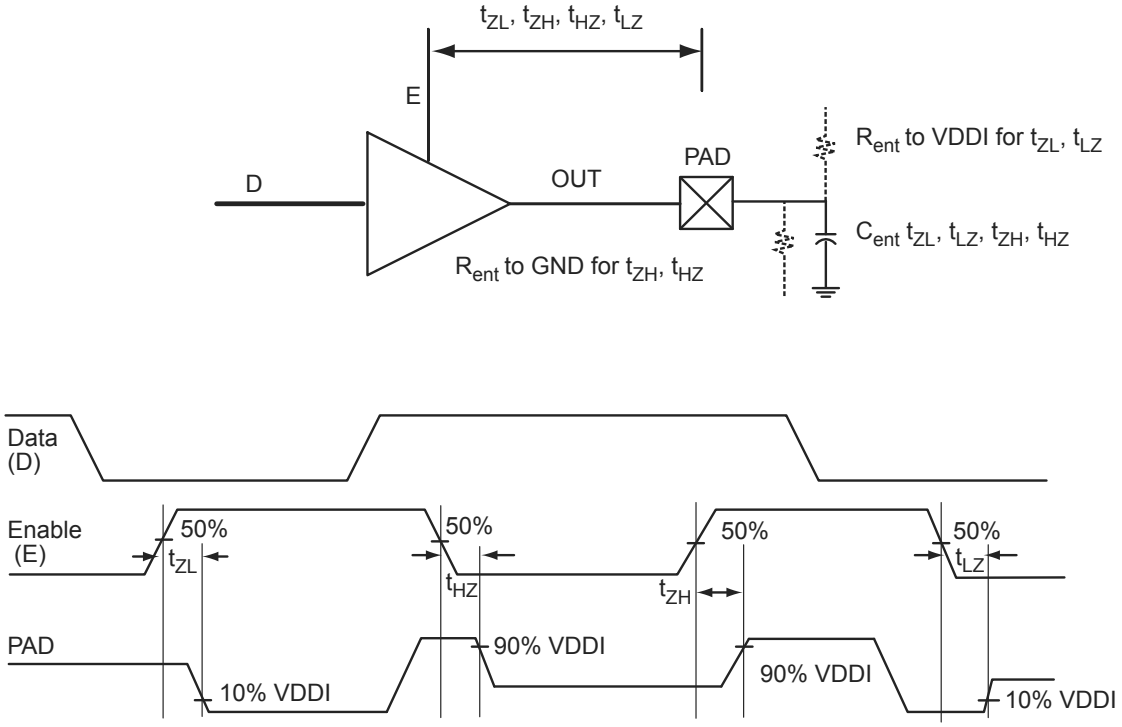

***Figure 4* • Tristate Buffer for Enable Path Test Point**

8.4 I/O Speeds

Table 16 • **Maximum Data Rate Summary for Worst-Case Automotive Grade 2 Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	560	–	–	Mbps
LVTTL 3.3 V	540	–	–	Mbps
LVCMOS 3.3 V	540	–	–	Mbps
LVCMOS 2.5 V	360	370	360	Mbps
LVCMOS 1.8 V	260	360	360	Mbps
LVCMOS 1.5 V	140	190	210	Mbps
LVCMOS 1.2 V	100	140	180	Mbps
LPDDR – LVCMOS 1.8 V Mode	–	–	360	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	360	Mbps
HSTL1.5 V	–	–	360	Mbps
SSTL 2.5 V	450	480	360	Mbps
SSTL 1.8 V	–	–	600	Mbps
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
SSTL 1.5 V	–	–	600	Mbps
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	810	–	–	Mbps
LVDS 3.3 V	480	480	–	Mbps
LVDS 2.5 V	480	480	–	Mbps
RSDS	460	480	–	Mbps
BLVDS	450	–	–	Mbps
MLVDS	450	–	–	Mbps
Mini-LVDS	460	480	–	Mbps

Table 17 • **Maximum Frequency Summary for Worst-Case Automotive Grade 2 Conditions**

Single-Ended I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
PCI 3.3 V	280	–	–	MHz
LVTTL 3.3 V	270	–	–	MHz
LVCMOS 3.3 V	270	–	–	MHz
LVCMOS 2.5 V	180	185	180	MHz
LVCMOS 1.8 V	130	180	180	MHz
LVCMOS 1.5 V	70	95	105	MHz
LVCMOS 1.2 V	50	70	90	MHz
LPDDR - LVCMOS 1.8 V mode	–	–	180	MHz
Voltage-Referenced I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LPDDR	–	–	180	MHz
HSTL1.5 V	–	–	180	MHz
SSTL 2.5 V	225	240	180	MHz
SSTL 1.8 V	–	–	300	MHz
SSTL 1.5 V	–	–	300	MHz
Differential I/O	**MSIO**	**MSIOD**	**DDRIO**	**Units**
LVPECL (input only)	405	–	–	MHz
LVDS 3.3 V	240	240	–	MHz
LVDS 2.5 V	240	240	–	MHz
RSDS	230	240	–	MHz
BLVDS	225	–	–	MHz
MLVDS	225	–	–	MHz
Mini-LVDS	230	240	–	MHz

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI=1.425 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
8 mA	slow	4.603	3.691	4.585	7.397	6.553	ns
	medium	4.081	3.242	4.062	7.064	6.189	ns
	medium_fast	3.827	3.015	3.804	6.912	6.051	ns
	fast	3.804	2.994	3.781	6.903	6.051	ns
10 mA	slow	4.519	3.612	4.499	7.578	6.676	ns
	medium	4.026	3.177	4.005	7.264	6.335	ns
	medium_fast	3.775	2.948	3.75	7.11	6.198	ns
	fast	3.747	2.929	3.721	7.103	6.19	ns
12 mA	slow	4.456	3.562	4.433	7.704	6.795	ns
	medium	3.965	3.13	3.943	7.388	6.425	ns
	medium_fast	3.731	2.912	3.704	7.278	6.303	ns
	fast	3.703	2.893	3.676	7.275	6.294	ns
LVCMOS 1.5 V (for MSIO I/O Bank)							
2 mA	slow	5.118	6.263	6.53	6.524	6.388	ns
4 mA	slow	4.657	5.178	5.65	8.57	7.55	ns
6 mA	slow	4.693	4.89	5.389	8.928	7.766	ns
8 mA	slow	4.876	4.663	5.183	9.59	8.173	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)							
2 mA	slow	3.085	3.795	4.086	6.838	6.477	ns
4 mA	slow	2.731	3.365	3.631	7.663	7.165	ns
6 mA	slow	2.742	3.162	3.417	8.126	7.52	ns

Table 49 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

8.6.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 50 • LVCMOS 1.2 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.14 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Codes)	None	2.539	2.556	ns
LVCMOS 1.2 V (for MSIO I/O Bank)	None	4.888	4.845	ns
	50	6.683	6.605	ns
	75	5.923	5.847	ns
	150	5.29	5.235	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)	None	4.281	4.235	ns
	50	6.806	6.721	ns
	75	5.643	5.564	ns
	150	4.813	4.753	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.14 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Code)							
2 mA	slow	6.938	5.599	6.948	7.568	6.612	ns
	medium	6.11	4.814	6.114	7.201	6.234	ns
	medium_fast	5.675	4.409	5.676	6.971	6.048	ns
	fast	5.633	4.379	5.634	6.958	6.037	ns
4 mA	slow	6.328	4.892	6.316	8.339	7.306	ns
	medium	5.538	4.192	5.521	7.961	6.923	ns
	medium_fast	5.119	3.832	5.097	7.76	6.741	ns
	fast	5.072	3.085	5.051	7.752	6.725	ns

Table 57 • HSTL AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
VDIFF	AC input differential voltage		0.4	–	–	V
Vx	AC differential cross point voltage		0.68	–	0.9	V
HSTL Maximum AC Switching Speed						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps
HSTL Impedance Specification						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
RTT	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for HSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for HSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • HSTL15 AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	ODT (On Die Termination) in Ω	t_{PY}	Units
		Speed Grade –1	
HSTL (for DDRIO I/O Bank with Fixed Code)			
Pseudo-Differential	None	1.673	ns
True-Differential	None	1.693	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
HSTL Class I (for DDRIO I/O Bank)						
Single Ended	2.922	2.91	2.904	3.225	3.218	ns
Differential	2.907	2.757	2.755	2.662	2.66	ns
HSTL Class II (for DDRIO I/O Bank)						
Single Ended	2.817	2.735	2.735	2.644	2.644	ns
Differential	2.827	2.81	2.803	3.205	3.197	ns

Table 62 • **DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t_{PY}	
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • **DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

Table 94 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 95 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 96 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

Table 109 • **Output/Enable Data Register Propagation Delays**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C,C	0.266	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable Register	E,E	0.065	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable Register	E,E	0.139	ns

8.10 DDR Module Specification

8.10.1 Input DDR Module

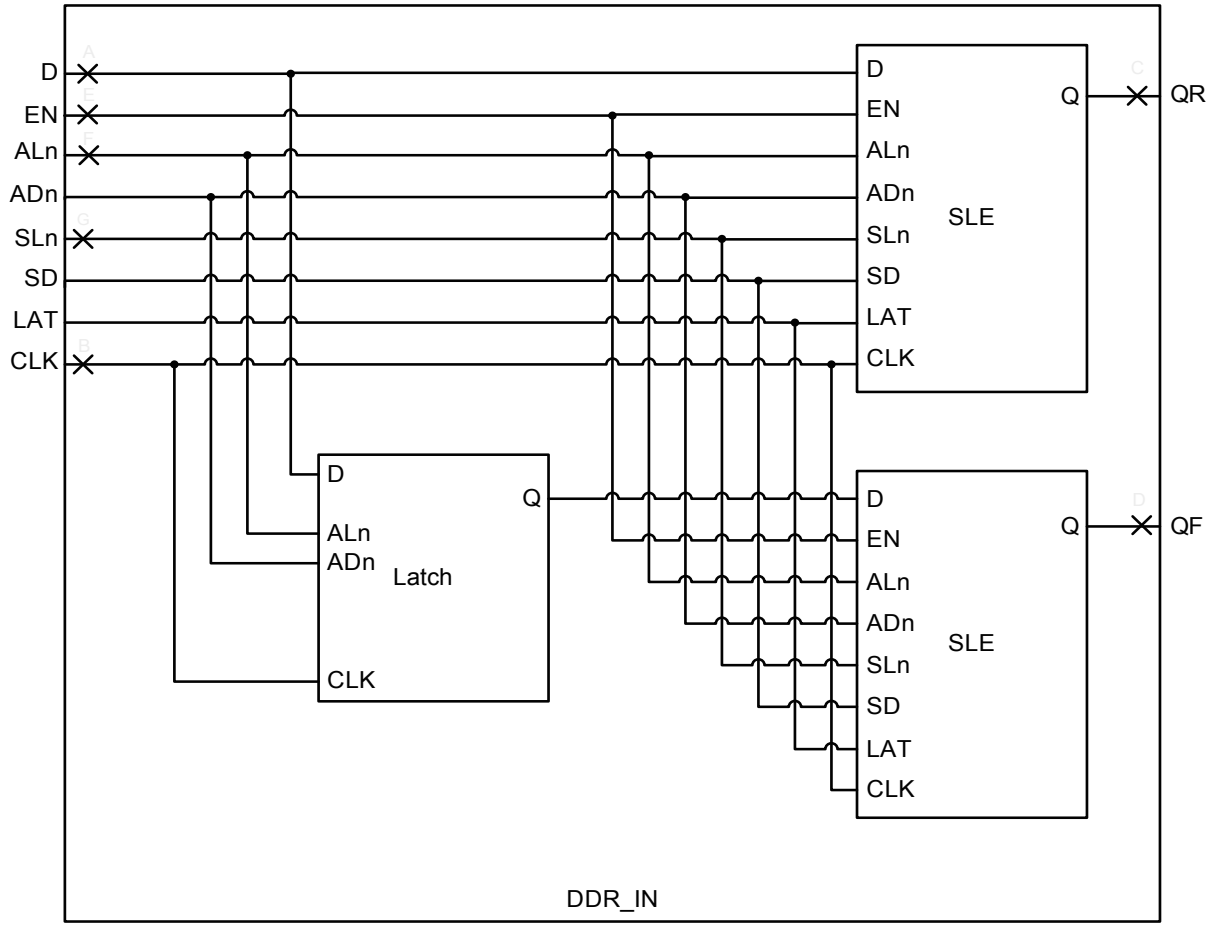

Figure 9 • **Input DDR Module**

8.10.5 Timing Characteristics

Table 111 • **Output DDR Propagation Delays**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E,G	0.272	ns
$t_{DDROSUDF}$	DF Data Setup for Output DDR	F,E	0.148	ns
$t_{DDROSUDR}$	DR Data Setup for Output DDR	A,E	0.196	ns
$t_{DDROHDF}$	DF Data Hold for Output DDR	F,E	0	ns
$t_{DDROHDR}$	DR Data Hold for Output DDR	A,E	0	ns
$t_{DDROSUE}$	Enable Setup for Output DDR	B,E	0.433	ns
t_{DDROHE}	Enable Hold for Output DDR	B,E	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Output DDR	D,E	0.203	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Output DDR	D,E	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C,G	0.545	ns
$t_{DDROREMAL}$	Asynchronous Load Removal time for Output DDR	C,E	0	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery time for Output DDR	C,E	0.035	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.266	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E,E	0.065	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.139	ns

11. FPGA Fabric SRAM

Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for more information.

11.1 FPGA Fabric Large SRAM (LSRAM)

Table 118 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1Kx18**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.578	ns
t_{ADDRSU}	Address Setup Time	0.455	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.352	–	ns
t_{DHD}	Data Hold Time	0.11	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.578	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.463	–	ns
t_{RDEHD}	Read Enable Hold Time	0.173	–	ns
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.473	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.631	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.34	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns

Table 127 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.24	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
Fmax	Maximum Frequency	–	250	MHz

Table 128 • uSRAM (RAM256x4) in 256x4 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.812	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.993	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.669	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.166	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.863	ns

Table 138 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification (continued)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Input Duty Cycle (Reference Clock)	Internal Feedback					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	10	–	90	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 100 MHz	25	–	75	%	–
	100 MHz ≤ f_{IN_CCC} ≤ 150 MHz	35	–	65	%	–
	150 MHz ≤ f_{IN_CCC} ≤ 200 MHz	45	–	55	%	–
	External Feedback (CCC, FPGA, Off-chip)					
	1 MHz ≤ f_{IN_CCC} ≤ 25 MHz	25	–	75	%	–
	25 MHz ≤ f_{IN_CCC} ≤ 35 MHz	35	–	65	%	–
	35 MHz ≤ f_{IN_CCC} ≤ 50 MHz	45	–	55	%	–
Output duty cycle	005, 010, and 025 Devices	46	–	52	%	–
	090 Devices	44	–	52	%	–
Spread Spectrum Characteristics						
Modulation frequency range	–	25	35	50	kHz	–
Modulation depth range	–	0	–	1.5	%	–
Modulation depth control	–	–	0.5	–	%	–

Notes:

1. *The minimum output clock frequency is limited by the PLL. For more information refer to the UG0449: SmartFusion2 and IGLOO2 Clocking Resources User Guide.*
2. *The PLL is used in conjunction with the Clock Conditioning Circuitry. Performance will be limited by the CCC output frequency.*

Table 139 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions/Package Combinations					Units	Notes
CCC Output Peak-to-Peak Period Jitter fOUT_CCC	–	–	–	–	–	–	–
010 FGG484 Packages	SSO = 0	0 < SSO <= 2	SSO <= 4	SSO <= 8	SSO <= 16	–	*
20 MHz to 100 MHz	Max(110, ± 1% x (1/fOUT_CCC))	Max(150, ± 1% x (1/fOUT_CCC))				ps	–
100 MHz to 400 MHz	120	150			170	ps	–
025 FGG484 Package	0 < SSO <=16						*
20 MHz to 74 MHz	± 1% x (1/fOUT_CCC)					ps	–
74 MHz to 400 MHz	210					ps	–
005 FGG484 Package	0 < SSO <=16						*
20 MHz to 53 MHz	± 1% x (1/fOUT_CCC)					ps	–
53 MHz to 400 MHz	270					ps	–
090 FGG484 and FGG676	0 < SSO <=16						*
20 MHz to 100 MHz	± 1% x (1/fOUT_CCC)					ps	–

Table 157 • **I2C Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 17 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	–	–	0.4	V	–
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	–
t_{OF}	Output fall time from VIHMin to VILMax	VIHmin to VILMax, Cload = 400 pF	–	21.04	–	ns	1
		VIHmin to VILMax, Cload = 100 pF	–	5.556	–	ns	–
t_{OR}	Output rise time from VILMax to VIHMin	VILMax to VIHmin, Cload = 400pF	–	19.887	–	ns	1
		VILMax to VIHmin, Cload = 100pF	–	5.218	–	ns	–
Rpull-up	Output buffer maximum pull-down resistance	–	–	–	50	Ω	2, 3
Rpull-down	Output buffer maximum pull-up resistance	–	–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	–
		Standard mode	–	–	100	Kbps	–
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	–

Notes:

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

Table 158 • **I2C Switching Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Definition	Conditions	Speed Grade –1		Units
			Min	Max	
t_{LOW}	Low period of I2C_x_SCL	–	1	–	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	1	–	pclk cycles
$t_{HD;STA}$	START hold time	–	1	–	pclk cycles
$t_{SU;STA}$	START setup time	–	1	–	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	1	–	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	1	–	pclk cycles
$t_{SU;STO}$	STOP setup time	–	1	–	pclk cycles

Table 159 • **SPI Characteristics (continued)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp3	**SPI_[0|1]_CLK minimum pulse width low**					
	SPI_[0|1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	0.385	–	–	µs	–
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%-90%)	–	2.77	–	ns	1
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%-90%)	–	2.906	–	ns	1
SPI Master Configuration						
sp6m	SPI_[0|1]_DO setup time	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0|1]_DO hold time	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0|1]_DI setup time	8	–	–	ns	2
sp9m	SPI_[0|1]_DI hold time	2.5	–	–	ns	2
SPI Slave Configuration						
sp6s	SPI_[0|1]_DO setup time	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0|1]_DO hold time	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0|1]_DI setup time	2	–	–	ns	2
sp9s	SPI_[0|1]_DI hold time	3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

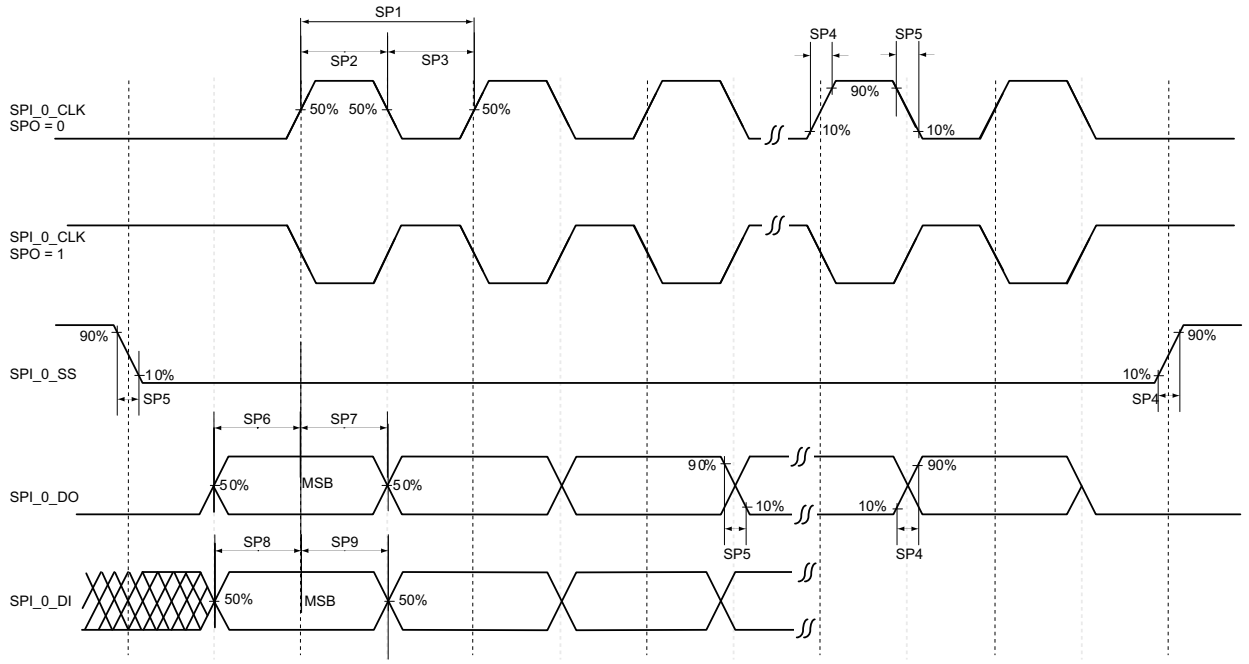

Figure 18 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**