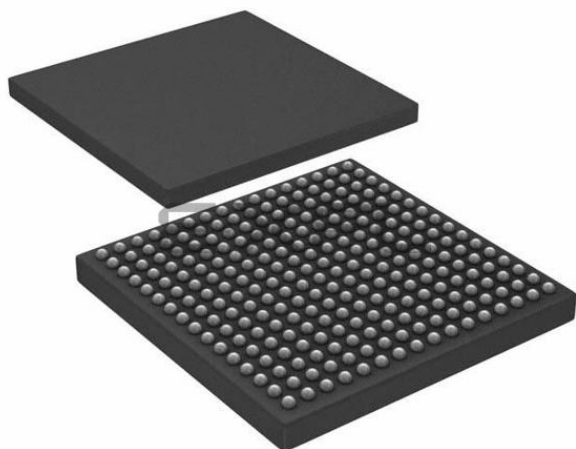




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What are [Embedded - System On Chip \(SoC\)](#)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	128KB
RAM Size	64KB
Peripherals	-
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 5K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s005s-1vfg256t2

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Table 57 • HSTL AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HSTL AC Differential Voltage Specifications						
V _{DIFF}	AC input differential voltage		0.4	–	–	V
V _x	AC differential cross point voltage		0.68	–	0.9	V
HSTL Maximum AC Switching Speed						
D _{max}	Maximum data rate	AC loading: per JEDEC specifications	–	–	360	Mbps
HSTL Impedance Specification						
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ω	–	25.5, 47.8	–	Ω
R _{TT}	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ω	–	47.8	–	Ω
HSTL AC Test Parameters Specification						
V _{trip}	Measuring/trip point for data path		–	0.75	–	V
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF
R _{tt_test}	Reference resistance for data test path for HSTL15 Class I (t _{DP})		–	50	–	Ω
R _{tt_test}	Reference resistance for data test path for HSTL15 Class II (t _{DP})		–	25	–	Ω
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF

8.7.1.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • HSTL15 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	ODT (On Die Termination) in Ω	t_{py}	Units
		Speed Grade –1	
HSTL (for DDRIO I/O Bank with Fixed Code)			
Pseudo-Differential	None	1.673	ns
True-Differential	None	1.693	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • HSTL 15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
HSTL Class I (for DDRIO I/O Bank)						
Single Ended	2.922	2.91	2.904	3.225	3.218	ns
Differential	2.907	2.757	2.755	2.662	2.66	ns
HSTL Class II (for DDRIO I/O Bank)						
Single Ended	2.817	2.735	2.735	2.644	2.644	ns
Differential	2.827	2.81	2.803	3.205	3.197	ns

8.7.2 Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.7.3 Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.7.3.1 Minimum and Maximum DC Input and Output Levels Specification

Table 60 • DDR1/SSTL2 Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply voltage	2.375	2.5	2.625	V
VTT	Termination voltage	1.164	1.250	1.339	V
VREF	Input reference voltage	1.164	1.250	1.339	V
SSTL2 DC Input Voltage Specification					
VIH (DC)	DC input logic High	VREF + 0.15	–	2.625	V
VIL (DC)	DC input logic Low	–0.3	–	VREF – 0.15	V
IIH (DC)	Input current High	–	–	10	μA
IIL (DC)	Input current Low	–	–	10	μA
SSTL2 DC Output Voltage Specification					
SSTL2 Class I (DDR Reduced Drive)					
VOH	DC output logic High	VTT + 0.608	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.608	V
IOH at VOH	Output minimum source DC current	8.1	–	–	mA
IOL at VOL	Output minimum sink current	–8.1	–	–	mA
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks Only					
VOH	DC output logic High	VTT + 0.81	–	–	V
VOL	DC output logic Low	–	–	VTT – 0.81	V
IOH at VOH	Output minimum source DC current	16.2	–	–	mA
IOL at VOL	Output minimum sink current	–16.2	–	–	mA
SSTL2 DC Differential Voltage Specification					
VID (DC)	DC input differential voltage	0.3	–	–	V

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1	Units
		t _{py}	
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

Table 65 • DDR2/SSTL18 AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL18 AC Differential Voltage Specification						
VDIFF (AC)	AC input differential voltage		0.5	–	–	V
Vx (AC)	AC differential cross point voltage		$0.5 \times VDDI - 0.175$	–	$0.5 \times VDDI + 0.175$	V
SSTL18 Maximum AC Switching Speed						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specification	–	–	600	Mbps
SSTL18 Impedance Specifications						
Rref	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 150 Ω	–	50, 75, 150	–	Ω
SSTL18 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.9	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL18 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL18 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 66 • DDR2/SSTL18 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 1.71\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t _{py}	
SSTL18 (for DDRIO I/O Bank with Fixed Codes)			
Pseudo differential	None	1.633	ns
True differential	None	1.65	ns

Table 79 • LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedance Option						
Rodt_cal	Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	5	–	pF
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

Table 80 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	–
8 mA	VDDI – 0.45	0.45	8	8	–
10 mA	VDDI – 0.45	0.45	10	10	–
12 mA	VDDI – 0.45	0.45	12	12	–
16 mA	VDDI – 0.45	0.45	16	16	*
Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance					

8.7.6.4 AC Switching Characteristics

Table 81 • LPPDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 83 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID	Input differential voltage		100	350	600	mV

Table 84 • LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	480	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
LVDS Impedance Specification						
Rt	Termination resistance	–	–	100	–	Ω
LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

Table 101 • RSDS DC Voltage Specification (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
VICM	Input common mode voltage		0.3	–	1.5	V
VID	Input differential voltage		100	–	600	mV

Table 102 • RSDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
RSDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
RSDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
RSDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 103 • RSDS AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Automotive Grade 2 conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{pY}	
RSDS (for MSIO I/O Bank)	None	3.112	ns
	100	3.108	ns
RSDS (for MSIOD I/O Bank)	None	2.832	ns
	100	2.821	ns

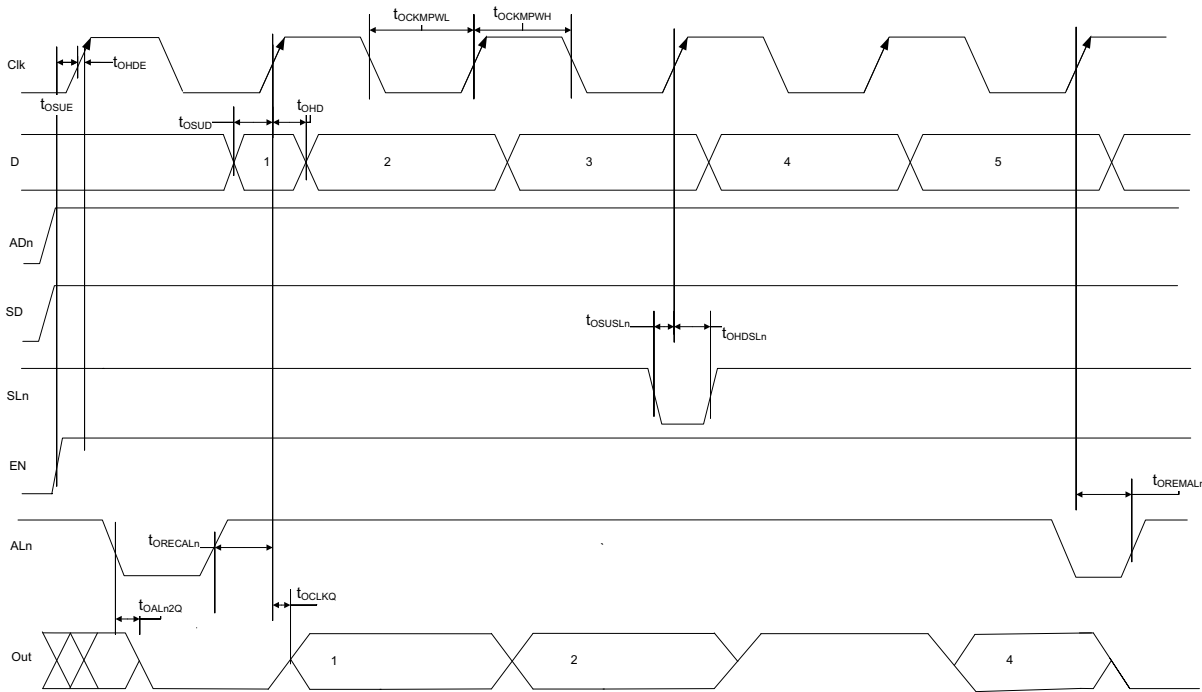


Figure 8 • I/O Register Output Timing Diagram

Table 109 • Output/Enable Data Register Propagation Delays
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade -1	Units
t_{OBYP}	Bypass Delay of the Output/Enable Register	F,G or H,I	0.364	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E,G or E,I	0.272	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A,E or J,E	0.196	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A,E or J,E	0	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B,E	0.433	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B,E	0	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D,E	0.203	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D,E	0	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register ($ADn=1$)	C,G or C,I	0.523	ns
	Asynchronous Preset-to-Q of the Output/Enable Register ($ADn=0$)	C,G or C,I	0.545	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable Register	C,E	0	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable Register	C,E	0.035	ns

9. Logic Element Specifications

9.1 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *SmartFusion2 and IGLOO2 Macro Library Guide*.

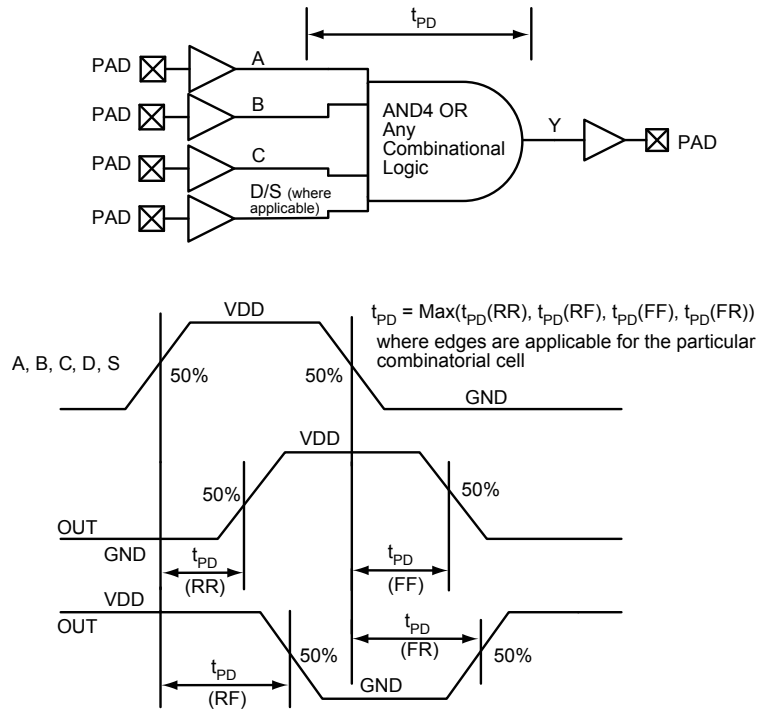


Figure 13 • LUT-4

9.1.1 Timing Characteristics

Table 112 • Combinatorial Cell Propagation Delays
Worst-Case Automotive Grade 2 Conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Speed Grade -1	Units
INV	$Y = !A$	t_{PD}	0.106	ns
AND2	$Y = A \cdot B$	t_{PD}	0.17	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.157	ns
OR2	$Y = A + B$	t_{PD}	0.17	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.157	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.17	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.236	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.217	ns
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.384	ns

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.546	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns
t_{RDPLESU}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t_{RDPLEHD}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.583	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t_{PLRSTREM}	Pipelined Register Asynchronous Reset Removal Time	–0.288	–	ns
t_{PLRSTREC}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t_{PLRSTMPW}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.504	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
F_{max}	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
t_{CLKMPWH}	Clock Minimum Pulse Width High	1.5	–	ns
t_{CLKMPWL}	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{\text{PLCLKMPWH}}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{\text{PLCLKMPWL}}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns

Table 124 • uSRAM (RAM64x18) in 64x18 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{DINCHD}	Write Input Data hold Time	0.155	–	ns
t_{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t_{ADDRCHD}	Write Address Hold Time	0.132	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 125 • uSRAM (RAM64x16) in 64x16 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
t_{CLKMPWH}	Read Clock Minimum Pulse Width High	1.8	–	ns
t_{CLKMPWL}	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{\text{PLCLKMPWH}}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{\text{PLCLKMPWL}}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.738	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.916	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.094	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.803	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.102	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns

Table 127 • uSRAM (RAM128x8) in 128x8 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8	–	ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.276	ns
	Read Access Time without Pipeline Register	–	1.776	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	1.959	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.125	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.704	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.14	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.865	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.104	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns

Table 129 • uSRAM (RAM512x2) in 512x2 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
t_{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t_{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.104	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
t_{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t_{ADDRCHD}	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

Table 130 • uSRAM (RAM1024x1) in 1024x1 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade -1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
t_{CLKMPWH}	Read Clock Minimum Pulse Width High	1.8	–	ns
t_{CLKMPWL}	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{\text{PLCLKMPWH}}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{\text{PLCLKMPWL}}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns

Table 139 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Conditions/Package Combinations	Units	Notes
100 MHz to 400 MHz	150	ps	–
Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.			

16. JTAG

Table 140 • JTAG 1532

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1 Speed Grade				Units
		005	010	025	090	
t_{TCK2Q}	Clock to Q (data out)	7.71	7.91	7.95	9.21	ns
t_{RSTB2Q}	Reset to Q (data out)	7.91	6.54	6.27	7.94	ns
t_{DISU}	Test Data Input Setup Time	-1.07	-0.70	-0.70	-1.33	ns
t_{DIHD}	Test Data Input Hold Time	2.43	2.38	2.47	2.71	ns
t_{TMSSU}	Test Mode Select Setup Time	-0.75	-0.86	-1.13	-1.03	ns
t_{TMDHD}	Test Mode Select Hold Time	1.41	1.48	1.98	1.69	ns
t_{TRSTREM}	ResetB Removal Time	-0.81	-1.1	-1.38	-0.8	ns
t_{TRSTREC}	ResetB Recovery Time	-0.81	-1.1	-1.38	-0.8	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	MHz

17. DEVRST_N Characteristics

Table 141 • DEVRST_N Characteristics

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	All Devices/Speed Grades			Units	Notes
		Min	Typ	Max		
TRAMPDEVRSTN	DEVRST_N ramp rate	–	–	10	ns	*
Note: * Slower ramp rates are susceptible to board level noise.						

18. System Controller SPI Characteristics

Table 142 • System Controller SPI Characteristics
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–
Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models . Use the supported I/O Configurations for the System Controller SPI in Table 143.							

Table 143 • Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

19. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 144 • Mathblocks With All Registers Used
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With All Registers Used		Speed Grade –1		Units
Parameter	Description	Min	Max	
t_{MISU}	Input, Control Register Setup time	0.149	–	ns
t_{MIHD}	Input, Control Register Hold time	0.08	–	ns
t_{MOCDSU}	CDIN Input Setup time	1.68	–	ns
t_{MOCDSHD}	CDIN Input Hold time	-0.419	–	ns
$t_{\text{MSRSTENSU}}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{\text{MSRSTENHD}}$	Synchronous Reset/Enable Hold time	0.011	–	ns
t_{MARSTREM}	Asynchronous Reset Removal time	0	–	ns
t_{MARSTREC}	Asynchronous Reset Recovery time	0.088	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.245	–	ns

Table 145 • Mathblock With Input Bypassed and Output Registers Used
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Bypassed and Output Registers Used		Speed Grade –1		Units
Parameter	Description	Min	Max	
t_{MOSU}	Output Register Setup time	2.294	–	ns
t_{MOHD}	Output Register Hold time	-0.444	–	ns
t_{MOCDSU}	CDIN Input Setup time	1.68	–	ns
t_{MOCDSHD}	CDIN Input Hold time	-0.419	–	ns
$t_{\text{MSRSTENSU}}$	Synchronous Reset/Enable Setup time	0.115	–	ns
$t_{\text{MSRSTENHD}}$	Synchronous Reset/Enable Hold time	0.011	–	ns
t_{MARSTREM}	Asynchronous Reset Removal time	0	–	ns
t_{MARSTREC}	Asynchronous Reset Recovery time	0.014	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.179	–	ns