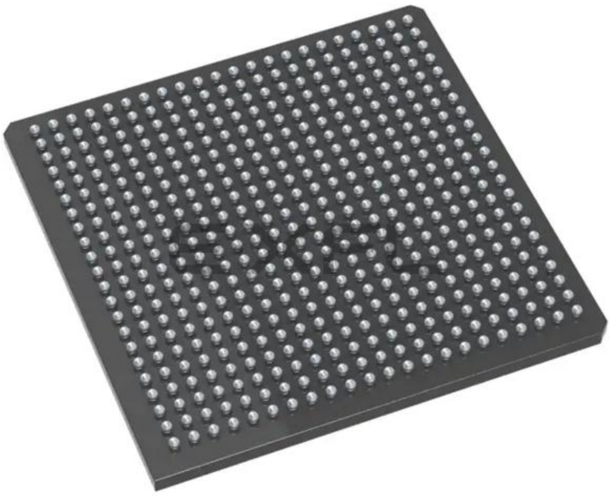

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 10K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s010ts-1fgg484t2

Table 5 • Embedded Flash Limits

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Automotive Grade 2	Embedded flash	Min T_J = -40°C Max T_J = 125°C	Min T_J = -40°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • Device Storage Temperature and Retention

Product Grade	Storage Temperature (Tstg)	Retention
Automotive Grade 2	Min T_J = -40°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3 Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA}			θ_{JB}	θ_{JC}	Units
	Still Air	1.0 m/s	2.5 m/s			
005						
FGG484	19.36	15.81	14.63	9.74	5.27	°C/W
VFG256	41.30	38.16	35.30	28.41	3.94	°C/W
VFG400	20.19	16.94	15.41	8.86	4.95	°C/W
010						
FGG484	18.22	14.83	13.62	8.83	4.92	°C/W
VFG256	37.36	34.26	31.45	24.84	7.89	°C/W
VFG400	19.40	15.75	14.22	8.11	4.22	°C/W
025						
FGG484	17.03	13.66	12.45	7.66	4.18	°C/W
VFG256	33.85	30.59	27.85	21.63	6.13	°C/W
VFG400	18.36	14.89	13.36	7.12	3.41	°C/W
060						
FGG484	15.40	12.06	10.85	6.14	3.15	°C/W
VFG400	17.45	14.01	12.47	6.22	2.69	°C/W
FGG676	15.49	12.21	11.06	7.07	3.87	°C/W
090						
FGG484	14.64	11.37	10.16	5.43	2.77	°C/W
FGG676	14.52	11.19	10.37	6.17	3.24	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 125°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL060TS-1FGG484 package at Automotive Grade 2 temperature and in still air, where:

θ_{JA} = 15.4°C/W (taken from Table 7 on page 6).

T_A = 105°C

$$\text{Maximum Power Allowed} = \frac{125°C - 105°C}{15.4°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

5.2. Programming Currents

The tables below represent programming, verify and Inrush currents for SmartFusion2 SoC and IGLOO2 FPGA devices.

Table 11 • **Currents During Program Cycle, 0°C < = T_J <= 85°C, Typical Process**

Power Supplies	Voltage (V)	005	010	025	090	Units	Notes
VDD	1.26	46	53	55	42	mA	–
VPP	3.46	8	11	6	12	mA	–
VPPNVM	3.46	1	2	2	3	mA	*
VDDI	2.62	31	16	17	12	mA	–
	3.46	62	31	36	17	mA	–
Number of banks		7	8	8	9	–	–
*Note: * VPP and VPPNVM are internally shorted.*							

Table 12 • **Currents During Verify Cycle, 0°C <= T_J <= 85°C, Typical Process**

Power Supplies	Voltage (V)	005	010	025	090	Units	Notes
VDD	1.26	44	53	55	41	mA	–
VPP	3.46	6	5	3	11	mA	–
VPPNVM	3.46	1	0	0	1	mA	*
VDDI	2.62	31	16	17	11	mA	–
	3.46	61	32	36	17	mA	–
Number of banks		7	8	8	9	–	–
*Note: * VPP and VPPNVM are internally shorted.*							

Table 13 • **Inrush Currents at Power up, -40°C <= T_J <=125°C, Typical Process**

Power Supplies	Voltage (V)	005	010	025	090	Units
VDD	1.26	36	53	78	98	mA
VPP	3.46	35	57	50	36	mA
VDDI	2.62	134	141	161	283	mA
Number of banks		7	8	8	9	–

6. Average Fabric Temperature and Voltage Derating Factors

Table 14 • **Average Temperature and Voltage Derating Factors for Fabric Timing Delays**
(Normalized to T_J = 125°C, Worst-Case VDD = 1.14 V)

Core Voltage VDD (V)	Junction Temperature (°C)							
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.14	0.91	0.91	0.93	0.94	0.96	0.97	0.98	1.00
1.2	0.82	0.83	0.84	0.85	0.87	0.87	0.88	0.90
1.26	0.75	0.75	0.77	0.77	0.79	0.80	0.81	0.75

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • **LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)**

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
*Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.*							

Table 22 • **LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)**

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • **LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)**

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	**Parameters**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

Table 61 • **DDR1/SSTL2 AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	450	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17pF load	–	–	480	Mbps
SSTL2 AC Differential Voltage Specifications						
VDIFF	AC Input Differential Voltage		0.7	–	–	V
Vx	AC Differential Cross Point Voltage		0.5 × VDDI - 0.2	–	0.5 × VDDI + 0.2	V
SSTL2 Impedance Specifications						
	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
SSTL2 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.25	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • **DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t_{PY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.425 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 72 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions						
VDDI	Supply voltage	1.71	1.8	1.89	V	–
VTT	Termination voltage	0.838	0.900	0.964	V	–
VREF	Input reference voltage	0.838	0.900	0.964	V	–
LPDDR DC Input Voltage Specification						
VIH (DC)	DC input logic High	0.7 × VDDI	–	1.89	V	–
VIL (DC)	DC input logic Low	–0.3	–	0.3 × VDDI	V	–
IIH (DC)	Input current High	–	–	10	µA	–
IIL (DC)	Input current Low	–	–	10	µA	–
LPDDR DC Output Voltage Specification						
LPDDR Reduced Drive						
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–
IOL at VOL	Output minimum sink current	–0.1	–	–	mA	–
LPDDR Full Drive						*
VOH	DC output logic High	0.9 × VDDI	–	–	V	–
VOL	DC output logic Low	–	–	0.1 × VDDI	V	–
IOH at VOH	Output minimum source DC current	0.1	–	–	mA	–

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 85 • **LVDS25 Receiver Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 86 • **LVDS25 Transmitter Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • **LVDS33 Receiver Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

	On Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 88 • **LVDS33 Transmitter Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • **B-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	µA
IIL (DC)	Input current Low		–	–	10	µA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • **B-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.2.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 91 • **B-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
Bus-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 92 • **B-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
Bus-LVDS (for MSIO I/O Bank)	2.78	2.632	2.617	2.448	2.436	ns

8.8.3 M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.3.1 Minimum and Maximum Input and Output Levels

Table 93 • **M-LVDS DC Voltage Specification**

Symbols	Parameters	Conditions	Min	Typ	Max	Units	Notes
M-LVDS Recommended DC Operating Conditions							–
VDDI	Supply voltage		2.375	2.5	2.625	V	*
M-LVDS DC Input Voltage Specification							–
VI	DC input voltage		0	–	2.925	V	–
IIH (DC)	Input current High		–	–	10	µA	–
IIL (DC)	Input current Low		–	–	10	µA	–
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)							–
VOH	DC output logic High		1.25	1.425	1.6	V	–
VOL	DC output logic Low		0.9	1.075	1.25	V	–
M-LVDS Differential Voltage Specification							–
VOD	Differential output voltage Swing (for MSIO I/O Bank only)		300	–	650	mV	–
VOCM	Output common mode voltage (for MSIO I/O Bank only)		0.3	–	2.1	V	–
VICM	Input common mode voltage		0.3	–	1.2	V	–
VID	Input differential voltage		50	–	2400	mV	–
*Note: *Only M-LVDS TYPE I is supported*							

Table 94 • **M-LVDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 95 • **M-LVDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 96 • **M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

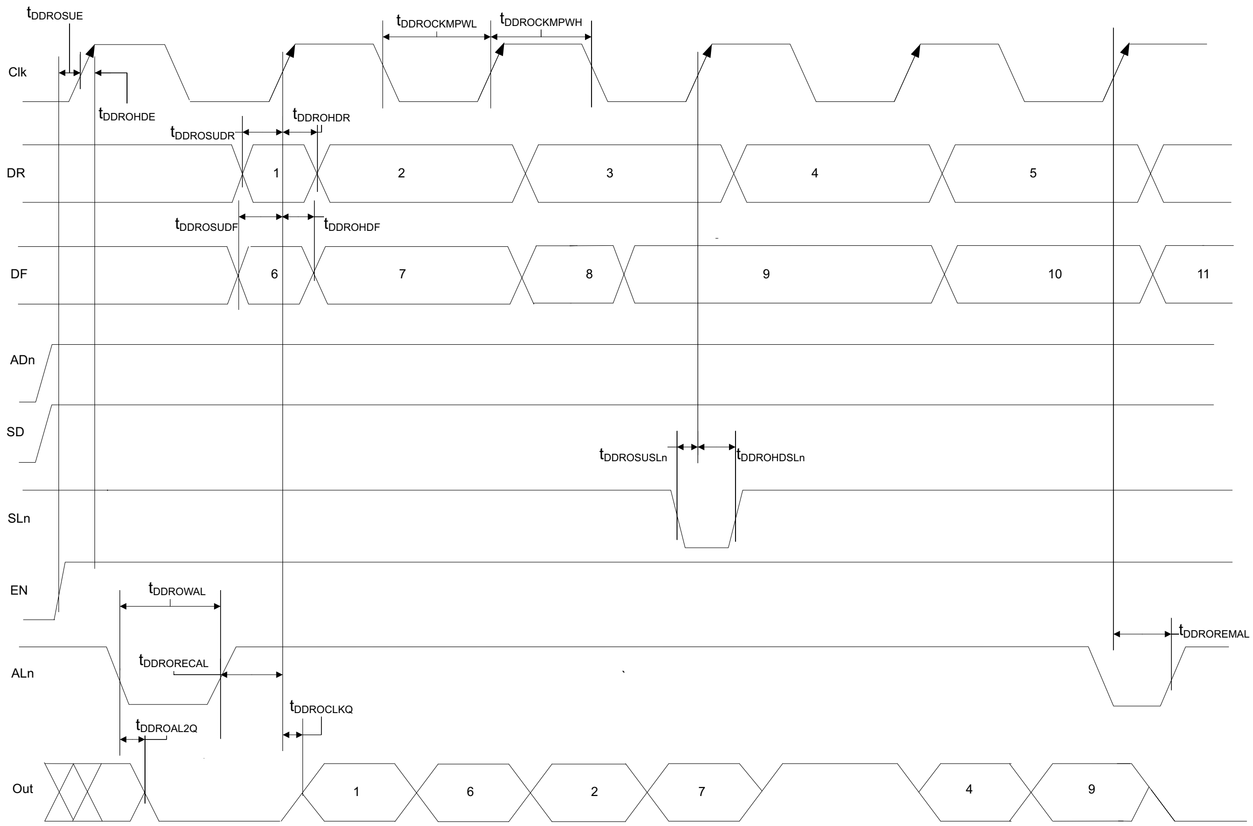

Figure 12 • **Output DDR Timing Diagram**

8.10.5 Timing Characteristics

Table 111 • Output DDR Propagation Delays
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)	Speed Grade –1	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E,G	0.272	ns
$t_{DDROSUDF}$	DF Data Setup for Output DDR	F,E	0.148	ns
$t_{DDROSUDR}$	DR Data Setup for Output DDR	A,E	0.196	ns
$t_{DDROHDF}$	DF Data Hold for Output DDR	F,E	0	ns
$t_{DDROHDR}$	DR Data Hold for Output DDR	A,E	0	ns
$t_{DDROSUE}$	Enable Setup for Output DDR	B,E	0.433	ns
t_{DDROHE}	Enable Hold for Output DDR	B,E	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Output DDR	D,E	0.203	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Output DDR	D,E	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C,G	0.545	ns
$t_{DDROREMAL}$	Asynchronous Load Removal time for Output DDR	C,E	0	ns
$t_{DDRORECAL}$	Asynchronous Load Recovery time for Output DDR	C,E	0.035	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.266	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E,E	0.065	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.139	ns

Table 119 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.428	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		
		Min	Max	Units
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register		0.334	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.56	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.345	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.532	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns

Table 120 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.473	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.631	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.34	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns

Table 130 • uSRAM (RAM1024x1) in 1024x1 Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1 Min	Speed Grade –1 Max	Units
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.274	ns
	Read Access Time without Pipeline Register	–	1.839	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.041	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.623	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.236	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.003	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
Fmax	Maximum Frequency	–	250	MHz

Table 134 • **Electrical Characteristics of the Crystal Oscillator – Medium Gain Mode (2 MHz)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	2	–	MHz
ACCXTAL	Accuracy	–	–	0.003	%
CYCXTAL	Output duty cycle	–	49–51	47–53	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	1	5	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	1	5	ns
IDYNXTAL	Operating current	–	0.3	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	4.5	ms

Table 135 • **Electrical Characteristics of the Crystal Oscillator – Low Gain Mode (32 kHz)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	32	–	kHz
ACCXTAL	Accuracy	–	–	0.006	%
CYCXTAL	Output duty cycle	–	49–51	45.5–54.5	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	150	300	ns
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	150	300	ns
IDYNXTAL	Operating current	–	0.044	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	120	ms

***Table 139* • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Conditions/Package Combinations	Units	Notes
100 MHz to 400 MHz	150	ps	–
*Note: *SSO Data is based on LVCMOS 2.5 V MSIO and/or MSIOD Bank I/Os.*			

16. JTAG

***Table 140* • JTAG 1532**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	-1 Speed Grade				Units
		005	010	025	090	
t_{TCK2Q}	Clock to Q (data out)	7.71	7.91	7.95	9.21	ns
t_{RSTB2Q}	Reset to Q (data out)	7.91	6.54	6.27	7.94	ns
t_{DISU}	Test Data Input Setup Time	-1.07	-0.70	-0.70	-1.33	ns
t_{DIHD}	Test Data Input Hold Time	2.43	2.38	2.47	2.71	ns
t_{TMSSU}	Test Mode Select Setup Time	-0.75	-0.86	-1.13	-1.03	ns
t_{TMDHD}	Test Mode Select Hold Time	1.41	1.48	1.98	1.69	ns
$t_{TRSTREM}$	ResetB Removal Time	-0.81	-1.1	-1.38	-0.8	ns
$t_{TRSTREC}$	ResetB Recovery Time	-0.81	-1.1	-1.38	-0.8	ns
FTCKMAX	TCK Maximum frequency	25	25	25	25	MHz

17. DEVRST_N Characteristics

***Table 141* • DEVRST_N Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	All Devices/Speed Grades			Units	Notes
		Min	Typ	Max		
TRAMPDEVRSTN	DEVRST_N ramp rate	–	–	10	ns	*
*Note: * Slower ramp rates are susceptible to board level noise.*						

19. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 144 • **Mathblocks With All Registers Used**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With All Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
t_{MISU}	Input, Control Register Setup time	0.149	–	ns
t_{MIHD}	Input, Control Register Hold time	0.08	–	ns
$t_{MOCDINSU}$	CDIN Input Setup time	1.68	–	ns
$t_{MOCDINHD}$	CDIN Input Hold time	-0.419	–	ns
$t_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.011	–	ns
$t_{MARSTREM}$	Asynchronous Reset Removal time	0	–	ns
$t_{MARSTREC}$	Asynchronous Reset Recovery time	0.088	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.245	–	ns

Table 145 • **Mathblock With Input Bypassed and Output Registers Used**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Bypassed and Output Registers Used		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
t_{MOSU}	Output Register Setup time	2.294	–	ns
t_{MOHD}	Output Register Hold time	-0.444	–	ns
$t_{MOCDINSU}$	CDIN Input Setup time	1.68	–	ns
$t_{MOCDINHD}$	CDIN Input Hold time	-0.419	–	ns
$t_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	0.115	–	ns
$t_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	0.011	–	ns
$t_{MARSTREM}$	Asynchronous Reset Removal time	0	–	ns
$t_{MARSTREC}$	Asynchronous Reset Recovery time	0.014	–	ns
t_{MOCQ}	Output Register Clock to Out delay	–	0.232	ns
t_{MCLKMP}	CLK Minimum period	2.179	–	ns

Table 146 • Mathblock With Input Register Used and Output in Bypass Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
t_{MISU}	Input Register Setup time	0.149	–	ns
t_{MIHD}	Input Register Hold time	0.08	–	ns
$t_{MSRSTENSU}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{MSRSTENHD}$	Synchronous Reset/Enable Hold time	-0.012	–	ns
$t_{MARSTREM}$	Asynchronous Reset Removal time	-0.005	–	ns
$t_{MARSTREC}$	Asynchronous Reset Recovery time	0.088	–	ns
t_{MICQ}	Input Register Clock to Output delay	–	2.52	ns
$t_{MCDIN2Q}$	CDIN to Output delay	–	1.951	ns

Table 147 • Mathblock With Input and Output in Bypass Mode
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Mathblock With Input and Output in Bypass Mode		Speed Grade –1		
Parameter	**Description**	**Min**	**Max**	**Units**
t_{MIQ}	Input to Output delay	–	2.568	ns
$t_{MCDIN2Q}$	CDIN to Output delay	–	1.951	ns

***Table 159* • SPI Characteristics (continued)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp3	**SPI_[0|1]_CLK minimum pulse width low**					
	SPI_[0|1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	0.385	–	–	µs	–
sp4	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS rise time (10%-90%)	–	2.77	–	ns	1
sp5	SPI_[0|1]_CLK, SPI_[0|1]_DO, SPI_[0|1]_SS fall time (10%-90%)	–	2.906	–	ns	1
SPI Master Configuration						
sp6m	SPI_[0|1]_DO setup time	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0|1]_DO hold time	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0|1]_DI setup time	8	–	–	ns	2
sp9m	SPI_[0|1]_DI hold time	2.5	–	–	ns	2
SPI Slave Configuration						
sp6s	SPI_[0|1]_DO setup time	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0|1]_DO hold time	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0|1]_DI setup time	2	–	–	ns	2
sp9s	SPI_[0|1]_DI hold time	3	–	–	ns	2

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*