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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

|                         |                                                                                                                                                                         |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status          | Active                                                                                                                                                                  |
| Architecture            | MCU, FPGA                                                                                                                                                               |
| Core Processor          | ARM® Cortex® -M3                                                                                                                                                        |
| Flash Size              | 256KB                                                                                                                                                                   |
| RAM Size                | 64KB                                                                                                                                                                    |
| Peripherals             | DDR, PCIe, SERDES                                                                                                                                                       |
| Connectivity            | CANbus, Ethernet, I <sup>2</sup> C, SPI, UART/USART, USB                                                                                                                |
| Speed                   | 166MHz                                                                                                                                                                  |
| Primary Attributes      | FPGA - 25K Logic Modules                                                                                                                                                |
| Operating Temperature   | -40°C ~ 125°C (TJ)                                                                                                                                                      |
| Package / Case          | 484-BGA                                                                                                                                                                 |
| Supplier Device Package | 484-FPBGA (23x23)                                                                                                                                                       |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/microchip-technology/m2s025ts-1fgg484t2">https://www.e-xfl.com/product-detail/microchip-technology/m2s025ts-1fgg484t2</a> |

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**Table 7 • Package Thermal Resistance**

| Product M2GL/M2S | $\theta_{JA}$ |         |         | $\theta_{JB}$ | $\theta_{JC}$ | Units |
|------------------|---------------|---------|---------|---------------|---------------|-------|
|                  | Still Air     | 1.0 m/s | 2.5 m/s |               |               |       |
| 005              |               |         |         |               |               |       |
| FGG484           | 19.36         | 15.81   | 14.63   | 9.74          | 5.27          | °C/W  |
| VFG256           | 41.30         | 38.16   | 35.30   | 28.41         | 3.94          | °C/W  |
| VFG400           | 20.19         | 16.94   | 15.41   | 8.86          | 4.95          | °C/W  |
| 010              |               |         |         |               |               |       |
| FGG484           | 18.22         | 14.83   | 13.62   | 8.83          | 4.92          | °C/W  |
| VFG256           | 37.36         | 34.26   | 31.45   | 24.84         | 7.89          | °C/W  |
| VFG400           | 19.40         | 15.75   | 14.22   | 8.11          | 4.22          | °C/W  |
| 025              |               |         |         |               |               |       |
| FGG484           | 17.03         | 13.66   | 12.45   | 7.66          | 4.18          | °C/W  |
| VFG256           | 33.85         | 30.59   | 27.85   | 21.63         | 6.13          | °C/W  |
| VFG400           | 18.36         | 14.89   | 13.36   | 7.12          | 3.41          | °C/W  |
| 060              |               |         |         |               |               |       |
| FGG484           | 15.40         | 12.06   | 10.85   | 6.14          | 3.15          | °C/W  |
| VFG400           | 17.45         | 14.01   | 12.47   | 6.22          | 2.69          | °C/W  |
| FGG676           | 15.49         | 12.21   | 11.06   | 7.07          | 3.87          | °C/W  |
| 090              |               |         |         |               |               |       |
| FGG484           | 14.64         | 11.37   | 10.16   | 5.43          | 2.77          | °C/W  |
| FGG676           | 14.52         | 11.19   | 10.37   | 6.17          | 3.24          | °C/W  |

### 4.3.2 Theta-JA

Junction-to-ambient thermal resistance ( $\theta_{JA}$ ) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 125°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL060TS-1FGG484 package at Automotive Grade 2 temperature and in still air, where:

$$\begin{aligned}\theta_{JA} &= 15.4^{\circ}\text{C/W (taken from Table 7 on page 6).} \\ T_A &= 105^{\circ}\text{C}\end{aligned}$$

$$\text{Maximum Power Allowed} = \frac{125^{\circ}\text{C} - 105^{\circ}\text{C}}{15.4^{\circ}\text{C/W}} = 1.3 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

**Table 30 • LVCMOS 2.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection |                   |                                                         | VOH (V)<br>Min | VOL (V)<br>Max | IOH (at VOH)<br>mA | IOL (at VOL)<br>mA |
|------------------------|-------------------|---------------------------------------------------------|----------------|----------------|--------------------|--------------------|
| MSIO<br>I/O Bank       | MSIOD<br>I/O Bank | DDRIO I/O Bank<br>(With Software Default<br>Fixed Code) |                |                |                    |                    |
| 2 mA                   | 2 mA              | 2 mA                                                    | 1.7            | 0.7            | 2                  | 2                  |
| 4 mA                   | 4 mA              | 4 mA                                                    | 1.7            | 0.7            | 4                  | 4                  |
| 6 mA                   | 6 mA              | 6 mA                                                    | 1.7            | 0.7            | 6                  | 6                  |
| 8 mA                   | 8 mA              | 8 mA                                                    | 1.7            | 0.7            | 8                  | 8                  |
| 12 mA                  | 12 mA             | 12 mA                                                   | 1.7            | 0.7            | 12                 | 12                 |
| 16 mA                  | N/A               | 16 mA                                                   | 1.7            | 0.7            | 16                 | 16                 |

*Note:* For board design considerations, output slew rates extraction, detailed output buffer resistances and I/V Curve use the corresponding IBIS models located at:  
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.

### 8.6.3.2 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 31 • LVCMOS 2.5 V AC Switching Characteristics for Receiver (Input Buffers)**

Worst-case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

|                                   | On-Die Termination<br>(ODT) in $\Omega$ | Speed Grade<br>-1 |           | Units |
|-----------------------------------|-----------------------------------------|-------------------|-----------|-------|
|                                   |                                         | $t_{PY}$          | $t_{PYS}$ |       |
| LVCMOS 2.5 V (for DDRIO I/O Bank) | None                                    | 1.903             | 2.021     | ns    |
| LVCMOS 2.5 V (for MSIO I/O Bank)  | None                                    | 2.689             | 2.698     | ns    |
| LVCMOS 2.5 V (for MSIOD I/O Bank) | None                                    | 2.447             | 2.46      | ns    |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 32 • LVCMOS 2.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**

Worst-case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

| Output Drive Selection                            | Slew Control | Speed Grade<br>-1 |                 |                 |                 |                 | Units |
|---------------------------------------------------|--------------|-------------------|-----------------|-----------------|-----------------|-----------------|-------|
|                                                   |              | t <sub>DP</sub>   | t <sub>ZL</sub> | t <sub>ZH</sub> | t <sub>HZ</sub> | t <sub>LZ</sub> |       |
| LVCMOS 2.5 V (for DDRIO I/O Bank with Fixed Code) |              |                   |                 |                 |                 |                 |       |
| 2 mA                                              | slow         | 3.967             | 3.664           | 3.986           | 4.172           | 3.811           | ns    |
|                                                   | medium       | 3.625             | 3.38            | 3.647           | 3.882           | 3.458           | ns    |
|                                                   | medium_fast  | 3.485             | 3.259           | 3.507           | 3.747           | 3.327           | ns    |
|                                                   | fast         | 3.458             | 3.253           | 3.48            | 3.74            | 3.31            | ns    |
| 4 mA                                              | slow         | 3.371             | 2.942           | 3.362           | 5.148           | 4.71            | ns    |
|                                                   | medium       | 3.063             | 2.701           | 3.059           | 4.874           | 4.381           | ns    |
|                                                   | medium_fast  | 2.925             | 2.566           | 2.92            | 4.686           | 4.248           | ns    |
|                                                   | fast         | 2.91              | 2.559           | 2.905           | 4.683           | 4.238           | ns    |

**Table 41 • LVCMOS 1.5 V Maximum AC Switching Speeds**

| Symbols                                        | Parameters                             | Conditions                                 | Min | Typ | Max | Units |
|------------------------------------------------|----------------------------------------|--------------------------------------------|-----|-----|-----|-------|
| <b>LVCMOS 1.5 V Maximum AC Switching Speed</b> |                                        |                                            |     |     |     |       |
| Dmax                                           | Maximum data rate (for DDRIO I/O Bank) | AC loading: 17 pF load, maximum drive/slew | –   | –   | 210 | Mbps  |
| Dmax                                           | Maximum data rate (for MSIO I/O Bank)  | AC loading: 17 pF load, maximum drive/slew | –   | –   | 140 | Mbps  |
| Dmax                                           | Maximum data rate (for MSIOD I/O Bank) | AC loading: 17 pF load, maximum drive/slew | –   | –   | 190 | Mbps  |

**Table 42 • LVCMOS 1.5 V AC Test Parameters and Driver Impedance Specifications**

| Symbols                                               | Parameters                                                                       | Min | Typ            | Max | Units    |
|-------------------------------------------------------|----------------------------------------------------------------------------------|-----|----------------|-----|----------|
| <b>LVCMOS 1.5 V AC Calibrated Impedance Option</b>    |                                                                                  |     |                |     |          |
| Rodt_cal                                              | Supported output driver calibrated impedance (for DDRIO I/O Bank)                | –   | 75, 60, 50, 40 | –   | $\Omega$ |
| <b>LVCMOS 1.5 V AC Test Parameters Specifications</b> |                                                                                  |     |                |     |          |
| Vtrip                                                 | Measuring/trip point for data path                                               | –   | 0.75           | –   | V        |
| Rent                                                  | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         | –   | 2k             | –   | $\Omega$ |
| Cent                                                  | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) | –   | 5              | –   | pF       |
| Cload                                                 | Capacitive loading for data path ( $t_{DP}$ )                                    | –   | 5              | –   | pF       |

**Table 43 • LVCMOS 1.5 V Transmitter Drive Strength Specifications**

| Output Drive Selection |                |                                  | VOH (V)            | VOL (V)            | IOH (at VOH) mA | IOL (at VOL) mA |
|------------------------|----------------|----------------------------------|--------------------|--------------------|-----------------|-----------------|
| MSIO I/O Bank          | MSIOD I/O Bank | DDRIO I/O Bank (with Fixed Code) | Min                | Max                |                 |                 |
| 2 mA                   | 2 mA           | 2 mA                             | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 2               | 2               |
| 4 mA                   | 4 mA           | 4 mA                             | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 4               | 4               |
| 6 mA                   | 6 mA           | 6 mA                             | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 6               | 6               |
| 8 mA                   | N/A            | 8 mA                             | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 8               | 8               |
| N/A                    | N/A            | 10 mA                            | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 10              | 10              |
| N/A                    | N/A            | 12 mA                            | $VDDI \times 0.75$ | $VDDI \times 0.25$ | 12              | 12              |

**Table 53 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)**

| Symbols                                            | Parameters                                                                       | Conditions                           | Min | Typ                 | Max | Units    |
|----------------------------------------------------|----------------------------------------------------------------------------------|--------------------------------------|-----|---------------------|-----|----------|
| <b>PCI/PCI-X AC Specifications</b>                 |                                                                                  |                                      |     |                     |     |          |
| Dmax                                               | Maximum data rate (MSIO I/O Bank)                                                | AC Loading: per JEDEC specifications | –   | –                   | 560 | Mbps     |
| <b>PCI/PCI-X AC Test Parameters Specifications</b> |                                                                                  |                                      |     |                     |     |          |
| Vtrip                                              | Measuring/trip point for data path (falling edge)                                |                                      | –   | $0.615 \times VDDI$ | –   | V        |
| Vtrip                                              | Measuring/trip point for data path (rising edge)                                 |                                      | –   | $0.285 \times VDDI$ | –   | V        |
| Rtt_test                                           | Resistance for data test path                                                    |                                      | –   | 25                  | –   | $\Omega$ |
| Rent                                               | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         |                                      | –   | 2k                  | –   | $\Omega$ |
| Cent                                               | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) |                                      | –   | 5                   | –   | pF       |
| Cload                                              | Capacitive loading for data path ( $t_{DP}$ )                                    |                                      | –   | 10                  | –   | pF       |

### 8.6.7.2 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 54 • PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)**

Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^\circ\text{C}$ ,  $VDD = 1.14\text{ V}$ ,  $VDDI = 3.15\text{ V}$

|                                 | ODT<br>(On Die Termination)<br>in $\Omega$ | Speed Grade<br>–1 |           | Units |
|---------------------------------|--------------------------------------------|-------------------|-----------|-------|
|                                 |                                            | $t_{PY}$          | $t_{PYS}$ |       |
| PCI/PCIX<br>(for MSIO I/O Bank) | None                                       | 2.379             | 2.387     | ns    |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 55 • PCI/PCIX AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**

Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^\circ\text{C}$ ,  $VDD = 1.14\text{ V}$ ,  $VDDI = 3.15\text{ V}$

|                              | Speed Grade<br>–1 |          |          |          |          | Units |
|------------------------------|-------------------|----------|----------|----------|----------|-------|
|                              | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| PCI/PCIX (for MSIO I/O Bank) | 2.394             | 2.274    | 2.316    | 6.876    | 6.242    | ns    |

## 8.7. Memory Interface and Voltage Referenced I/O Standards

### 8.7.1 High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 FPGA and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

#### 8.7.1.1 Minimum and Maximum Input and Output Levels Specification

**Table 56 • HSTL DC Voltage Specification (Applicable to DDRIO I/O Bank Only)**

| Symbols                                            | Parameters                       | Conditions | Min   | Typ   | Max        | Units |
|----------------------------------------------------|----------------------------------|------------|-------|-------|------------|-------|
| <b>HSTL Recommended DC Operating Conditions</b>    |                                  |            |       |       |            |       |
| VDDI                                               | Supply voltage                   |            | 1.425 | 1.5   | 1.575      | V     |
| VTT                                                | Termination voltage              |            | 0.698 | 0.750 | 0.803      | V     |
| VREF                                               | Input reference voltage          |            | 0.698 | 0.750 | 0.803      | V     |
| <b>HSTL DC Input Voltage Specification</b>         |                                  |            |       |       |            |       |
| VIH (DC)                                           | DC input logic High              | VREF + 0.1 | –     | –     | 1.575      | V     |
| VIL (DC)                                           | DC input logic Low               | –0.3       | –     | –     | VREF – 0.1 | V     |
| IIH (DC)                                           | Input current High               | –          | –     | –     | 10         | μA    |
| IIL (DC)                                           | Input current Low                | –          | –     | –     | 10         | μA    |
| <b>HSTL DC Output Voltage Specification</b>        |                                  |            |       |       |            |       |
| <b>HSTL Class I</b>                                |                                  |            |       |       |            |       |
| VOH                                                | DC output logic High             | VDDI – 0.4 | –     | –     | –          | V     |
| VOL                                                | DC output logic Low              | –          | –     | –     | 0.4        | V     |
| IOH at VOH                                         | Output minimum source DC current | –7.0       | –     | –     | –          | mA    |
| IOL at VOL                                         | Output minimum sink current      | 7.0        | –     | –     | –          | mA    |
| <b>HSTL Class II</b>                               |                                  |            |       |       |            |       |
| VOH                                                | DC output logic High             | VDDI – 0.4 | –     | –     | –          | V     |
| VOL                                                | DC output logic Low              | –          | –     | –     | 0.4        | V     |
| IOH at VOH                                         | Output minimum source DC current | –15.0      | –     | –     | –          | mA    |
| IOL at VOL                                         | Output minimum sink current      | 15.0       | –     | –     | –          | mA    |
| <b>HSTL DC Differential Voltage Specifications</b> |                                  |            |       |       |            |       |
| VID (DC)                                           | DC input differential voltage    | 0.2        | –     | –     | –          | V     |

### 8.7.4 Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

#### 8.7.4.1 Minimum and Maximum Input and Output Levels Specification

**Table 64 • DDR2/SSTL18 AC/DC Minimum and Maximum Input and Output Levels Specification**

| Symbols                                                                             | Parameters                                             | Min          | Typ   | Max          | Units | Notes |
|-------------------------------------------------------------------------------------|--------------------------------------------------------|--------------|-------|--------------|-------|-------|
| <b>Recommended DC Operating Conditions</b>                                          |                                                        |              |       |              |       |       |
| VDDI                                                                                | Supply voltage                                         | 1.71         | 1.8   | 1.89         | V     | –     |
| VTT                                                                                 | Termination voltage                                    | 0.838        | 0.900 | 0.964        | V     | –     |
| VREF                                                                                | Input reference voltage                                | 0.838        | 0.900 | 0.964        | V     | –     |
| <b>SSTL18 DC Input Voltage Specification</b>                                        |                                                        |              |       |              |       |       |
| VIH (DC)                                                                            | DC input logic High                                    | VREF + 0.125 | –     | 1.89         | V     | –     |
| VIL (DC)                                                                            | DC input logic Low                                     | –0.3         | –     | VREF – 0.125 | V     | –     |
| IIH (DC)                                                                            | Input current High                                     | –            | –     | 10           | μA    | –     |
| IIL (DC)                                                                            | Input current Low                                      | –            | –     | 10           | μA    | –     |
| <b>SSTL18 DC Output Voltage Specification</b>                                       |                                                        |              |       |              |       |       |
| <b>SSTL18 Class I (DDR2 Reduced Drive)</b>                                          |                                                        |              |       |              |       |       |
| VOH                                                                                 | DC output logic High                                   | VTT + 0.603  | –     | –            | V     | –     |
| VOL                                                                                 | DC output logic Low                                    | –            | –     | VTT – 0.603  | V     | –     |
| IOH at VOH                                                                          | Output minimum source DC current (DDRIO I/O Bank only) | 6.0          | –     | –            | mA    | –     |
| IOL at VOL                                                                          | Output minimum sink current (DDRIO I/O Bank only)      | –6.0         | –     | –            | mA    | –     |
| <b>SSTL18 Class II (DDR2 Full Drive)</b>                                            |                                                        |              |       |              |       | *     |
| VOH                                                                                 | DC output logic High                                   | VTT + 0.603  | –     | –            | V     | –     |
| VOL                                                                                 | DC output logic Low                                    | –            | –     | VTT – 0.603  | V     | –     |
| IOH at VOH                                                                          | Output minimum source DC current (DDRIO I/O Bank only) | 12.0         | –     | –            | mA    | –     |
| IOL at VOL                                                                          | Output minimum sink current (DDRIO I/O Bank only)      | –12.0        | –     | –            | mA    | –     |
| <b>SSTL18 DC Differential Voltage Specification</b>                                 |                                                        |              |       |              |       |       |
| VID (DC)                                                                            | DC input differential voltage                          | 0.3          | –     | –            | V     | –     |
| <i>Note: *To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.</i> |                                                        |              |       |              |       |       |

**Table 94 • M-LVDS AC Specifications**

| Symbols                                         | Parameters                                                                       | Conditions                                        | Min | Typ         | Max | Units    |
|-------------------------------------------------|----------------------------------------------------------------------------------|---------------------------------------------------|-----|-------------|-----|----------|
| <b>M-LVDS Maximum AC Switching Speeds</b>       |                                                                                  |                                                   |     |             |     |          |
| Dmax                                            | Maximum data rate (for MSIO I/O Bank)                                            | AC loading: 2 pF / 100 $\Omega$ differential load | –   | –           | 450 | Mbps     |
| <b>M-LVDS Impedance Specification</b>           |                                                                                  |                                                   |     |             |     |          |
| Rt                                              | Termination resistance                                                           | –                                                 | –   | 50          | –   | $\Omega$ |
| <b>M-LVDS AC Test Parameters Specifications</b> |                                                                                  |                                                   |     |             |     |          |
| VTrip                                           | Measuring/trip point for data path                                               |                                                   | –   | Cross point | –   | V        |
| Rent                                            | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         |                                                   | –   | 2k          | –   | $\Omega$ |
| Cent                                            | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) |                                                   | –   | 5           | –   | pF       |

### 8.8.3.2 AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 95 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)**

Worst-case Automotive Grade 2 conditions:  $T_j = 125^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

|                             | On-Die Termination (ODT) in $\Omega$ | Speed Grade –1 | Units |
|-----------------------------|--------------------------------------|----------------|-------|
|                             |                                      | $t_{PY}$       |       |
| M-LVDS (for MSIO I/O Bank)  | None                                 | 3.011          | ns    |
|                             | 100                                  | 3.006          | ns    |
| M-LVDS (for MSIOD I/O Bank) | None                                 | 2.722          | ns    |
|                             | 100                                  | 2.725          | ns    |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 96 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**

Worst-case Automotive Grade 2 conditions:  $T_j = 125^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

|                            | Speed Grade –1 |          |          |          |          | Units |
|----------------------------|----------------|----------|----------|----------|----------|-------|
|                            | $t_{DP}$       | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| M-LVDS (for MSIO I/O Bank) | 2.78           | 2.632    | 2.616    | 2.447    | 2.436    | ns    |

### 8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

#### 8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

**Table 97 • Mini-LVDS DC Voltage Specification**

| Symbols                                             | Parameters                        | Conditions | Min   | Typ   | Max   | Units |
|-----------------------------------------------------|-----------------------------------|------------|-------|-------|-------|-------|
| <b>Recommended DC Operating Conditions</b>          |                                   |            |       |       |       |       |
| VDDI                                                | Supply voltage                    |            | 2.375 | 2.5   | 2.625 | V     |
| <b>Mini-LVDS DC Input Voltage Specification</b>     |                                   |            |       |       |       |       |
| VI                                                  | DC Input voltage                  |            | 0     | –     | 2.925 | V     |
| <b>Mini-LVDS DC Output Voltage Specification</b>    |                                   |            |       |       |       |       |
| VOH                                                 | DC output logic High              |            | 1.25  | 1.425 | 1.6   | V     |
| VOL                                                 | DC output logic Low               |            | 0.9   | 1.075 | 1.25  | V     |
| <b>Mini-LVDS Differential Voltage Specification</b> |                                   |            |       |       |       |       |
| VOD                                                 | Differential output voltage swing |            | 300   | –     | 600   | mV    |
| VOCM                                                | Output common mode voltage        |            | 1     | –     | 1.4   | V     |
| VICM                                                | Input common mode voltage         |            | 0.3   | –     | 1.2   | V     |
| VID                                                 | Input differential voltage        |            | 100   | –     | 600   | mV    |

**Table 98 • Mini-LVDS AC Specifications**

| Symbols                                            | Parameters                                                                       | Conditions                                         | Min | Typ         | Max | Units    |
|----------------------------------------------------|----------------------------------------------------------------------------------|----------------------------------------------------|-----|-------------|-----|----------|
| <b>Mini-LVDS Maximum AC Switching Speed</b>        |                                                                                  |                                                    |     |             |     |          |
| Dmax                                               | Maximum data rate (MSIO I/O Bank)                                                | AC loading: 2 pF / 100 $\Omega$ differential load  | –   | –           | 460 | Mbps     |
| Dmax                                               | Maximum data rate (MSIOD I/O Bank)                                               | AC loading: 10 pF / 100 $\Omega$ differential load | –   | –           | 480 | Mbps     |
| <b>Mini-LVDS Impedance Specification</b>           |                                                                                  |                                                    |     |             |     |          |
| Rt                                                 | Termination resistance                                                           |                                                    | –   | 100         | –   | $\Omega$ |
| <b>Mini-LVDS AC Test Parameters Specifications</b> |                                                                                  |                                                    |     |             |     |          |
| VTrip                                              | Measuring/trip point for data path                                               |                                                    | –   | Cross point | –   | V        |
| Rent                                               | Resistance for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ )         |                                                    | –   | 2k          | –   | $\Omega$ |
| Cent                                               | Capacitive loading for enable path ( $t_{ZH}$ , $t_{ZL}$ , $t_{HZ}$ , $t_{LZ}$ ) |                                                    | –   | 5           | –   | pF       |

### 8.8.4.2. AC Switching Characteristics

#### AC Switching Characteristics for Receiver (Input Buffers)

**Table 99 • Mini-LVDS AC Switching Characteristics for Receiver (Input Buffers)**

Worst-case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

|                                | On-Die Termination (ODT) in $\Omega$ | Speed Grade<br>-1 | Units |
|--------------------------------|--------------------------------------|-------------------|-------|
|                                |                                      | $t_{PY}$          |       |
| Mini-LVDS (for MSIO I/O Bank)  | None                                 | 3.112             | ns    |
|                                | 100                                  | 2.995             | ns    |
| Mini-LVDS (for MSIOD I/O Bank) | None                                 | 2.612             | ns    |
|                                | 100                                  | 2.612             | ns    |

#### AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

**Table 100 • Mini-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**

Worst-case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$ ,  $V_{DDI} = 2.375\text{ V}$

|                                | Speed Grade<br>-1 |          |          |          |          | Units |
|--------------------------------|-------------------|----------|----------|----------|----------|-------|
|                                | $t_{DP}$          | $t_{ZL}$ | $t_{ZH}$ | $t_{HZ}$ | $t_{LZ}$ |       |
| Mini-LVDS (for MSIO I/O Bank)  | 2.3               | 2.602    | 2.59     | 2.306    | 2.32     | ns    |
| Mini-LVDS (for MSIOD I/O Bank) |                   |          |          |          |          |       |
| No pre-emphasis                | 1.652             | 1.84     | 1.833    | 1.988    | 1.965    | ns    |
| Min pre-emphasis               | 1.652             | 1.84     | 1.833    | 1.988    | 1.965    | ns    |
| Med pre-emphasis               | 1.577             | 1.868    | 1.86     | 2.02     | 1.994    | ns    |
| Max pre-emphasis               | 1.555             | 1.894    | 1.883    | 2.048    | 2.019    | ns    |

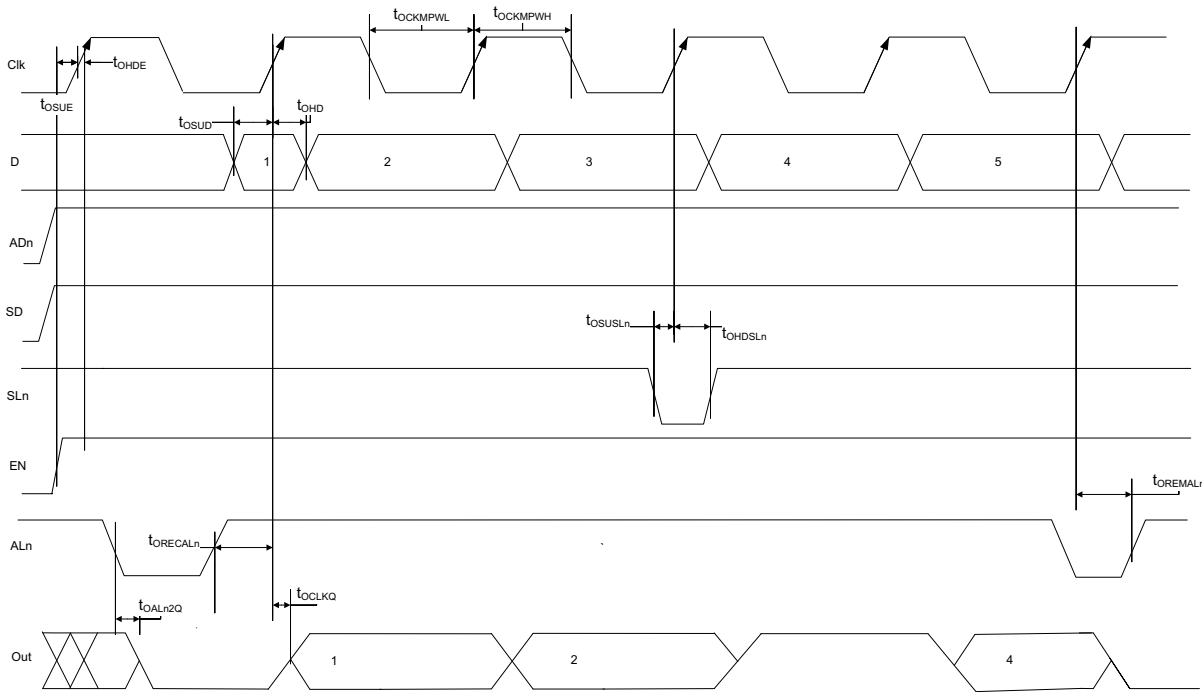
### 8.8.5 RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

#### 8.8.5.1 Minimum and Maximum Input and Output Levels

**Table 101 • RSDS DC Voltage Specification**

| Symbols                                        | Parameters                        | Conditions | Min   | Typ   | Max   | Units |
|------------------------------------------------|-----------------------------------|------------|-------|-------|-------|-------|
| <b>Recommended DC Operating Conditions</b>     |                                   |            |       |       |       |       |
| $V_{DDI}$                                      | Supply voltage                    |            | 2.375 | 2.5   | 2.625 | V     |
| <b>RSDS DC Input Voltage Specification</b>     |                                   |            |       |       |       |       |
| $V_I$                                          | DC input voltage                  |            | 0     | –     | 2.925 | V     |
| <b>RSDS DC Output Voltage Specification</b>    |                                   |            |       |       |       |       |
| $V_{OH}$                                       | DC output logic High              |            | 1.25  | 1.425 | 1.6   | V     |
| $V_{OL}$                                       | DC output logic Low               |            | 0.9   | 1.075 | 1.25  | V     |
| <b>RSDS Differential Voltage Specification</b> |                                   |            |       |       |       |       |
| $V_{OD}$                                       | Differential output voltage swing |            | 100   | –     | 600   | mV    |
| $V_{OCM}$                                      | Output common mode voltage        |            | 0.5   | –     | 1.5   | V     |



**Figure 8 • I/O Register Output Timing Diagram**

**Table 109 • Output/Enable Data Register Propagation Delays**  
Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

| Parameter     | Description                                                        | Measuring Nodes (from, to)* | Speed Grade -1 | Units |
|---------------|--------------------------------------------------------------------|-----------------------------|----------------|-------|
| $t_{OBYP}$    | Bypass Delay of the Output/Enable Register                         | F,G or H,I                  | 0.364          | ns    |
| $t_{OCLKQ}$   | Clock-to-Q of the Output/Enable Register                           | E,G or E,I                  | 0.272          | ns    |
| $t_{OSUD}$    | Data Setup Time for the Output/Enable Register                     | A,E or J,E                  | 0.196          | ns    |
| $t_{OHD}$     | Data Hold Time for the Output/Enable Register                      | A,E or J,E                  | 0              | ns    |
| $t_{OSUE}$    | Enable Setup Time for the Output/Enable Register                   | B,E                         | 0.433          | ns    |
| $t_{OHE}$     | Enable Hold Time for the Output/Enable Register                    | B,E                         | 0              | ns    |
| $t_{OSUSL}$   | Synchronous Load Setup Time for the Output/Enable Register         | D,E                         | 0.203          | ns    |
| $t_{OHSL}$    | Synchronous Load Hold Time for the Output/Enable Register          | D,E                         | 0              | ns    |
| $t_{OALn2Q}$  | Asynchronous Clear-to-Q of the Output/Enable Register ( $ADn=1$ )  | C,G or C,I                  | 0.523          | ns    |
|               | Asynchronous Preset-to-Q of the Output/Enable Register ( $ADn=0$ ) | C,G or C,I                  | 0.545          | ns    |
| $t_{OREMALn}$ | Asynchronous Load Removal Time for the Output/Enable Register      | C,E                         | 0              | ns    |
| $t_{ORECALn}$ | Asynchronous Load Recovery Time for the Output/Enable Register     | C,E                         | 0.035          | ns    |

**Table 126 • uSRAM (RAM128x9) in 128x9 Mode**  
Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$  (continued)

| Parameter             | Description                                                                           | Speed Grade<br>–1 |       | Units |
|-----------------------|---------------------------------------------------------------------------------------|-------------------|-------|-------|
|                       |                                                                                       | Min               | Max   |       |
| $t_{\text{BLKSU}}$    | Read Block Select Setup Time                                                          | 1.898             | –     | ns    |
| $t_{\text{BLKHD}}$    | Read Block Select Hold Time                                                           | -0.671            | –     | ns    |
| $t_{\text{BLK2Q}}$    | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | –                 | 2.14  | ns    |
| $t_{\text{RSTREM}}$   | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.15             | –     | ns    |
|                       | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.047             | –     | ns    |
| $t_{\text{RSTREC}}$   | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.524             | –     | ns    |
|                       | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.244             | –     | ns    |
| $t_{\text{R2Q}}$      | Read Asynchronous Reset to Output Propagation Delay (with Pipe-Line Register Enabled) | –                 | 0.865 | ns    |
| $t_{\text{SRSTSU}}$   | Read Synchronous Reset Setup Time                                                     | 0.279             | –     | ns    |
| $t_{\text{SRSTHD}}$   | Read Synchronous Reset Hold Time                                                      | 0.062             | –     | ns    |
| $t_{\text{CCY}}$      | Write Clock Period                                                                    | 4                 | –     | ns    |
| $t_{\text{CCLKMPWH}}$ | Write Clock Minimum Pulse Width High                                                  | 1.8               | –     | ns    |
| $t_{\text{CCLKMPWL}}$ | Write Clock Minimum Pulse Width Low                                                   | 1.8               | –     | ns    |
| $t_{\text{BLKCSU}}$   | Write Block Setup Time                                                                | 0.417             | –     | ns    |
| $t_{\text{BLKCHD}}$   | Write Block Hold Time                                                                 | 0.007             | –     | ns    |
| $t_{\text{DINCSU}}$   | Write Input Data setup Time                                                           | 0.104             | –     | ns    |
| $t_{\text{DINCHD}}$   | Write Input Data hold Time                                                            | 0.142             | –     | ns    |
| $t_{\text{ADDRCSU}}$  | Write Address Setup Time                                                              | 0.091             | –     | ns    |
| $t_{\text{ADDRCHD}}$  | Write Address Hold Time                                                               | 0.24              | –     | ns    |
| $t_{\text{WECSU}}$    | Write Enable Setup Time                                                               | 0.41              | –     | ns    |
| $t_{\text{WECHD}}$    | Write Enable Hold Time                                                                | -0.027            | –     | ns    |
| $F_{\text{max}}$      | Maximum Frequency                                                                     | –                 | 250   | MHz   |

**Table 128 • uSRAM (RAM256x4) in 256x4 Mode**  
Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$  (continued)

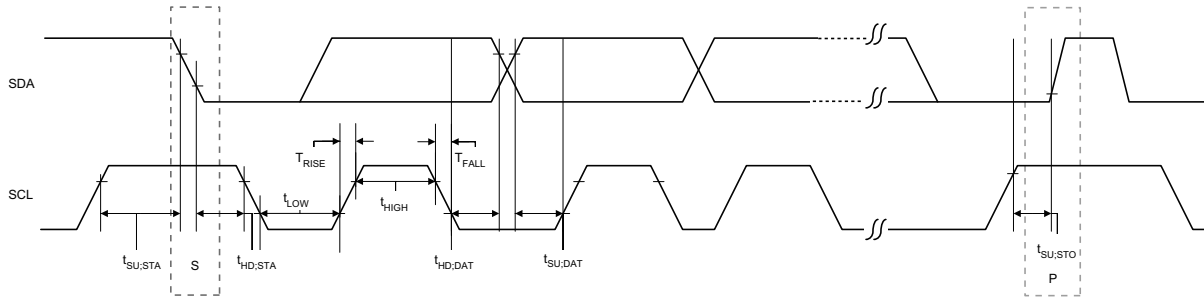
| Parameter      | Description                          | Speed Grade<br>-1 |     | Units |
|----------------|--------------------------------------|-------------------|-----|-------|
|                |                                      | Min               | Max |       |
| $t_{SRSTSU}$   | Read Synchronous Reset Setup Time    | 0.279             | –   | ns    |
| $t_{SRSTHD}$   | Read Synchronous Reset Hold Time     | 0.062             | –   | ns    |
| $t_{CCY}$      | Write Clock Period                   | 4                 | –   | ns    |
| $t_{CCLKMPWH}$ | Write Clock Minimum Pulse Width High | 1.8               | –   | ns    |
| $t_{CCLKMPWL}$ | Write Clock Minimum Pulse Width Low  | 1.8               | –   | ns    |
| $t_{BLKCSU}$   | Write Block Setup Time               | 0.417             | –   | ns    |
| $t_{BLKCHD}$   | Write Block Hold Time                | 0.007             | –   | ns    |
| $t_{DINCSU}$   | Write Input Data setup Time          | 0.104             | –   | ns    |
| $t_{DINCHD}$   | Write Input Data hold Time           | 0.142             | –   | ns    |
| $t_{ADDRCSU}$  | Write Address Setup Time             | 0.091             | –   | ns    |
| $t_{ADDRCHD}$  | Write Address Hold Time              | 0.253             | –   | ns    |
| $t_{WECSU}$    | Write Enable Setup Time              | 0.41              | –   | ns    |
| $t_{WECHD}$    | Write Enable Hold Time               | -0.027            | –   | ns    |
| $F_{max}$      | Maximum Frequency                    | –                 | 250 | MHz   |

**Table 129 • uSRAM (RAM512x2) in 512x2 Mode**  
Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$

| Parameter       | Description                                   | Speed Grade<br>-1 |       | Units |
|-----------------|-----------------------------------------------|-------------------|-------|-------|
|                 |                                               | Min               | Max   |       |
| $t_{CY}$        | Read Clock Period                             | 4                 | –     | ns    |
| $t_{CLKMPWH}$   | Read Clock Minimum Pulse Width High           | 1.8               | –     | ns    |
| $t_{CLKMPWL}$   | Read Clock Minimum pulse Width Low            | 1.8               | –     | ns    |
| $t_{PLCY}$      | Read Pipe-line clock period                   | 4                 | –     | ns    |
| $t_{PLCLKMPWH}$ | Read Pipe-line clock Minimum Pulse Width High | 1.8               | –     | ns    |
| $t_{PLCLKMPWL}$ | Read Pipe-line clock Minimum Pulse Width Low  | 1.8               | –     | ns    |
| $t_{CLK2Q}$     | Read Access Time with Pipeline Register       | –                 | 0.276 | ns    |
|                 | Read Access Time without Pipeline Register    | –                 | 1.824 | ns    |
| $t_{ADDRSU}$    | Read Address Setup Time in Synchronous Mode   | 0.311             | –     | ns    |
|                 | Read Address Setup Time in Asynchronous Mode  | 2.023             | –     | ns    |
| $t_{ADDRHD}$    | Read Address Hold Time in Synchronous Mode    | 0.141             | –     | ns    |
|                 | Read Address Hold Time in Asynchronous Mode   | -0.599            | –     | ns    |
| $t_{RDENSU}$    | Read Enable Setup Time                        | 0.287             | –     | ns    |
| $t_{RDENHD}$    | Read Enable Hold Time                         | 0.059             | –     | ns    |
| $t_{BLKSU}$     | Read Block Select Setup Time                  | 1.898             | –     | ns    |

**Table 130 • uSRAM (RAM1024x1) in 1024x1 Mode**  
Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^{\circ}\text{C}$ ,  $V_{DD} = 1.14\text{ V}$  (continued)

| Parameter             | Description                                                                           | Speed Grade<br>-1 |       | Units |
|-----------------------|---------------------------------------------------------------------------------------|-------------------|-------|-------|
|                       |                                                                                       | Min               | Max   |       |
| $t_{\text{CLK2Q}}$    | Read Access Time with Pipeline Register                                               | –                 | 0.274 | ns    |
|                       | Read Access Time without Pipeline Register                                            | –                 | 1.839 | ns    |
| $t_{\text{ADDRSU}}$   | Read Address Setup Time in Synchronous Mode                                           | 0.311             | –     | ns    |
|                       | Read Address Setup Time in Asynchronous Mode                                          | 2.041             | –     | ns    |
| $t_{\text{ADDRHD}}$   | Read Address Hold Time in Synchronous Mode                                            | 0.141             | –     | ns    |
|                       | Read Address Hold Time in Asynchronous Mode                                           | -0.623            | –     | ns    |
| $t_{\text{RDENSU}}$   | Read Enable Setup Time                                                                | 0.287             | –     | ns    |
| $t_{\text{RDENHD}}$   | Read Enable Hold Time                                                                 | 0.059             | –     | ns    |
| $t_{\text{BLKSU}}$    | Read Block Select Setup Time                                                          | 1.898             | –     | ns    |
| $t_{\text{BLKHD}}$    | Read Block Select Hold Time                                                           | -0.671            | –     | ns    |
| $t_{\text{BLK2Q}}$    | Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)        | –                 | 2.236 | ns    |
| $t_{\text{RSTREM}}$   | Read Asynchronous Reset Removal Time (Pipelined Clock)                                | -0.15             | –     | ns    |
|                       | Read Asynchronous Reset Removal Time (Non-Pipelined Clock)                            | 0.047             | –     | ns    |
| $t_{\text{RSTREC}}$   | Read Asynchronous Reset Recovery Time (Pipelined Clock)                               | 0.524             | –     | ns    |
|                       | Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)                           | 0.244             | –     | ns    |
| $t_{\text{R2Q}}$      | Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled) | –                 | 0.862 | ns    |
| $t_{\text{SRSTSU}}$   | Read Synchronous Reset Setup Time                                                     | 0.279             | –     | ns    |
| $t_{\text{SRSTHD}}$   | Read Synchronous Reset Hold Time                                                      | 0.062             | –     | ns    |
| $t_{\text{CCY}}$      | Write Clock Period                                                                    | 4                 | –     | ns    |
| $t_{\text{CCLKMPWH}}$ | Write Clock Minimum Pulse Width High                                                  | 1.8               | –     | ns    |
| $t_{\text{CCLKMPWL}}$ | Write Clock Minimum Pulse Width Low                                                   | 1.8               | –     | ns    |
| $t_{\text{BLKCSU}}$   | Write Block Setup Time                                                                | 0.417             | –     | ns    |
| $t_{\text{BLKCHD}}$   | Write Block Hold Time                                                                 | 0.007             | –     | ns    |
| $t_{\text{DINCSU}}$   | Write Input Data setup Time                                                           | 0.003             | –     | ns    |
| $t_{\text{DINCHD}}$   | Write Input Data hold Time                                                            | 0.142             | –     | ns    |
| $t_{\text{ADDRCSU}}$  | Write Address Setup Time                                                              | 0.091             | –     | ns    |
| $t_{\text{ADDRCHD}}$  | Write Address Hold Time                                                               | 0.255             | –     | ns    |
| $t_{\text{WECSU}}$    | Write Enable Setup Time                                                               | 0.41              | –     | ns    |
| $t_{\text{WECHD}}$    | Write Enable Hold Time                                                                | -0.027            | –     | ns    |
| $F_{\text{max}}$      | Maximum Frequency                                                                     | –                 | 250   | MHz   |



**Figure 16 • I²C Timing Parameter Definition**

## 24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI\_x\_CLK. For timing parameter definitions, refer to Figure 17 on page 102.

**Table 159 • SPI Characteristics**

**Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$**

| Symbol | Description                            | All Devices/Speed Grades |     |     | Unit | Notes |
|--------|----------------------------------------|--------------------------|-----|-----|------|-------|
|        |                                        | Min                      | Typ | Max |      |       |
| sp1    | SPI_[0 1]_CLK minimum period           |                          |     |     |      |       |
|        | SPI_[0 1]_CLK = PCLK/2                 | 12                       | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/4                 | 24.1                     | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/8                 | 48.2                     | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/16                | 0.1                      | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/32                | 0.19                     | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/64                | 0.39                     | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/128               | 0.77                     | —   | —   | μs   | —     |
| sp2    | SPI_[0 1]_CLK minimum pulse width high |                          |     |     |      |       |
|        | SPI_[0 1]_CLK = PCLK/2                 | 6                        | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/4                 | 12.05                    | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/8                 | 24.1                     | —   | —   | ns   | —     |
|        | SPI_[0 1]_CLK = PCLK/16                | 0.05                     | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/32                | 0.095                    | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/64                | 0.195                    | —   | —   | μs   | —     |
|        | SPI_[0 1]_CLK = PCLK/128               | 0.385                    | —   | —   | μs   | —     |

**Notes:**

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:  
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

**Table 163 • SPI Characteristics**

**Worst-Case Automotive Grade 2 Conditions:  $T_J = 125^\circ\text{C}$ ,  $V_{DD} = 1.14\text{ V}$  (continued)**

| Symbol                                                                                                                                                                                                                                                                                                                                                        | Description                                                      | All Devices/Speed Grades    |       |     | Unit | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------|-------|-----|------|-------|
|                                                                                                                                                                                                                                                                                                                                                               |                                                                  | Min                         | Typ   | Max |      |       |
| sp3                                                                                                                                                                                                                                                                                                                                                           | SPI_[0 1]_CLK minimum pulse width low                            |                             |       |     |      |       |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/2                                           | 6                           | –     | –   | ns   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/4                                           | 12.05                       | –     | –   | ns   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/8                                           | 24.1                        | –     | –   | ns   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/16                                          | 0.05                        | –     | –   | µs   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/32                                          | 0.095                       | –     | –   | µs   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/64                                          | 0.195                       | –     | –   | µs   | –     |
|                                                                                                                                                                                                                                                                                                                                                               | SPI_[0 1]_CLK = PCLK/128                                         | 0.385                       | –     | –   | µs   | –     |
| sp4                                                                                                                                                                                                                                                                                                                                                           | SPI_[0 1]_CLK, SPI_[0 1]_DO,<br>SPI_[0 1]_SS rise time (10%-90%) | –                           | 2.77  | –   | ns   | 1     |
| sp5                                                                                                                                                                                                                                                                                                                                                           | SPI_[0 1]_CLK, SPI_[0 1]_DO,<br>SPI_[0 1]_SS fall time (10%-90%) | –                           | 2.906 | –   | ns   | 1     |
| SPI Master Configuration                                                                                                                                                                                                                                                                                                                                      |                                                                  |                             |       |     |      |       |
| sp6m                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DO setup time                                          | (SPI_x_CLK_period/2) – 3.0  | –     | –   | ns   | 2     |
| sp7m                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DO hold time                                           | (SPI_x_CLK_period/2) – 2.5  | –     | –   | ns   | 2     |
| sp8m                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DI setup time                                          | 8                           | –     | –   | ns   | 2     |
| sp9m                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DI hold time                                           | 2.5                         | –     | –   | ns   | 2     |
| SPI Slave Configuration                                                                                                                                                                                                                                                                                                                                       |                                                                  |                             |       |     |      |       |
| sp6s                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DO setup time                                          | (SPI_x_CLK_period/2) – 12.0 | –     | –   | ns   | 2     |
| sp7s                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DO hold time                                           | (SPI_x_CLK_period/2) + 3.0  | –     | –   | ns   | 2     |
| sp8s                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DI setup time                                          | 2                           | –     | –   | ns   | 2     |
| sp9s                                                                                                                                                                                                                                                                                                                                                          | SPI_[0 1]_DI hold time                                           | 3                           | –     | –   | ns   | 2     |
| Notes:                                                                                                                                                                                                                                                                                                                                                        |                                                                  |                             |       |     |      |       |
| 1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:<br><a href="http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models">http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models</a> . |                                                                  |                             |       |     |      |       |
| 2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.                                                                                                                                                                                           |                                                                  |                             |       |     |      |       |

## Datasheet Categories

### Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in Table 1 on page 1 is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Production

This version contains information that is considered to be final.

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**Microsemi Corporate Headquarters**  
One Enterprise, Aliso Viejo,  
CA 92656 USA

**Within the USA:** +1 (800) 713-4113  
**Outside the USA:** +1 (949) 380-6100  
**Sales:** +1 (949) 380-6136  
**Fax:** +1 (949) 215-4996

**E-mail:** [sales.support@microsemi.com](mailto:sales.support@microsemi.com)

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