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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex® -M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 25K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s025ts-1vfg256t2

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8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

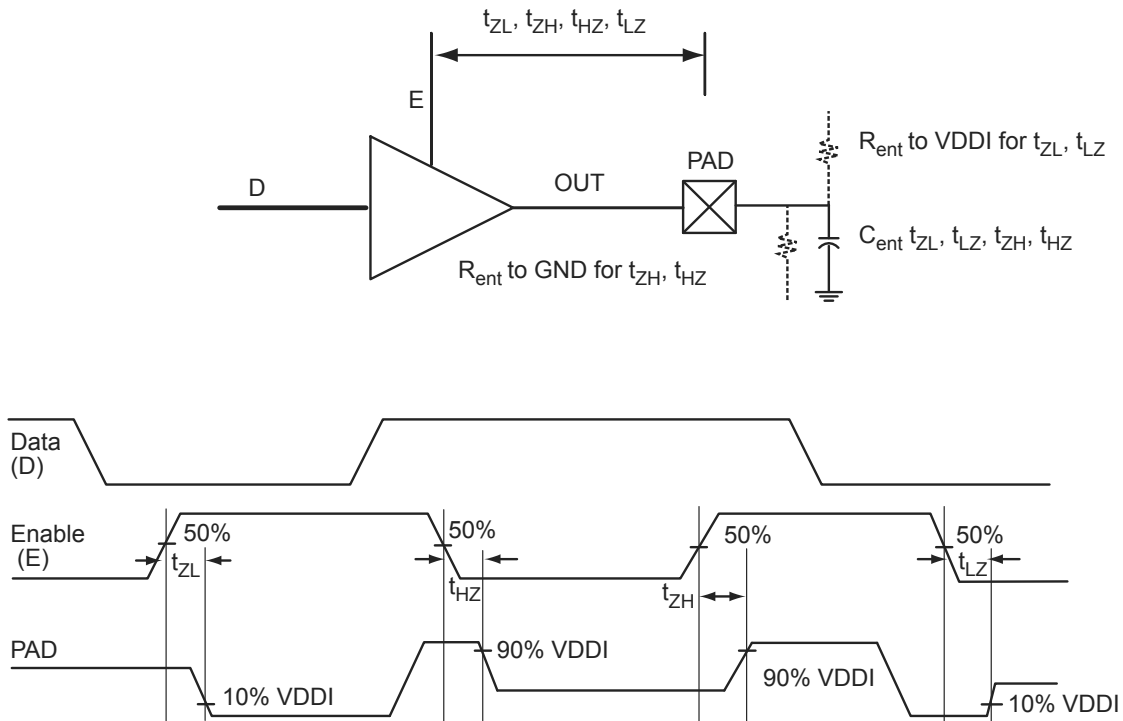


Figure 4 • Tristate Buffer for Enable Path Test Point

Table 17 • Maximum Frequency Summary for Worst-Case Automotive Grade 2 Conditions

Single-Ended I/O	MSIO	MSIOD	DDRIO	Units
PCI 3.3 V	280	–	–	MHz
LVTTL 3.3 V	270	–	–	MHz
LVC MOS 3.3 V	270	–	–	MHz
LVC MOS 2.5 V	180	185	180	MHz
LVC MOS 1.8 V	130	180	180	MHz
LVC MOS 1.5 V	70	95	105	MHz
LVC MOS 1.2 V	50	70	90	MHz
LPDDR - LVC MOS 1.8 V mode	–	–	180	MHz
Voltage-Referenced I/O	MSIO	MSIOD	DDRIO	Units
LPDDR	–	–	180	MHz
HSTL 1.5 V	–	–	180	MHz
SSTL 2.5 V	225	240	180	MHz
SSTL 1.8 V	–	–	300	MHz
SSTL 1.5 V	–	–	300	MHz
Differential I/O	MSIO	MSIOD	DDRIO	Units
LVPECL (input only)	405	–	–	MHz
LVDS 3.3 V	240	240	–	MHz
LVDS 2.5 V	240	240	–	MHz
RS DS	230	240	–	MHz
BLVDS	225	–	–	MHz
MLVDS	225	–	–	MHz
Mini-LVDS	230	240	–	MHz

8.5 Detailed I/O Characteristics

Table 18 • Input Capacitance

Symbol	Definition	Min	Max	Units
CIN	Input Capacitance	–	10	pF

Table 19 • I/O Weak Pull-Up/Pull-Down Resistance Values for DDRIO, MSIO, and MSIOD Banks
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	DDRIO I/O Bank				MSIO I/O Bank				MSIOD I/O Bank				
	R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		R _(WEAK PULL-UP) at VOH (Ω)		R _(WEAK PULL-DOWN) at VOL (Ω)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3 V	N/A	N/A	N/A	N/A	9.9K	14.5K	9.98K	14.9K	N/A	N/A	N/A	N/A	
2.5 V	10K	15.1K	9.98K	15.3K	10K	15K	10.1K	15.6K	9.6K	14.1K	9.5K	13.9K	1,2
1.8 V	10.3K	16.2K	10.3K	16.6K	10.4K	16.2K	10.4K	17.3K	9.7K	14.7K	9.7K	14.5K	1,2
1.5 V	10.6K	17.2K	10.6K	17.9K	10.7K	17.3K	10.8K	18.9K	9.9K	15.3K	9.8K	15K	1,2
1.2 V	11.1K	19.3K	11.2K	20.9K	11.3K	19.7K	11.5K	22.7K	10.3K	16.7K	10K	16.2K	1,2

Notes:

- $R_{(WEAK \text{ PULL-DOWN})} = (VOL_{spec}) / I_{(WEAK \text{ PULL-DOWN MAX})}$
- $R_{(WEAK \text{ PULL-UP})} = (VDDI_{max} - VOH_{spec}) / I_{(WEAK \text{ PULL-UP MIN})}$

Table 20 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (Typical, unless otherwise noted)
3.3 V LVTTTL / LVCMOS / PCI / PCI-X	$0.05 \times VDDI$ (Worst-case)
2.5 V LVCMOS	$0.05 \times VDDI$ (Worst-case)
1.8 V LVCMOS	$0.1 \times VDDI$ (Worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

8.6 Single-Ended I/O Standards

8.6.1 Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs are: LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

8.6.2 3.3 V LVCMOS/LVTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTL) is a general standard for 3.3 V applications.

8.6.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 21 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units	Notes
LVTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	–
LVTTL/LVCMOS 3.3 V DC Input Voltage Specification							
VIH (DC)	DC input logic High		2.0	–	3.45	V	–
VIL (DC)	DC input logic Low		–0.3	–	0.8	V	–
IIH (DC)	Input current High		–	–	10	μA	–
IIL (DC)	Input current Low		–	–	10	μA	–
LVCMOS 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	*
VOL	DC output logic Low		–	–	0.4	V	*
LVTTL 3.3 V DC Output Voltage Specification							
VOH	DC output logic High		2.4	–	–	V	–
VOL	DC output logic Low		–	–	0.4	V	–
Note: * The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.							

Table 22 • LVTTL/LVCMOS 3.3 V Maximum Switching Speeds (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min	Typ	Max	Units
LVTTL/LVCMOS 3.3 V Maximum Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	540	Mbps

Table 23 • LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications (Applicable to MSIO Bank Only)

LVTTL/LVCMOS 3.3 V AC Test Parameter Specifications						
Symbol	Parameters	Conditions	Min	Typ	Max	Units
Vtrip	Measuring/trip point for data path		–	1.4	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	None	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	None	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	None	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.425\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 49 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Fixed Code)	Min	Max		
2 mA	2 mA	2 mA	VDDI × 0.75	VDDI × 0.25	2	2
4 mA	4 mA	4 mA	VDDI × 0.75	VDDI × 0.25	4	4
N/A	N/A	6 mA	VDDI × 0.75	VDDI × 0.25	6	6

8.6.6.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 50 • LVCMOS 1.2 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: T_j=125°C, VDD=1.14 V, VDDI= 1.14 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t _{py}	t _{pys}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Codes)	None	2.539	2.556	ns
LVCMOS 1.2 V (for MSIO I/O Bank)	None	4.888	4.845	ns
	50	6.683	6.605	ns
	75	5.923	5.847	ns
	150	5.29	5.235	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)	None	4.281	4.235	ns
	50	6.806	6.721	ns
	75	5.643	5.564	ns
	150	4.813	4.753	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: T_j=125°C, VDD=1.14 V, VDDI= 1.14 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.2 V (for DDRIO I/O Bank with Fixed Code)							
2 mA	slow	6.938	5.599	6.948	7.568	6.612	ns
	medium	6.11	4.814	6.114	7.201	6.234	ns
	medium_fast	5.675	4.409	5.676	6.971	6.048	ns
	fast	5.633	4.379	5.634	6.958	6.037	ns
4 mA	slow	6.328	4.892	6.316	8.339	7.306	ns
	medium	5.538	4.192	5.521	7.961	6.923	ns
	medium_fast	5.119	3.832	5.097	7.76	6.741	ns
	fast	5.072	3.085	5.051	7.752	6.725	ns

Table 53 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCI-X AC Specifications						
Dmax	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	560	Mbps
PCI/PCI-X AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path (falling edge)		–	$0.615 \times VDDI$	–	V
Vtrip	Measuring/trip point for data path (rising edge)		–	$0.285 \times VDDI$	–	V
Rtt_test	Resistance for data test path		–	25	–	Ω
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Cload	Capacitive loading for data path (t_{DP})		–	10	–	pF

8.6.7.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 54 • PCI/PCIX AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 3.15\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
PCI/PCIX (for MSIO I/O Bank)	None	2.379	2.387	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 55 • PCI/PCIX AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 3.15\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
PCI/PCIX (for MSIO I/O Bank)	2.394	2.274	2.316	6.876	6.242	ns

Table 61 • DDR1/SSTL2 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	450	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17pF load	–	–	480	Mbps
SSTL2 AC Differential Voltage Specifications						
V _{DIFF}	AC Input Differential Voltage		0.7	–	–	V
V _x	AC Differential Cross Point Voltage		$0.5 \times V_{DDI} - 0.2$	–	$0.5 \times V_{DDI} + 0.2$	V
SSTL2 Impedance Specifications						
	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
SSTL2 AC Test Parameters Specifications						
V _{trip}	Measuring/trip point for data path		–	1.25	–	V
R _{ent}	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
C _{ent}	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
R _{tt_test}	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ω
R _{tt_test}	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ω
C _{load}	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t _{py}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns

Table 68 • DDR3 SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only) (continued)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
IOL at VOL	Output minimum sink current		-7.6	–	–	mA
SSTL15 Differential Voltage Specification						
VID	DC input differential voltage		0.2	–	–	V
Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.						

Table 69 • DDR3/SSTL15 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL15 AC Differential Voltage Specification						
VDIFF	AC input differential voltage		0.3	–	–	V
Vx	AC differential cross point voltage		$0.5 \times VDDI$ – 0.150	–	$0.5 \times VDDI +$ 0.150	V
SSTL15 Maximum AC Switching Speed (for DDRIO I/O Banks Only)						
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–	–	600	Mbps
SSTL15 AC Calibrated Impedance Option						
Rref	Supported output driver calibrated impedance	Reference resistor = 240 Ω	–	34, 40	–	Ω
RTT	Effective impedance value (ODT)	Reference resistor = 240 Ω	–	20, 30, 40, 60, 120	–	Ω
SSTL15 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	0.75	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL15 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL15 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 70 • DDR3/SSTL15 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $VDD = 1.14\text{ V}$, $VDDI = 1.425\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t _{PY}	
DDR3/SSTL15 (for DDRIO I/O Bank) – Calibration Mode Only			
Pseudo-Differential	None	1.672	ns
True-Differential	None	1.694	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 76 • LPDDR AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.71\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LPDDR Reduced Drive (for DDRIO I/O Bank)						
Single Ended	2.645	2.431	2.434	2.396	2.398	ns
Differential	2.652	3.044	3.038	2.46	2.455	ns
LPDDR Full Drive (for DDRIO I/O Bank)						
Single Ended	2.532	2.401	2.398	2.368	2.365	ns
Differential	2.546	2.509	2.503	2.852	2.845	ns

8.7.6.3 Minimum and Maximum AC/DC Input and Output Levels Specification using LPDDR-LVCMOS 1.8 V Mode

Table 77 • LPDDR-LVCMOS 1.8 V Mode, Minimum and Maximum DC Input and Output Levels
(Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR-LVCMOS 1.8 V Recommended DC Operating Conditions						
VDDI	Supply Voltage	–	1.710	1.8	1.89	V
LPDDR-LVCMOS 1.8 V Mode DC Input Voltage Specification						
$V_{IH}(\text{DC})$	DC input Logic HIGH for (MSIOD and DDRIO I/O Banks)	–	$0.65 \times V_{DDI}$	–	1.89	V
$V_{IH}(\text{DC})$	DC input Logic HIGH (for MSIO I/O Bank)	–	$0.65 \times V_{DDI}$	–	3.45	V
$V_{IL}(\text{DC})$	DC input Logic LOW	–	-0.3	–	$0.35 \times V_{DDI}$	V
$I_{IH}(\text{DC})$	Input current HIGH	–	–	–	10	μA
$I_{IL}(\text{DC})$	Input current LOW	–	–	–	10	μA
LPDDR-LVCMOS 1.8 V Mode DC Output Voltage Specification						
V_{OH}	DC output Logic HIGH	–	$V_{DDI} - 0.45$	–	–	V
V_{OL}	DC output Logic LOW	–	–	–	0.45	V

Table 78 • LPDDR-LVCMOS 1.8 V Maximum AC Switching Speeds (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
D_{max}	Maximum Data Rate (for DDRIO I/O Bank)	AC Loading: 17pF Load, 8mA Drive and Above/All Slew	–	–	360	Mbps

Table 79 • LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedance Option						
Rodt_cal	Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})	–	–	5	–	pF
Cload	Capacitive Loading for Data Path (t_{DP})	–	–	5	–	pF

Table 80 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	–
8 mA	VDDI – 0.45	0.45	8	8	–
10 mA	VDDI – 0.45	0.45	10	10	–
12 mA	VDDI – 0.45	0.45	12	12	–
16 mA	VDDI – 0.45	0.45	16	16	*
Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance					

8.7.6.4 AC Switching Characteristics

Table 81 • LPPDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns

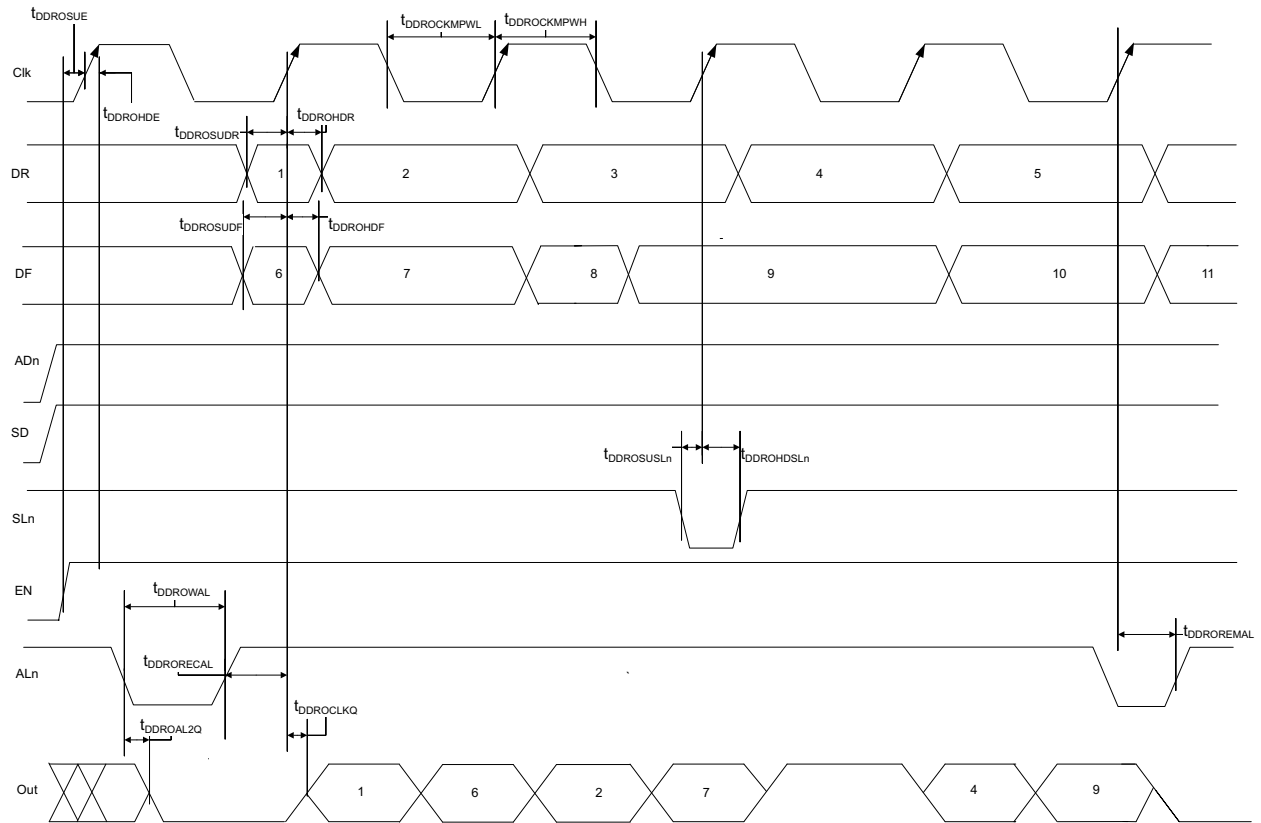


Figure 12 • Output DDR Timing Diagram

9.2 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

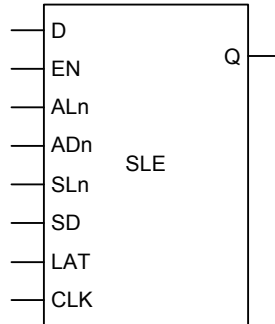


Figure 14 • Sequential Module

Figure 15 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

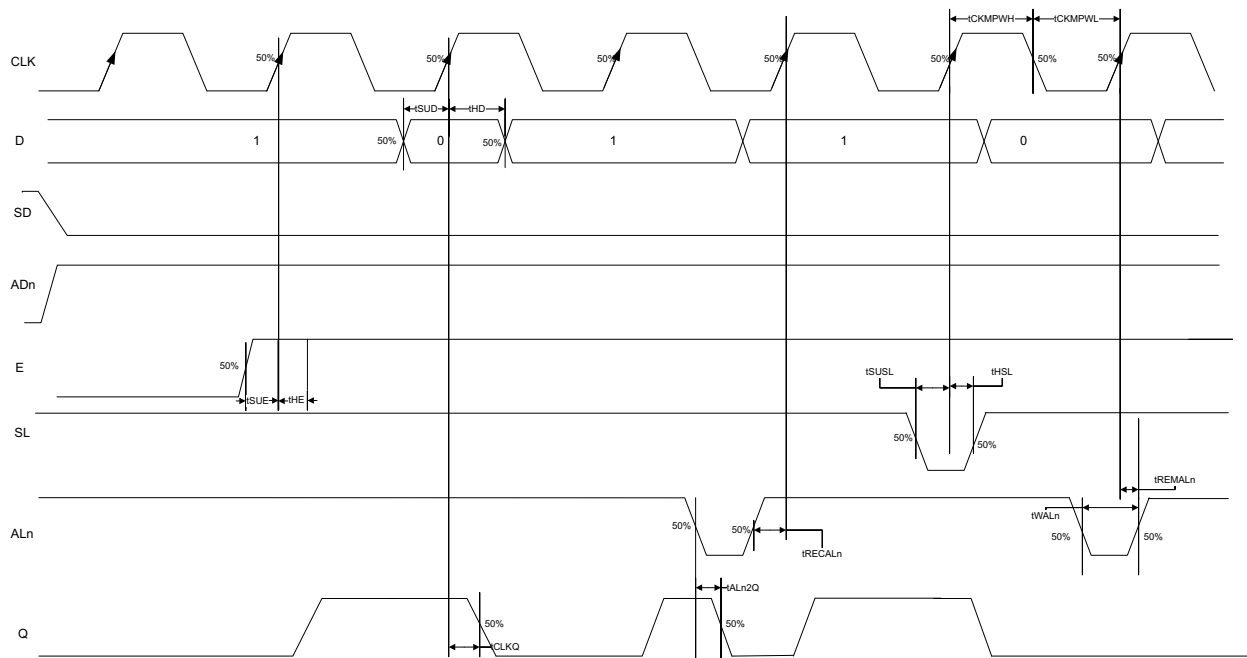


Figure 15 • Sequential Module Timing Diagram

Table 130 • uSRAM (RAM1024x1) in 1024x1 Mode
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.274	ns
	Read Access Time without Pipeline Register	–	1.839	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.041	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.623	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.236	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
t_{CCLKMPWH}	Write Clock Minimum Pulse Width High	1.8	–	ns
t_{CCLKMPWL}	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.003	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
t_{ADDRCSU}	Write Address Setup Time	0.091	–	ns
t_{ADDRCHD}	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
F_{max}	Maximum Frequency	–	250	MHz

22. SFP Transceiver Characteristics

IGLOO2 and SmartFusion2 SERDES complies with small form-factor pluggable (SFP) requirements as specified in SFP INF-80741. Table 150 provides the electrical characteristics.

Table 150 • SFP Transceiver Electrical Characteristics
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Pin	Direction	Differential Peak-Peak Voltage			Unit	Note
		Min	Typ	Max		
RD+/-	Output	1600	–	2400	mV	1
TD+/-	Input	350	–	2400	mV	2

Notes:

1. Based on default SERDES transmitter settings for PCIe Gen1. Lower amplitudes are available through programming changes to TX_AMP setting.
2. Based on Input Voltage Common-Mode (VICM) = 0 V. Requires AC Coupling.

23. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 151 • Transmitter Parameters
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VTX-DIFF-PP	Differential swing PCIe Gen1	0.8	–	1.2	V
VTX-CM-AC-P	Output common mode voltage PCIe Gen1	–	–	20	mV
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen1	0.125	–	–	UI
ZTX-DIFF-DC	Output impedance – differential	80	–	120	Ω
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen1	–	–	500 ps + 2 UI	ps
RLTX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLTX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
TX-LOCK-RST	Transmit PLL lock time from reset	–	–	10	μs

Table 152 • Receiver Parameters

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units
VRX-DIFF-PP-CC	Input levels PCIe Gen1	0.175	–	1.2	V
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	–
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV
VRX-DIFF-PP-CC	Differential input sensitivity Gen1	0.175	–	–	mV
ZRX-DIFF-DC	Differential input termination	80	100	120	Ω
REXT	External calibration resistor	1,188	1,200	1,212	Ω
CDR-LOCK-RST	CDR relock time from reset	–	–	15	μs
RLRX-DIFF	Return loss differential mode PCIe Gen1	–10	–	–	dB
RLRX-CM	Return loss common mode PCIe Gen1	–6	–	–	dB
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV

Table 153 • SERDES Reference Clock AC Specifications

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, Worst-Case $V_{DD} = 1.14\text{V}$

Symbols	Description	Min	Typ	Max	Units
FREFCLK	Reference Clock Frequency	100	–	160	MHz
TRISE	Reference Clock Rise Time	0.6	–	4	V/ns
TFALL	Reference Clock Fall Time	0.6	–	4	V/ns
TCYC	Reference Clock Duty Cycle	40	–	60	%
Mmrefclk	Reference Clock Mismatch	–300	–	300	ppm
SSCref	Reference Spread Spectrum Clock	0	–	5000	ppm

Table 154 • HCSL Minimum and Maximum DC Input Levels (Applicable to SERDES REFCLK Only)

Symbols	Parameters	Min	Typ	Max	Units
Recommended DC Operating Conditions					
VDDI	Supply Voltage	2.375	2.5	2.625	V
HCSL DC Input Voltage Specification					
VI	DC Input voltage	0	–	2.625	V
HCSL Differential Voltage Specification					
VICM	Input common mode voltage	0.05	–	2.4	V
VIDIFF	Input differential voltage	100	–	1100	mV

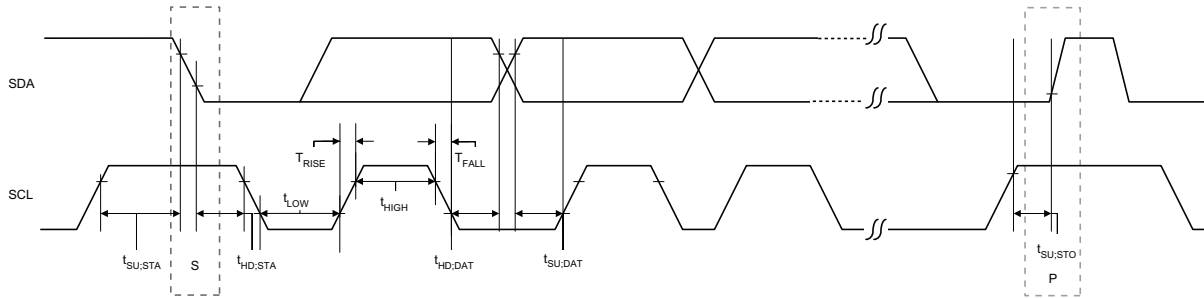


Figure 16 • I²C Timing Parameter Definition

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 102.

Table 159 • SPI Characteristics

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp1	SPI_[0 1]_CLK minimum period					
	SPI_[0 1]_CLK = PCLK/2	12	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/4	24.1	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/8	48.2	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/16	0.1	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/32	0.19	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/64	0.39	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/128	0.77	—	—	μs	—
sp2	SPI_[0 1]_CLK minimum pulse width high					
	SPI_[0 1]_CLK = PCLK/2	6	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/4	12.05	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/8	24.1	—	—	ns	—
	SPI_[0 1]_CLK = PCLK/16	0.05	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/32	0.095	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/64	0.195	—	—	μs	—
	SPI_[0 1]_CLK = PCLK/128	0.385	—	—	μs	—

Notes:

- For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.

Table 159 • SPI Characteristics (continued)
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	0.05	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/32	0.095	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/64	0.195	–	–	µs	–
	SPI_[0 1]_CLK = PCLK/128	0.385	–	–	µs	–
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	–	2.906	–	ns	1
SPI Master Configuration						
sp6m	SPI_[0 1]_DO setup time	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	2.5	–	–	ns	2
SPI Slave Configuration						
sp6s	SPI_[0 1]_DO setup time	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	2	–	–	ns	2
sp9s	SPI_[0 1]_DI hold time	3	–	–	ns	2
Notes:						
1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models .						
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.						



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