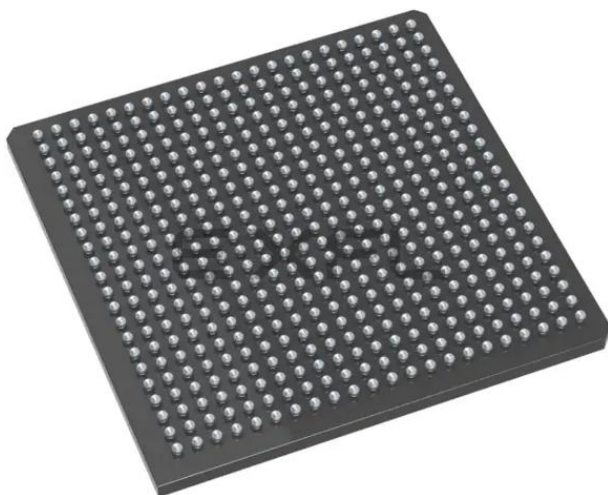




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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex® -M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I ² C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 60K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s060ts-1fgg484t2



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4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

Table 2 • Absolute Maximum Ratings

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	−0.3	1.32	V	—
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	−0.3	3.63	V	—
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	—
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	—
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	−0.3	3.63	V	—
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	—
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	—
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	−0.3	3.63	V	—
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	−0.3	3.63	V	—
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	−0.3	2.75	V	—
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	−0.3	1.32	V	—
SERDES_[01]_VDD	PCIe®/PCS power supply	−0.3	1.32	V	—
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	−0.3	3.63	V	—
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	−0.3	2.75	V	—
VI	I/O Input voltage for MSIO I/O Bank	−0.3	3.63	V	—
	I/O Input voltage for MSIOD/DDRIO I/O Bank	−0.3	2.75	V	—
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	−0.3	3.63	V	—
T _{STG}	Storage temperature	−65	150	°C	*
T _J	Junction temperature	—	135	°C	—

Note: * For flash programming and retention maximum limits, refer to Table 4 on page 4. For recommended operating conditions, refer to Table 3 on page 3.

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

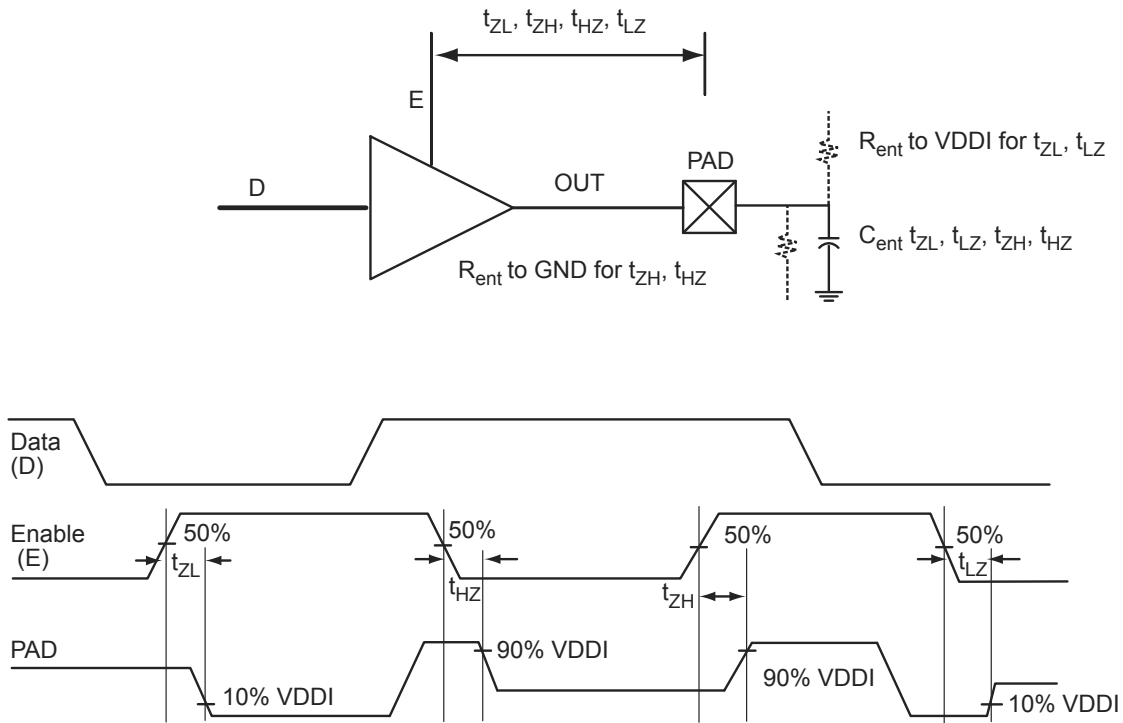


Figure 4 • Tristate Buffer for Enable Path Test Point

8.6.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 38 • LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	3.185	3.171	ns
	50	3.394	3.397	ns
	75	3.322	3.316	ns
	150	3.252	3.239	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.827	2.813	ns
	50	3.043	3.053	ns
	75	2.968	2.963	ns
	150	2.898	2.886	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

Output Drive Selection	Slew Control	Speed Grade -1					Units
		t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
12 mA	slow	3.795	3.096	3.773	6.773	6.067	ns
	medium	3.408	2.764	3.389	6.47	5.743	ns
	medium_fast	3.215	2.599	3.194	6.346	5.61	ns
	fast	3.196	2.584	3.175	6.335	5.604	ns
16 mA	slow	3.744	3.035	3.719	6.944	6.207	ns
	medium	3.358	2.712	3.339	6.657	5.868	ns
	medium_fast	3.175	2.546	3.153	6.547	5.751	ns
	fast	3.156	2.531	3.133	6.541	5.747	ns
LVCMOS 1.8 V (for MSIO I/O Bank)							
2 mA	slow	3.957	4.784	5.023	5.643	5.866	ns
4 mA	slow	3.668	4.162	4.485	6.543	6.382	ns
6 mA	slow	3.586	3.994	4.358	7.622	6.941	ns
8 mA	slow	3.616	3.782	4.162	7.988	7.161	ns
10 mA	slow	3.662	3.732	4.121	8.396	7.423	ns
12 mA	slow	3.75	3.615	4.006	8.576	7.543	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)							
2 mA	slow	3.048	3.692	3.898	5.818	5.609	ns
4 mA	slow	2.5	3.088	3.288	6.421	6.121	ns
6 mA	slow	2.225	2.747	2.937	7.18	6.753	ns
8 mA	slow	2.233	2.72	2.904	7.49	6.992	ns
10 mA	slow	2.263	2.577	2.759	7.851	7.253	ns

8.6.5 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 FPGAs and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.6.5.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 40 • LVCMOS 1.5 V Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Min	Typ	Max	Units
LVCMOS 1.5 V Recommended DC Operating Conditions					
VDDI	Supply voltage	1.425	1.5	1.575	V
LVCMOS 1.5 V DC Input Voltage Specification					
V_{IH} (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)	$0.65 \times V_{DDI}$	–	1.575	V
V_{IH} (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 \times V_{DDI}$	–	2.75	V
V_{IL} (DC)	DC input logic Low	–0.3	–	$0.35 \times V_{DDI}$	V
I_{IH} (DC)	Input current High	–	–	10	μA
I_{IL} (DC)	Input current Low	–	–	10	μA
LVCMOS 1.5 V DC Output Voltage Specification					
V_{OH}	DC output logic High	$V_{DDI} \times 0.75$	–	–	V
V_{OL}	DC output logic Low	–	–	$V_{DDI} \times 0.25$	V

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: $T_J=125^{\circ}\text{C}$, $V_{DD}=1.14\text{ V}$, $V_{DDI}=1.14\text{ V}$ (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	6.092	4.681	6.075	8.685	7.589	ns
	medium	5.342	4.016	5.32	8.33	7.19	ns
	medium_fast	4.949	3.66	4.922	8.139	7.022	ns
	fast	4.903	3.622	4.876	8.107	7.006	ns
LVCMOS 1.2 V (for MSIO I/O Bank)							
2 mA	slow	7.051	7.856	8.541	10.387	8.768	ns
4 mA	slow	7.385	7.027	7.815	11.547	9.444	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
V_{DDI}	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
V_I	DC input voltage		0	–	3.45	V
$I_{IH}(\text{DC})$	Input current High		–	–	10	μA
$I_{IL}(\text{DC})$	Input current Low		–	–	10	μA
PCI/PCIX DC Output Voltage Specification						
V_{OH}	DC output logic High		Per PCI Specification			V
V_{OL}	DC output logic Low		Per PCI Specification			V

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	ODT (On Die Termination) in Ω	Speed Grade -1	Units
		t _{py}	
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 71 • DDR3/SSTL15 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

	Speed Grade -1					Units
	t _{DP}	t _{ZL}	t _{ZH}	t _{HZ}	t _{LZ}	
DDR3 Reduced Drive/SSTL15 Class I (for DDRIO I/O Bank)						
Single Ended	2.832	2.766	2.767	2.658	2.659	ns
Differential	2.848	3.401	3.393	3.173	3.166	ns
DDR3 Full Drive/SSTL15 Class II (for DDRIO I/O Bank)						
Single Ended	2.832	2.76	2.759	2.655	2.655	ns
Differential	2.845	3.397	3.387	3.179	3.171	ns

8.7.6 Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 FPGA and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer. This I/O standard is supported in DDRIO I/O Bank only.

8.7.6.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 72 • LPDDR AC/DC Specifications (for DDRIO IO Bank Only)

Symbols	Parameters	Min	Typ	Max	Units	Notes
Recommended DC Operating Conditions						
VDDI	Supply voltage	1.71	1.8	1.89	V	—
VTT	Termination voltage	0.838	0.900	0.964	V	—
VREF	Input reference voltage	0.838	0.900	0.964	V	—
LPDDR DC Input Voltage Specification						
VIH (DC)	DC input logic High	$0.7 \times V_{DDI}$	—	1.89	V	—
VIL (DC)	DC input logic Low	−0.3	—	$0.3 \times V_{DDI}$	V	—
IIH (DC)	Input current High	—	—	10	μA	—
IIL (DC)	Input current Low	—	—	10	μA	—
LPDDR DC Output Voltage Specification						
LPDDR Reduced Drive						
VOH	DC output logic High	$0.9 \times V_{DDI}$	—	—	V	—
VOL	DC output logic Low	—	—	$0.1 \times V_{DDI}$	V	—
IOH at VOH	Output minimum source DC current	0.1	—	—	mA	—
IOL at VOL	Output minimum sink current	−0.1	—	—	mA	—
LPDDR Full Drive						*
VOH	DC output logic High	$0.9 \times V_{DDI}$	—	—	V	—
VOL	DC output logic Low	—	—	$0.1 \times V_{DDI}$	V	—
IOH at VOH	Output minimum source DC current	0.1	—	—	mA	—

8.8. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero® System-on-Chip (SoC) software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.8.1 LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.8.1.1 Minimum and Maximum Input and Output Levels

Table 83 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V
LVDS DC Input Voltage Specification						
VI	DC Input voltage	2.5 V range	0	–	2.925	V
VI	DC input voltage	3.3 V range	0	–	3.45	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		250	350	450	mV
VOCM	Output common mode voltage		1.125	1.25	1.375	V
VICM	Input common mode voltage		0.05	1.25	2.35	V
VID	Input differential voltage		100	350	600	mV

Table 84 • LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ω differential load	–	–	480	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
LVDS Impedance Specification						
Rt	Termination resistance	–	–	100	–	Ω
LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

8.8.2 B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.8.2.1 Minimum and Maximum AC/DC Input and Output Levels Specification

Table 89 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Bus-LVDS DC Input Voltage Specification						
VI	DC input voltage		0	–	2.925	V
IIH (DC)	Input current High		–	–	10	μA
IIL (DC)	Input current Low		–	–	10	μA
Bus-LVDS DC Output Voltage Specification (for MSIO I/O Bank only)						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Bus-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing (for MSIO I/O Bank only)		65	–	460	mV
VOCM	Output common mode voltage (for MSIO I/O Bank only)		1.1	–	1.5	V
VICM	Input common mode voltage		0.05	–	2.4	V
VID	Input differential voltage		0.1	–	VDDI	V

Table 90 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Bus-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
Bus-LVDS Impedance Specifications						
Rt	Termination resistance		–	27	–	Ω
Bus-LVDS AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF

Table 94 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 95 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)

Worst-case Automotive Grade 2 conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 96 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-case Automotive Grade 2 conditions: $T_j = 125^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 97 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 98 • Mini-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF

8.9.2 Output/Enable Register

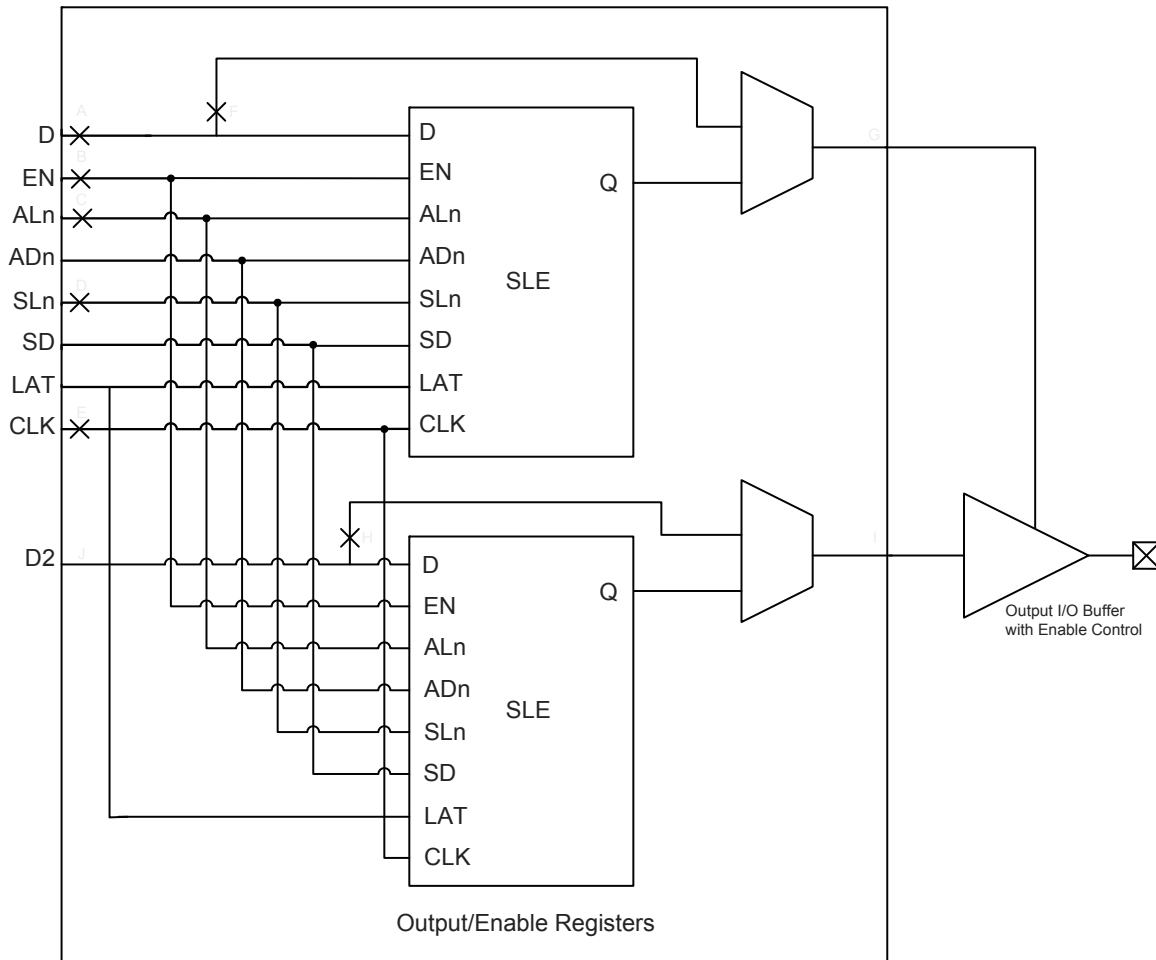


Figure 7 • Timing Model for Output/Enable Register

Table 121 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.546	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns
t_{RDPLESU}	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
t_{RDPLEHD}	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.583	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
t_{PLRSTREM}	Pipelined Register Asynchronous Reset Removal Time	–0.288	–	ns
t_{PLRSTREC}	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
t_{PLRSTMPW}	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.504	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
F_{max}	Maximum Frequency	–	300	MHz

Table 122 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16Kx1
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
t_{CLKMPWH}	Clock Minimum Pulse Width High	1.5	–	ns
t_{CLKMPWL}	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{\text{PLCLKMPWH}}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{\text{PLCLKMPWL}}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns

12. Embedded NVM (eNVM) Characteristics

Table 131 • eNVM Read Performance

Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T _J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
F _{MAXREAD}	eNVM Maximum Read Frequency	25	25	25	25	25	25	MHz

Table 132 • eNVM Page Programming

Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T _J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
t _{PAGEPGM}	eNVM Page Programming Time	40	40	40	40	40	40	ms

13. Crystal Oscillator

Table 133 describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 133 • Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)

Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	20	–	MHz
ACCXTAL	Accuracy	–	–	0.006	%
CYCXTAL	Output duty cycle	–	49-51	47-53	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	200	300	ps
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	200	550	ps
IDYNXTAL	Operating current	–	1.5	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	1	ms

Table 146 • Mathblock With Input Register Used and Output in Bypass Mode

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input Register Used and Output in Bypass Mode		Speed Grade –1		Units
Parameter	Description	Min	Max	
t_{MISU}	Input Register Setup time	0.149	–	ns
t_{MIHD}	Input Register Hold time	0.08	–	ns
$t_{\text{MSRSTENSU}}$	Synchronous Reset/Enable Setup time	0.185	–	ns
$t_{\text{MSRSTENHD}}$	Synchronous Reset/Enable Hold time	-0.012	–	ns
t_{MARSTREM}	Asynchronous Reset Removal time	-0.005	–	ns
t_{MARSTREC}	Asynchronous Reset Recovery time	0.088	–	ns
t_{MICQ}	Input Register Clock to Output delay	–	2.52	ns
t_{MCDIN2Q}	CDIN to Output delay	–	1.951	ns

Table 147 • Mathblock With Input and Output in Bypass Mode

Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Mathblock With Input and Output in Bypass Mode		Speed Grade –1		Units
Parameter	Description	Min	Max	
t_{MIQ}	Input to Output delay	–	2.568	ns
t_{MCDIN2Q}	CDIN to Output delay	–	1.951	ns

Table 159 • SPI Characteristics (continued)
Worst-Case Automotive Grade 2 Conditions: $T_J = 125^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp3	SPI_[0 1]_CLK minimum pulse width low					
	SPI_[0 1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0 1]_CLK = PCLK/16	0.05	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/32	0.095	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/64	0.195	–	–	μs	–
	SPI_[0 1]_CLK = PCLK/128	0.385	–	–	μs	–
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%)	–	2.77	–	ns	1
sp5	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS fall time (10%-90%)	–	2.906	–	ns	1
SPI Master Configuration						
sp6m	SPI_[0 1]_DO setup time	(SPI_x_CLK_period/2) – 3.0	–	–	ns	2
sp7m	SPI_[0 1]_DO hold time	(SPI_x_CLK_period/2) – 2.5	–	–	ns	2
sp8m	SPI_[0 1]_DI setup time	8	–	–	ns	2
sp9m	SPI_[0 1]_DI hold time	2.5	–	–	ns	2
SPI Slave Configuration						
sp6s	SPI_[0 1]_DO setup time	(SPI_x_CLK_period/2) – 12.0	–	–	ns	2
sp7s	SPI_[0 1]_DO hold time	(SPI_x_CLK_period/2) + 3.0	–	–	ns	2
sp8s	SPI_[0 1]_DI setup time	2	–	–	ns	2
sp9s	SPI_[0 1]_DI hold time	3	–	–	ns	2
Notes:						
1. For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models .						
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.						

Datasheet Information

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 2 (September 2015)	Updated Table 9: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Typical Process" for typical process values (SAR 69218).	8
	Updated Table 10: "SmartFusion2 and IGLOO2 Quiescent Supply Current – Worst-Case Process" for worst-case process values (SAR 69218).	8
	Updated Table 139: "IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Jitter Specifications" for FGG (SAR 69806).	90
Revision 1 (June 2015)	Initial release.	NA

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