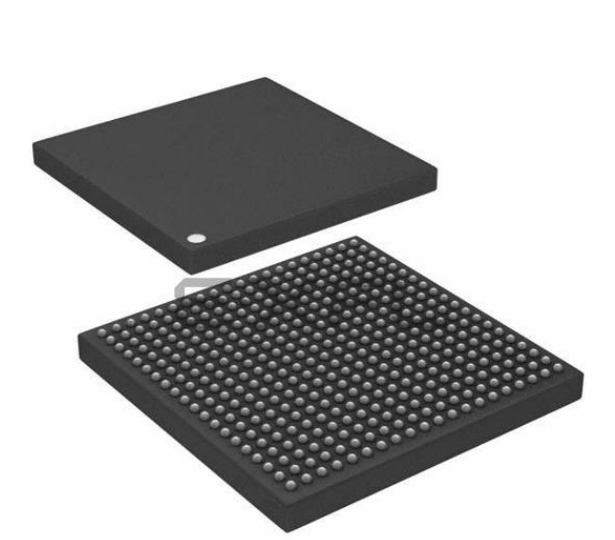

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	256KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 60K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	400-LFBGA
Supplier Device Package	400-VFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s060ts-1vfg400t2

4. General Specifications

4.1 Operating Conditions

Stresses beyond those listed in Table 2 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 2 is not implied.

Table 2 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits		Units	Notes
		Min	Max		
VDD	DC core supply voltage. Must always power this pin.	–0.3	1.32	V	–
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	–0.3	3.63	V	–
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	–0.3	3.63	V	–
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	–0.3	3.63	V	–
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	–0.3	3.63	V	–
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	–0.3	3.63	V	–
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	–0.3	2.75	V	–
SERDES_[01]_L[0123]_VDDAIO	TX/RX analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	–0.3	1.32	V	–
SERDES_[01]_VDD	PCIe®/PCS power supply	–0.3	1.32	V	–
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	–0.3	3.63	V	–
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	–0.3	2.75	V	–
VI	I/O Input voltage for MSIO I/O Bank	–0.3	3.63	V	–
	I/O Input voltage for MSIOD/DDRIO I/O Bank	–0.3	2.75	V	–
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	–0.3	3.63	V	–
T_{STG}	Storage temperature	–65	150	°C	*
T_J	Junction temperature	–	135	°C	–

*Note: * For flash programming and retention maximum limits, refer to Table 4 on page 4. For recommended operating conditions, refer to Table 3 on page 3.*

Table 5 • **Embedded Flash Limits**

Product Grade	Element	Programming Temperature	Maximum Operating Temperature	Programming Cycles	Retention (Biased/Unbiased)
Automotive Grade 2	Embedded flash	Min T_J = -40°C Max T_J = 125°C	Min T_J = -40°C Max T_J = 125°C	< 10,000 cycles per pages, up to one million cycles per eNVM array	10 Years

Table 6 • **Device Storage Temperature and Retention**

Product Grade	Storage Temperature (Tstg)	Retention
Automotive Grade 2	Min T_J = -40°C Max T_J = 125°C	10 Years

4.2 Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% or the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3 Thermal Characteristics

4.3.1 Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures.

EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 7 • **Package Thermal Resistance**

Product M2GL/M2S	θ_{JA} Still Air	θ_{JA} 1.0 m/s	θ_{JA} 2.5 m/s	θ_{JB}	θ_{JC}	Units
005						
FGG484	19.36	15.81	14.63	9.74	5.27	°C/W
VFG256	41.30	38.16	35.30	28.41	3.94	°C/W
VFG400	20.19	16.94	15.41	8.86	4.95	°C/W
010						
FGG484	18.22	14.83	13.62	8.83	4.92	°C/W
VFG256	37.36	34.26	31.45	24.84	7.89	°C/W
VFG400	19.40	15.75	14.22	8.11	4.22	°C/W
025						
FGG484	17.03	13.66	12.45	7.66	4.18	°C/W
VFG256	33.85	30.59	27.85	21.63	6.13	°C/W
VFG400	18.36	14.89	13.36	7.12	3.41	°C/W
060						
FGG484	15.40	12.06	10.85	6.14	3.15	°C/W
VFG400	17.45	14.01	12.47	6.22	2.69	°C/W
FGG676	15.49	12.21	11.06	7.07	3.87	°C/W
090						
FGG484	14.64	11.37	10.16	5.43	2.77	°C/W
FGG676	14.52	11.19	10.37	6.17	3.24	°C/W

4.3.2 Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 125°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL060TS-1FGG484 package at Automotive Grade 2 temperature and in still air, where:

θ_{JA} = 15.4°C/W (taken from Table 7 on page 6).

T_A = 105°C

$$\text{Maximum Power Allowed} = \frac{125°C - 105°C}{15.4°C/W} = 1.3\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

8.6.4.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 38 • LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	3.185	3.171	ns
	50	3.394	3.397	ns
	75	3.322	3.316	ns
	150	3.252	3.239	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.827	2.813	ns
	50	3.043	3.053	ns
	75	2.968	2.963	ns
	150	2.898	2.886	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 39 • LVCMOS 1.8 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.8 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	4.681	4.017	4.69	5.388	4.852	ns
	medium	4.211	3.599	4.219	5.058	4.488	ns
	medium_fast	3.978	3.392	3.986	4.874	4.327	ns
	fast	3.953	3.373	3.961	4.858	4.316	ns
4 mA	slow	4.355	3.657	4.346	5.967	5.399	ns
	medium	3.886	3.246	3.879	5.628	5.01	ns
	medium_fast	3.656	3.05	3.647	5.461	4.845	ns
	fast	3.635	3.033	3.626	5.447	4.838	ns
6 mA	slow	4.105	3.422	4.092	6.221	5.599	ns
	medium	3.68	3.05	3.668	5.9	5.257	ns
	medium_fast	3.477	2.867	3.463	5.739	5.118	ns
	fast	3.451	2.849	3.437	5.72	5.104	ns
8 mA	slow	4.015	3.32	3.998	6.458	5.808	ns
	medium	3.59	2.947	3.574	6.129	5.449	ns
	medium_fast	3.383	2.761	3.366	5.963	5.304	ns
	fast	3.357	2.746	3.34	5.954	5.289	ns
10 mA	slow	3.888	3.18	3.864	6.739	6.045	ns
	medium	3.485	2.822	3.467	6.422	5.7	ns
	medium_fast	3.281	2.642	3.26	6.277	5.553	ns
	fast	3.258	2.627	3.238	6.27	5.546	ns

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.14 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	6.092	4.681	6.075	8.685	7.589	ns
	medium	5.342	4.016	5.32	8.33	7.19	ns
	medium_fast	4.949	3.66	4.922	8.139	7.022	ns
	fast	4.903	3.622	4.876	8.107	7.006	ns
LVCMOS 1.2 V (for MSIO I/O Bank)							
2 mA	slow	7.051	7.856	8.541	10.387	8.768	ns
4 mA	slow	7.385	7.027	7.815	11.547	9.444	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
IIH(DC)	Input current High		–	–	10	µA
IIL(DC)	Input current Low		–	–	10	µA
PCI/PCIX DC Output Voltage Specification						
VOH	DC output logic High		Per PCI Specification			V
VOL	DC output logic Low		Per PCI Specification			V

Table 62 • **DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t_{PY}	
SSTL2 (MSIOD I/O Bank)			
Pseudo-Differential	None	2.721	ns
True-Differential	None	2.71	ns

Table 63 • **DDR1/SSTL2 AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
SSTL2 Class I						
DDRIO I/O Bank						
Single Ended	2.457	2.145	2.137	2.302	2.293	ns
Differential	2.454	2.38	2.375	2.589	2.584	ns
MSIO I/O Bank						
Single Ended	2.283	2.255	2.243	2.286	2.273	ns
Differential	2.434	2.702	2.691	2.39	2.381	ns
MSIOD I/O Bank						
Single Ended	1.646	1.59	1.589	1.82	1.818	ns
Differential	1.774	1.93	1.926	2.012	2.007	ns
SSTL2 Class II						
DDRIO I/O Bank						
Single Ended	2.317	2.06	2.053	2.229	2.221	ns
Differential	2.32	2.213	2.21	2.57	2.565	ns
MSIO I/O Bank						
Single Ended	2.563	2.208	2.19	2.205	2.187	ns
Differential	2.703	2.566	2.555	2.363	2.353	ns

8.8.1.2 LVDS25 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 85 • LVDS25 Receiver Characteristics
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
LVDS (for MSIO I/O Bank)	None	3.061	ns
	100	3.057	ns
LVDS (for MSIOD I/O Bank)	None	2.792	ns
	100	2.787	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 86 • LVDS25 Transmitter Characteristics
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS (for MSIO I/O Bank)	2.299	2.602	2.589	2.305	2.32	ns
LVDS (for MSIOD I/O Bank)						
No pre-emphasis	1.656	1.845	1.838	1.992	1.969	ns
Min pre-emphasis	1.583	1.868	1.866	2.018	1.998	ns
Med pre-emphasis	1.559	1.893	1.886	2.045	2.021	ns

8.8.1.3 LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 87 • LVDS33 Receiver Characteristics
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

	On Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
LVDS33 (for MSIO I/O Bank)	None	2.763	ns
	100	2.76	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 88 • LVDS33 Transmitter Characteristics
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 3.15 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVDS33 (for MSIO I/O Bank)	2.069	2.112	2.106	2.078	2.09	ns

Table 94 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
M-LVDS Maximum AC Switching Speeds						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	450	Mbps
M-LVDS Impedance Specification						
Rt	Termination resistance	–	–	50	–	Ω
M-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 95 • M-LVDS AC Switching Characteristics for Receiver (Input Buffers)
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
M-LVDS (for MSIO I/O Bank)	None	3.011	ns
	100	3.006	ns
M-LVDS (for MSIOD I/O Bank)	None	2.722	ns
	100	2.725	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 96 • M-LVDS AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	Speed Grade –1					Units
	t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
M-LVDS (for MSIO I/O Bank)	2.78	2.632	2.616	2.447	2.436	ns

Table 101 • **RSDS DC Voltage Specification (continued)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
VICM	Input common mode voltage		0.3	–	1.5	V
VID	Input differential voltage		100	–	600	mV

Table 102 • **RSDS AC Specifications**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
RSDS Maximum AC Switching Speed						
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
RSDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
RSDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

8.8.5.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 103 • **RSDS AC Switching Characteristics for Receiver (Input Buffers)**
Worst-case Automotive Grade 2 conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 2.375 V

	On-Die Termination (ODT) in Ω	Speed Grade –1	Units
		t_{PY}	
RSDS (for MSIO I/O Bank)	None	3.112	ns
	100	3.108	ns
RSDS (for MSIOD I/O Bank)	None	2.832	ns
	100	2.821	ns

8.10.4 Output DDR Module

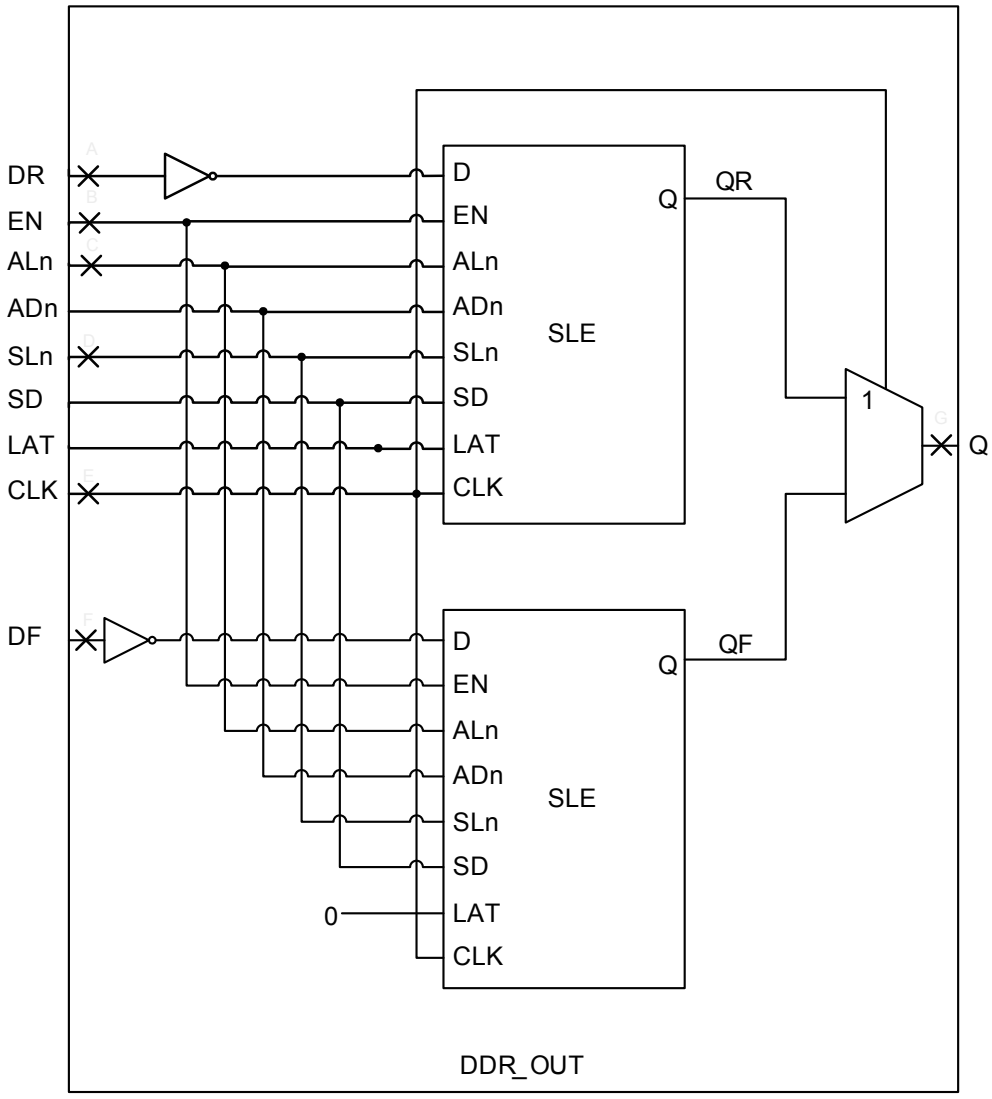

***Figure 11* • Output DDR Module**

Table 116 • **M2S010T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.598	0.639	ns
t_{RCKH}	Input High Delay for Global Clock	1.116	1.192	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.076	ns

Table 117 • **M2S005T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.736	0.789	ns
t_{RCKH}	Input High Delay for Global Clock	0.927	0.995	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.068	ns

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.473	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.631	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.34	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns

Table 123 • **RAM1K18 – Two-Port Mode for Depth × Width Configuration 512x36**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.346	ns
	Read Access Time without Pipeline Register	–	2.322	ns
t_{ADDRSU}	Address Setup Time	0.323	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.348	–	ns
t_{DHD}	Data Hold Time	0.114	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.208	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.322	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.463	–	ns
t_{RDEHD}	Read Enable Hold Time	0.173	–	ns
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.561	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.402	–	ns
t_{WEHD}	Write Enable Hold Time	0.25	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 130 • **uSRAM (RAM1024x1) in 1024x1 Mode**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.274	ns
	Read Access Time without Pipeline Register	–	1.839	ns
t_{ADDRSU}	Read Address Setup Time in Synchronous Mode	0.311	–	ns
	Read Address Setup Time in Asynchronous Mode	2.041	–	ns
t_{ADDRHD}	Read Address Hold Time in Synchronous Mode	0.141	–	ns
	Read Address Hold Time in Asynchronous Mode	-0.623	–	ns
t_{RDENSU}	Read Enable Setup Time	0.287	–	ns
t_{RDENHD}	Read Enable Hold Time	0.059	–	ns
t_{BLKSU}	Read Block Select Setup Time	1.898	–	ns
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.236	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.003	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
Fmax	Maximum Frequency	–	250	MHz

14. On-Chip Oscillator

Table 136 and Table 137 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 136 • **Electrical Characteristics of the 50 MHz RC Oscillator**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter		200	500	ps
		Cycle-to-Cycle Jitter		320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 137 • **Electrical Characteristics of the 1 MHz RC Oscillator**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	µs

15. Clock Conditioning Circuits (CCC)

Table 138 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032	–	200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	µs	–

18. System Controller SPI Characteristics

Table 142 • **System Controller SPI Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Typ	Max		–
sp1	SC_SPI_SCK minimum period	–	20	–	–	ns	–
sp2	SC_SPI_SCK minimum pulse width high	–	10	–	–	ns	–
sp3	SC_SPI_SCK minimum pulse width low	–	10	–	–	ns	–
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.239	–	ns	*
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	I/O Configuration: LVTTL 3.3V- 20mA AC Loading: 35pF Test Conditions: Typical Voltage, 25C	–	1.245	–	ns	*
sp6	Data from master (SC_SPI_SDO) setup time	–	160	–	–	ns	–
sp7	Data from master (SC_SPI_SDO) hold time	–	160	–	–	ns	–
sp8	SC_SPI_SDI setup time	–	20	–	–	ns	–
sp9	SC_SPI_SDI hold time	–	20	–	–	ns	–

*Note: *For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models. Use the supported I/O Configurations for the System Controller SPI in Table 143.*

Table 143 • **Supported I/O Configurations for System Controller SPI (for MSIO Bank Only)**

Voltage Supply	I/O Drive Configuration	Units
3.3 V	20	mA
2.5 V	16	mA
1.8 V	12	mA
1.5 V	8	mA
1.2 V	4	mA

20. Flash*Freeze Timing Characteristics

Table 148 • **Flash*Freeze Entry and Exit Times**
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V

Symbols	Parameters	Conditions	Entry/Exit Timing	Units	Notes
TFF_ENTRY	Entry time	eNVM and MSS/HPMS PLL = ON	160	µs	1
		eNVM and MSS/HPMS PLL = OFF	215	µs	1
TFF_EXIT	Exit Time with respect to MSS PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	100	µs	1
		eNVM = ON and MSS/HPMS PLL =OFF during F*F and MSS/HPMS PLL turned back on at exit	136	µs	1
		eNVM and MSS PLL = OFF during F*F and both are turned back on at exit	200	µs	1
		eNVM = OFF and MSS PLL = ON during F*F and eNVM turned back on at exit	200	µs	1
	Exit Time with respect to Fabric PLL Lock	eNVM and MSS/HPMS PLL = ON during F*F	1.5	ms	1, 2
		eNVM and MSS PLL = OFF during F*F and both are turned back on at exit	1.5	ms	1, 2
	Exit Time with respect to Fabric buffer output	eNVM and MSS/HPMS PLL = ON during F*F	21	µs	1, 2
		eNVM and MSS PLL =O FF during F*F and both are turned back on at exit	65	µs	1

Notes:

1. *F*F entry and exit times were measured with FCLK = 100 MHz*
2. *PLL Lock Delay set to 1024 cycles (default)*

21. DDR Memory Interface Characteristics

Table 149 • **DDR Memory Interface Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Standard	Supported Data Rate			Unit
	Min	Typ	Max	
DDR3	667			Mbps
DDR2	667			Mbps
LPDDR	50	—	400	Mbps

Table 155 • **HCSL Maximum AC Switching Speeds (Applicable to SERDES REFCLK Only)**

Symbols	Parameters	Conditions	Min	Typ	Max	Units
HCSL AC Specifications						
Fmax	Maximum Data Rate (for MSIO IO Bank)	–	–	–	350	Mbps
HCSL Impedance Specifications						
Rt	Termination Resistance	–	–	100	–	Ω

24. SmartFusion2 Specifications

24.1 MSS Clock Frequency

Table 156 • **Maximum Frequency for MSS Main Clock**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	Speed Grade –1	Units
M3_CLK	Maximum frequency for the MSS Main Clock (FCLK)	133	MHz

24.2 SmartFusion2 Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 16 on page 100.

Table 157 • **I2C Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 17 for more information. I/O standard used for illustration: MSIO bank– LVTTL 8 mA low drive.	–0.3	–	0.8	V	–
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 17 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	2	–	3.45	V	–
VHYS	Hysteresis of Schmitt triggered inputs for VDDI > 2 V	Refer to Table 20 on page 17 for more information.	0.05 x VDDI	–	–	V	–
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 17 for more information.	–	–	10	µA	–
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 17 for more information.	–	–	10	µA	–
Tir	Input rise time	Standard Mode	–	–	1000	ns	–
		Fast Mode	–	–	300	ns	–
Tif	Input fall time	Standard Mode	–	–	300	ns	–
		Fast Mode	–	–	300	ns	–

Table 157 • **I2C Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Definition	Conditions	Min	Typ	Max	Units	Notes
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 17 for more information. I/O standard used for illustration: MSIO bank – LVTTL 8 mA low drive.	–	–	0.4	V	–
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	–
t_{OF}	Output fall time from VIHMin to VILMax	VIHmin to VILMax, Cload = 400 pF	–	21.04	–	ns	1
		VIHmin to VILMax, Cload = 100 pF	–	5.556	–	ns	–
t_{OR}	Output rise time from VILMax to VIHMin	VILMax to VIHmin, Cload = 400pF	–	19.887	–	ns	1
		VILMax to VIHmin, Cload = 100pF	–	5.218	–	ns	–
Rpull-up	Output buffer maximum pull-down resistance	–	–	–	50	Ω	2, 3
Rpull-down	Output buffer maximum pull-up resistance	–	–	–	131.25	Ω	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	–
		Standard mode	–	–	100	Kbps	–
t_{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	–

Notes:

1. *These values are provided for MSIO Bank - LVTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
3. *R(PULL-DOWN-MAX) = (VOLspec) / IOLspec*
4. *R(PULL-UP-MAX) = (VDDImax – VOHspec) / IOHspec*

Table 158 • **I2C Switching Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Definition	Conditions	Speed Grade –1		Units
			Min	Max	
t_{LOW}	Low period of I2C_x_SCL	–	1	–	pclk cycles
t_{HIGH}	High period of I2C_x_SCL	–	1	–	pclk cycles
$t_{HD;STA}$	START hold time	–	1	–	pclk cycles
$t_{SU;STA}$	START setup time	–	1	–	pclk cycles
$t_{HD;DAT}$	DATA hold time	–	1	–	pclk cycles
$t_{SU;DAT}$	DATA setup time	–	1	–	pclk cycles
$t_{SU;STO}$	STOP setup time	–	1	–	pclk cycles

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