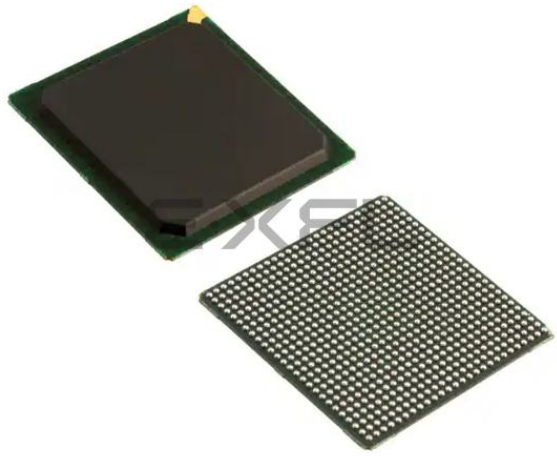

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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	ARM® Cortex®-M3
Flash Size	512KB
RAM Size	64KB
Peripherals	DDR, PCIe, SERDES
Connectivity	CANbus, Ethernet, I²C, SPI, UART/USART, USB
Speed	166MHz
Primary Attributes	FPGA - 90K Logic Modules
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m2s090ts-1fgg676t2

Microsemi

SmartFusion2 and IGLOO2 Automotive Grade 2 AC/DC Electrical Characteristics

1. Introduction

Microsemi®'s automotive grade SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) and IGLOO®2 FPGA families offer the best-in-class security, industry leading high reliability and lowest static power in a flash-based fabric. With a strong heritage of supplying to Military and Aviation customers, Microsemi automotive grade devices are ideally suited to meet the demands of the automotive industry providing the lowest total-cost-of-ownership. These next-generation devices integrate an industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, high-performance SERDES communications interfaces on a single chip with extended temperature support.

Automotive grade SmartFusion2 and IGLOO2 devices offer up to 90 K Logic Elements, up to 5 MB of embedded RAM, up to 4 SERDES lanes, up to 2 PCIe endpoints and integrated hard DDR3 memory controllers with single error correct and double error detect. IGLOO2 automotive grade devices integrate a high-performance memory subsystem (HPMS) with on-chip flash, 32 kbyte embedded SRAM, and multiple DMA controllers. SmartFusion2 automotive grade SoC FPGAs provide a low-power real time microcontroller subsystem (MSS) with an embedded ARM® Cortex™-M3 encapsulating the benefits of HPMS along with a rich set of industry standard peripherals including Ethernet, USB, and CAN.

SmartFusion2 and IGLOO2 FPGAs are the best alternative to ASICs and SRAM based FPGAs with their advantages of Zero FIT reliability, tamper-free advanced security, industry's lowest static power and supply assurance for long product lifetime support.

2. Device Status

The following SmartFusion2 and IGLOO2 devices are available. For more information on device status, refer to the "Datasheet Categories".

Table 1 • **IGLOO2 FPGA and SmartFusion2 SoC FPGA Device Status**

Design Security Device Densities	Status
005S	Production
010TS	Production
025TS	Production
060TS	Preliminary
090TS	Production

3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

- PB0135: Automotive Grade IGLOO2 FPGAs Product Brief
- DS0124: IGLOO2 Pin Descriptions
- PB0136: Automotive Grade SmartFusion2 SoC FPGAs Product Brief
- DS0115: SmartFusion2 Pin Descriptions

Table 15 • **Timing Model Parameters (continued)**

Index	Parameter	Description	Speed Grade –1	Units	Notes
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.283	ns	Refer to page 38 for more information
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12mA, fast slew on the DDRIO Bank	3.703	ns	Refer to page 28 for more information

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 FPGA and SmartFusion2 SoC FPGA families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the “I/Os” section of the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide*.

8.1 Input Buffer and AC Loading

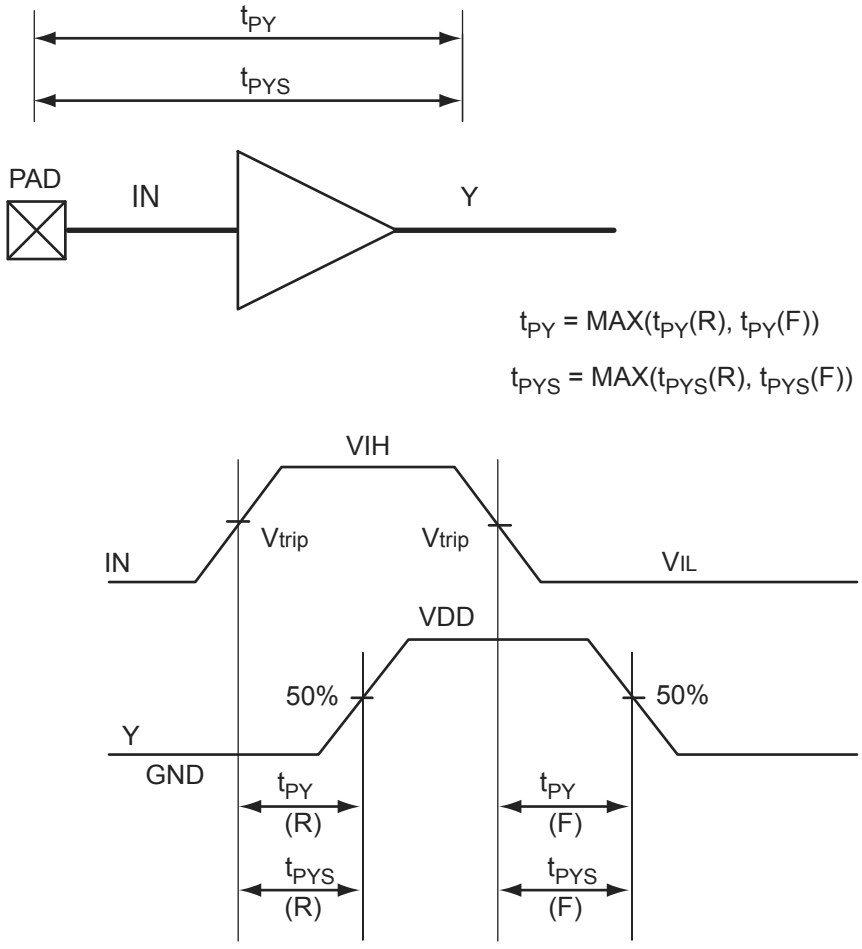

Figure 2 • **Input Buffer AC Loading**

8.6.5.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 44 • LVCMOS 1.5 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.425 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)	None	2.19	2.216	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	None	3.679	3.652	ns
	50	4.151	4.126	ns
	75	3.984	3.953	ns
	150	3.823	3.791	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	None	3.262	3.229	ns
	50	3.76	3.739	ns
	75	3.555	3.52	ns
	150	3.395	3.359	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 45 • LVCMOS 1.5 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI=1.425 V

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
LVCMOS 1.5 V (for DDRIO I/O Bank with Fixed Codes)							
2 mA	slow	5.712	4.796	5.735	5.814	5.138	ns
	medium	5.094	4.274	5.114	5.484	4.779	ns
	medium_fast	4.793	4.013	4.81	5.288	4.625	ns
	fast	4.762	3.98	4.78	5.261	4.615	ns
4 mA	slow	4.966	4.133	4.956	6.763	6.05	ns
	medium	4.412	3.62	4.401	6.433	5.664	ns
	medium_fast	4.145	3.358	4.131	6.249	5.507	ns
	fast	4.116	3.338	4.103	6.238	5.498	ns
6 mA	slow	4.744	3.869	4.728	7.173	6.383	ns
	medium	4.212	3.382	4.195	6.837	6.004	ns
	medium_fast	3.951	3.135	3.93	6.668	5.861	ns
	fast	3.919	3.11	3.899	6.644	5.845	ns

Table 51 • LVCMOS 1.2 V AC Switching Characteristics for Transmitter (Output and Tristate Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J=125°C, VDD=1.14 V, VDDI= 1.14 V (continued)

Output Drive Selection	Slew Control	Speed Grade –1					Units
		t_{DP}	t_{ZL}	t_{ZH}	t_{HZ}	t_{LZ}	
6 mA	slow	6.092	4.681	6.075	8.685	7.589	ns
	medium	5.342	4.016	5.32	8.33	7.19	ns
	medium_fast	4.949	3.66	4.922	8.139	7.022	ns
	fast	4.903	3.622	4.876	8.107	7.006	ns
LVCMOS 1.2 V (for MSIO I/O Bank)							
2 mA	slow	7.051	7.856	8.541	10.387	8.768	ns
4 mA	slow	7.385	7.027	7.815	11.547	9.444	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)							
2 mA	slow	4.048	5.123	5.552	8.401	7.824	ns
4 mA	slow	3.941	4.406	4.814	9.422	8.656	ns

8.6.7 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.6.7.1 Minimum and Maximum Input and Output Levels Specification

Table 52 • PCI/PCI-X DC Voltage Specification (Applicable to MSIO Bank Only

Symbols	Parameters	Conditions	Min	Typ	Max	Units
PCI/PCIX Recommended DC Operating Conditions						
VDDI	Supply voltage		3.15	3.3	3.45	V
PCI/PCIX DC Input Voltage Specification						
VI	DC input voltage		0	–	3.45	V
IIH(DC)	Input current High		–	–	10	µA
IIL(DC)	Input current Low		–	–	10	µA
PCI/PCIX DC Output Voltage Specification						
VOH	DC output logic High		Per PCI Specification			V
VOL	DC output logic Low		Per PCI Specification			V

Table 61 • DDR1/SSTL2 AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
SSTL2 Maximum AC Switching Speeds						
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	360	Mbps
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	450	Mbps
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17pF load	–	–	480	Mbps
SSTL2 AC Differential Voltage Specifications						
VDIFF	AC Input Differential Voltage		0.7	–	–	V
Vx	AC Differential Cross Point Voltage		0.5 × VDDI - 0.2	–	0.5 × VDDI + 0.2	V
SSTL2 Impedance Specifications						
	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ω	–	20, 42	–	Ω
SSTL2 AC Test Parameters Specifications						
Vtrip	Measuring/trip point for data path		–	1.25	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF
Rtt_test	Reference resistance for data test path for SSTL2 Class I (t_{DP})		–	50	–	Ω
Rtt_test	Reference resistance for data test path for SSTL2 Class II (t_{DP})		–	25	–	Ω
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF

8.7.3.2 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 62 • DDR1/SSTL2 AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI= 2.375 V

	ODT (On Die Termination) in Ω	Speed Grade –1	Units
		t_{PY}	
SSTL2 (DDRIO I/O Bank)			
Pseudo-Differential	None	1.613	ns
True-Differential	None	1.647	ns
SSTL2 (MSIO I/O Bank)			
Pseudo-Differential	None	3.083	ns
True-Differential	None	3.028	ns

Table 79 • LPDDR-LVCMOS 1.8 V AC Test Parameters and Driver Impedance Specifications (Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min	Typ	Max	Units
LPDDR - LVCMOS 1.8 V Calibrated Impedance Option						
Rodt_cal	Supported Output Driver Calibrated Impedance (for DDRIO I/O Bank)	–	–	75, 60, 50, 33, 25, 20	–	Ω
LPDDR- LVCMOS 1.8 V AC Test Parameters Specifications						
Vtrip	Measuring/Trip Point for Data Path	–	–	0.9	–	V
Rent	Resistance for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	2k	–	Ω
Cent	Capacitive Loading for Enable Path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})	–	–	5	–	pF
Cload	Capacitive Loading for Data Path ($t_{DP)}$	–	–	5	–	pF

Table 80 • LPDDR-LVCMOS 1.8 V Mode Transmitter Drive Strength Specification (Applicable to DDRIO I/O Bank Only)

Output Drive Selection	VOH (V) Min	VOL (V) Max	IOH (at VOH) mA	IOL (at VOL) mA	Notes
2 mA	VDDI – 0.45	0.45	2	2	–
4 mA	VDDI – 0.45	0.45	4	4	–
6 mA	VDDI – 0.45	0.45	6	6	–
8 mA	VDDI – 0.45	0.45	8	8	–
10 mA	VDDI – 0.45	0.45	10	10	–
12 mA	VDDI – 0.45	0.45	12	12	–
16 mA	VDDI – 0.45	0.45	16	16	*
*Note: * 16mA Drive Strengths, All Slews, meet LPDDR JEDEC electrical compliance*					

8.7.6.4 AC Switching Characteristics

Table 81 • LPPDR - LVCMOS 1.8 V AC Switching Characteristics for Receiver (Input Buffers)
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V, VDDI = 1.71 V

	ODT (On Die Termination) in Ω	Speed Grade –1		Units
		t_{PY}	t_{PYS}	
LPDDR-LVCMOS 1.8 mode (for DDRIO I/O Bank with Fixed Codes)	None	2.071	2.213	ns

8.8.4 Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.8.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 97 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Recommended DC Operating Conditions						
VDDI	Supply voltage		2.375	2.5	2.625	V
Mini-LVDS DC Input Voltage Specification						
VI	DC Input voltage		0	–	2.925	V
Mini-LVDS DC Output Voltage Specification						
VOH	DC output logic High		1.25	1.425	1.6	V
VOL	DC output logic Low		0.9	1.075	1.25	V
Mini-LVDS Differential Voltage Specification						
VOD	Differential output voltage swing		300	–	600	mV
VOCM	Output common mode voltage		1	–	1.4	V
VICM	Input common mode voltage		0.3	–	1.2	V
VID	Input differential voltage		100	–	600	mV

Table 98 • Mini-LVDS AC Specifications

Symbols	Parameters	Conditions	Min	Typ	Max	Units
Mini-LVDS Maximum AC Switching Speed						
Dmax	Maximum data rate (MSIO I/O Bank)	AC loading: 2 pF / 100 Ω differential load	–	–	460	Mbps
Dmax	Maximum data rate (MSIOD I/O Bank)	AC loading: 10 pF / 100 Ω differential load	–	–	480	Mbps
Mini-LVDS Impedance Specification						
Rt	Termination resistance		–	100	–	Ω
Mini-LVDS AC Test Parameters Specifications						
VTrip	Measuring/trip point for data path		–	Cross point	–	V
Rent	Resistance for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	2k	–	Ω
Cent	Capacitive loading for enable path (t_{ZH}, t_{ZL}, t_{HZ}, t_{LZ})		–	5	–	pF

Table 108 • **Input Data Register Propagation Delays**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Measuring Nodes (from, to)*	Speed Grade –1	Units
t_{IBYP}	Bypass Delay of the Input Register	F,G	0.364	ns
t_{ICLKQ}	Clock-to-Q of the Input Register	E,G	0.165	ns
t_{ISUD}	Data Setup Time for the Input Register	A,E	0.369	ns
t_{IHD}	Data Hold Time for the Input Register	A,E	0	ns
t_{ISUE}	Enable Setup Time for the Input Register	B,E	0.475	ns
t_{IHE}	Enable Hold Time for the Input Register	B,E	0	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input Register	D,E	0.475	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D,E	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register (ADn=1)	C,G	0.648	ns
	Asynchronous Preset-to-Q of the Input Register (ADn=0)	C,G	0.606	ns
$t_{IREMALn}$	Asynchronous Load Removal Time for the Input Register	C,E	0	ns
$t_{IRECALn}$	Asynchronous Load Recovery Time for the Input Register	C,E	0.076	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C,C	0.313	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Register	E,E	0.078	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Register	E,E	0.164	ns

8.9.2 Output/Enable Register

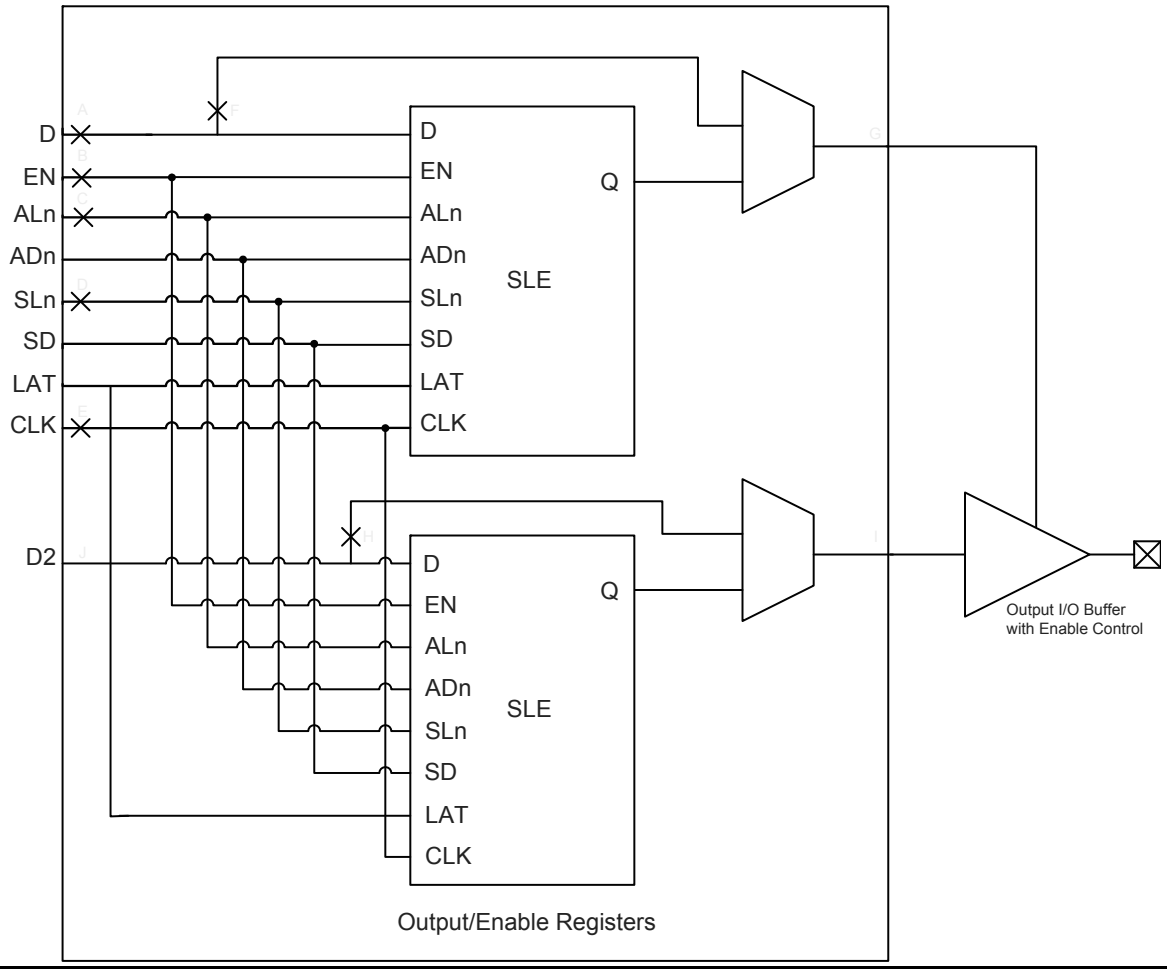

Figure 7 • **Timing Model for Output/Enable Register**

9.2 Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

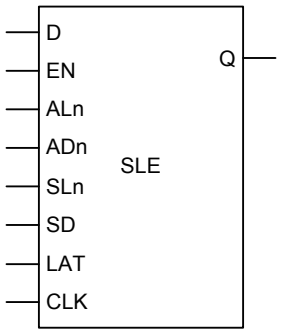

***Figure 14* • Sequential Module**

Figure 15 shows a configuration with SD = 0 (synchronous clear) and ADn = 1 (asynchronous clear) for a flip-flop (LAT = 0).

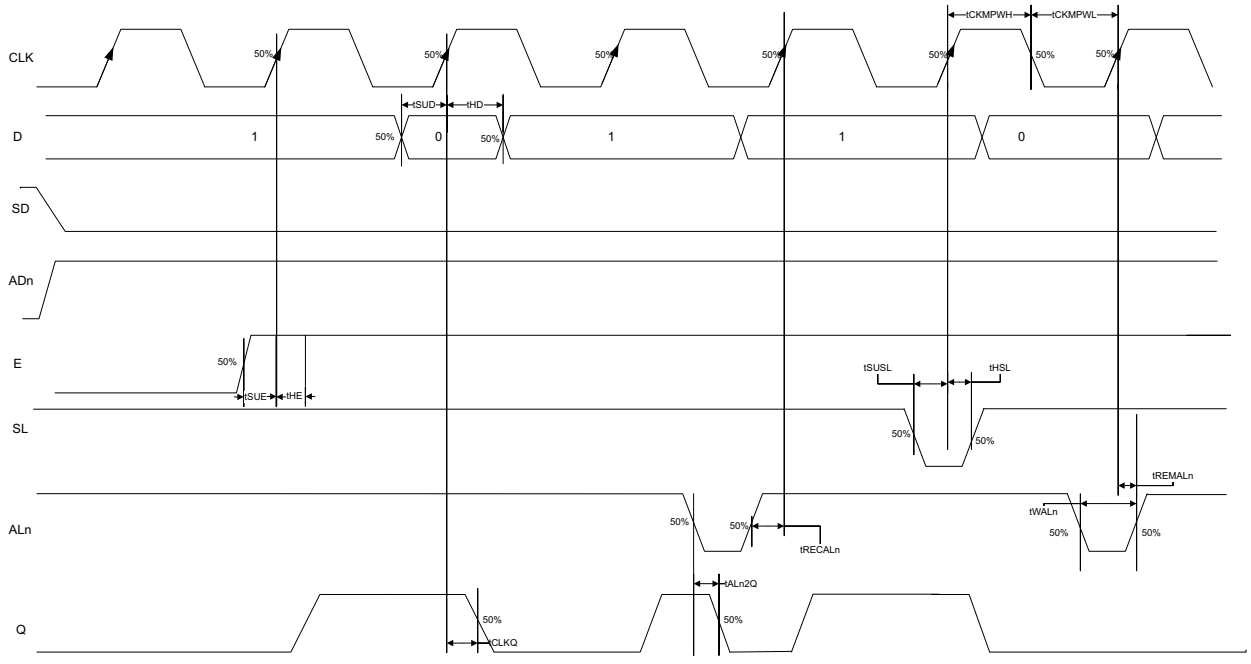

***Figure 15* • Sequential Module Timing Diagram**

9.2.1 Timing Characteristics

Table 113 • **Register Delays**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.112	ns
t_{SUD}	Data Setup Time for the Core Register	0.262	ns
t_{HD}	Data Hold Time for the Core Register	0	ns
t_{SUE}	Enable Setup Time for the Core Register	0.346	ns
t_{HE}	Enable Hold Time for the Core Register	0	ns
t_{SUSL}	Synchronous Load Setup Time for the Core Register	0.346	ns
t_{HSL}	Synchronous Load Hold Time for the Core Register	0	ns
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core Register (ADn=1)	0.49	ns
	Asynchronous Preset-to-Q of the Core Register (ADn=0)	0.466	ns
t_{REMALn}	Asynchronous Load Removal Time for the Core Register	0	ns
t_{RECALn}	Asynchronous Load Recovery Time for the Core Register	0.364	ns
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core Register	0.266	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.065	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.139	ns

10. Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the *UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide* for the positions of various global routing resources.

Table 114 • **M2S090T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.793	0.847	ns
t_{RCKH}	Input High Delay for Global Clock	1.412	1.498	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.086	ns

Table 115 • **M2S025T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.713	0.762	ns
t_{RCKH}	Input High Delay for Global Clock	1.306	1.391	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.085	ns

Table 116 • **M2S010T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.598	0.639	ns
t_{RCKH}	Input High Delay for Global Clock	1.116	1.192	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.076	ns

Table 117 • **M2S005T Device Global Resource**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RCKL}	Input Low Delay for Global Clock	0.736	0.789	ns
t_{RCKH}	Input High Delay for Global Clock	0.927	0.995	ns
t_{RCKSW}	Maximum Skew for Global Clock	–	0.068	ns

Table 119 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2Kx9**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.428	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		
		Min	Max	Units
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register		0.334	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.56	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.345	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns
t_{BLKHD}	Block Select Hold Time	0.223	–	ns
t_{BLK2Q}	Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	1.56	ns
t_{BLKMPW}	Block Select Minimum Pulse Width	0.218	–	ns
t_{RDESU}	Read Enable Setup Time	0.532	–	ns
t_{RDEHD}	Read Enable Hold Time	0.073	–	ns

Table 120 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4Kx4**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		
		Min	Max	Units
$t_{RDPLESU}$	Pipelined Read Enable Setup Time (A_DOUT_EN, B_DOUT_EN)	0.256	–	ns
$t_{RDPLEHD}$	Pipelined Read Enable Hold Time (A_DOUT_EN, B_DOUT_EN)	0.106	–	ns
t_{R2Q}	Asynchronous Reset to Output Propagation Delay	–	1.562	ns
t_{RSTREM}	Asynchronous Reset Removal Time	0.522	–	ns
t_{RSTREC}	Asynchronous Reset Recovery Time	0.005	–	ns
t_{RSTMPW}	Asynchronous Reset Minimum Pulse Width	0.352	–	ns
$t_{PLRSTREM}$	Pipelined Register Asynchronous Reset Removal Time	-0.288	–	ns
$t_{PLRSTREC}$	Pipelined Register Asynchronous Reset Recovery Time	0.338	–	ns
$t_{PLRSTMPW}$	Pipelined Register Asynchronous Reset Minimum Pulse Width	0.33	–	ns
t_{SRSTSU}	Synchronous Reset Setup Time	0.233	–	ns
t_{SRSTHD}	Synchronous Reset Hold Time	0.037	–	ns
t_{WESU}	Write Enable Setup Time	0.473	–	ns
t_{WEHD}	Write Enable Hold Time	0.05	–	ns
Fmax	Maximum Frequency	–	300	MHz

Table 121 • **RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8Kx2**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Clock Period	3.333	–	ns
$t_{CLKMPWH}$	Clock Minimum Pulse Width High	1.5	–	ns
$t_{CLKMPWL}$	Clock Minimum pulse Width Low	1.5	–	ns
t_{PLCY}	Pipelined Clock Period	3.333	–	ns
$t_{PLCLKMPWH}$	Pipelined Clock Minimum Pulse Width High	1.5	–	ns
$t_{PLCLKMPWL}$	Pipelined Clock Minimum pulse Width Low	1.5	–	ns
t_{CLK2Q}	Read Access Time with Pipeline Register	–	0.332	ns
	Read Access Time without Pipeline Register	–	2.346	ns
	Access Time with Feed-Through Write Timing	–	1.56	ns
t_{ADDRSU}	Address Setup Time	0.631	–	ns
t_{ADDRHD}	Address Hold Time	0.282	–	ns
t_{DSU}	Data Setup Time	0.34	–	ns
t_{DHD}	Data Hold Time	0.084	–	ns
t_{BLKSU}	Block Select Setup Time	0.214	–	ns

Table 129 • **uSRAM (RAM512x2) in 512x2 Mode**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V (continued)

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{BLKHD}	Read Block Select Hold Time	-0.671	–	ns
t_{BLK2Q}	Read Block Select to Out Disable Time (when Pipe-Lined Registered is Disabled)	–	2.219	ns
t_{RSTREM}	Read Asynchronous Reset Removal Time (Pipelined Clock)	-0.15	–	ns
	Read Asynchronous Reset Removal Time (Non-Pipelined Clock)	0.047	–	ns
t_{RSTREC}	Read Asynchronous Reset Recovery Time (Pipelined Clock)	0.524	–	ns
	Read Asynchronous Reset Recovery Time (Non-Pipelined Clock)	0.244	–	ns
t_{R2Q}	Read Asynchronous Reset to Output Propagation Delay (With Pipe-Line Register Enabled)	–	0.862	ns
t_{SRSTSU}	Read Synchronous Reset Setup Time	0.279	–	ns
t_{SRSTHD}	Read Synchronous Reset Hold Time	0.062	–	ns
t_{CCY}	Write Clock Period	4	–	ns
$t_{CCLKMPWH}$	Write Clock Minimum Pulse Width High	1.8	–	ns
$t_{CCLKMPWL}$	Write Clock Minimum Pulse Width Low	1.8	–	ns
t_{BLKCSU}	Write Block Setup Time	0.417	–	ns
t_{BLKCHD}	Write Block Hold Time	0.007	–	ns
t_{DINCSU}	Write Input Data setup Time	0.104	–	ns
t_{DINCHD}	Write Input Data hold Time	0.142	–	ns
$t_{ADDRCSU}$	Write Address Setup Time	0.091	–	ns
$t_{ADDRCHD}$	Write Address Hold Time	0.255	–	ns
t_{WECSU}	Write Enable Setup Time	0.41	–	ns
t_{WECHD}	Write Enable Hold Time	-0.027	–	ns
Fmax	Maximum Frequency	–	250	MHz

Table 130 • **uSRAM (RAM1024x1) in 1024x1 Mode**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Speed Grade –1		Units
		Min	Max	
t_{CY}	Read Clock Period	4	–	ns
$t_{CLKMPWH}$	Read Clock Minimum Pulse Width High	1.8		ns
$t_{CLKMPWL}$	Read Clock Minimum pulse Width Low	1.8	–	ns
t_{PLCY}	Read Pipe-line clock period	4	–	ns
$t_{PLCLKMPWH}$	Read Pipe-line clock Minimum Pulse Width High	1.8	–	ns
$t_{PLCLKMPWL}$	Read Pipe-line clock Minimum Pulse Width Low	1.8	–	ns

12. Embedded NVM (eNVM) Characteristics

Table 131 • **eNVM Read Performance**
Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T_J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
$F_{MAXREAD}$	eNVM Maximum Read Frequency	25	25	25	25	25	25	MHz

Table 132 • **eNVM Page Programming**
Worst-Case Conditions: VDD = 1.14 V, VPPNVM = VPP = 2.375 V

Symbol	Description	Operating Temperature Range						Unit
T_J	Junction Temperature Range	-55°C to 125°C		-40°C to 100°C		0°C to 85°C		°C
Speed grade		-1	Std	-1	Std	-1	Std	–
$t_{PAGEPGM}$	eNVM Page Programming Time	40	40	40	40	40	40	ms

13. Crystal Oscillator

Table 133 describes the electrical characteristics of the crystal oscillator in the IGLOO2 FPGA and SmartFusion2 SoC FPGAs.

Table 133 • **Electrical Characteristics of the Crystal Oscillator – High Gain Mode (20 MHz)**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FXTAL	Operating frequency	–	20	–	MHz
ACCXTAL	Accuracy	–	–	0.006	%
CYCXTAL	Output duty cycle	–	49-51	47-53	%
JITPERXTAL	Output Period Jitter (peak to peak)	–	200	300	ps
JITCYCXTAL	Output Cycle to Cycle Jitter (peak to peak)	–	200	550	ps
IDYNXTAL	Operating current	–	1.5	–	mA
VIHXTAL	Input logic level High	0.9 × VPP	–	–	V
VILXTAL	Input logic level Low	–	–	0.1 × VPP	V
SUXTAL	Startup time (with regard to stable oscillator output)	–	–	1	ms

14. On-Chip Oscillator

Table 136 and Table 137 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 FPGAs and SmartFusion2 SoC FPGAs.

Table 136 • **Electrical Characteristics of the 50 MHz RC Oscillator**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F50RC	Operating frequency	–	–	50	–	MHz
ACC50RC	Accuracy	–	–	1	8	%
CYC50RC	Output duty cycle	–	–	49–51	46–54	%
JIT50RC	Output jitter (peak to peak)	Period Jitter		200	500	ps
		Cycle-to-Cycle Jitter		320	900	ps
IDYN50RC	Operating current	–	–	8.5	–	mA

Table 137 • **Electrical Characteristics of the 1 MHz RC Oscillator**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Condition	Min	Typ	Max	Units
F1RC	Operating frequency	–	–	1	–	MHz
ACC1RC	Accuracy	–	–	1	6	%
CYC1RC	Output duty cycle	–	–	49–51	46.5–53.5	%
JIT1RC	Output jitter (peak to peak)	Period Jitter	–	10	36	ps
		Cycle-to-Cycle Jitter	–	10	50	ps
IDYN1RC	Operating current	–	–	0.1	–	mA
SU1RC	Startup time	–	–	–	20	µs

15. Clock Conditioning Circuits (CCC)

Table 138 • **IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Conditions	Min	Typ	Max	Units	Notes
Clock conditioning circuitry input frequency f_{IN_CCC}	All CCC	1	–	200	MHz	–
	32 kHz Capable CCC	0.032	–	200	MHz	–
Clock conditioning circuitry output frequency f_{OUT_CCC}	–	0.078	–	400	MHz	1
PLL VCO frequency	–	500	–	1000	MHz	2
Delay increments in programmable delay blocks	–	–	75	100	ps	–
Number of programmable values in each programmable delay block	–	–	–	64	–	–
Acquisition time	–	–	70	100	µs	–

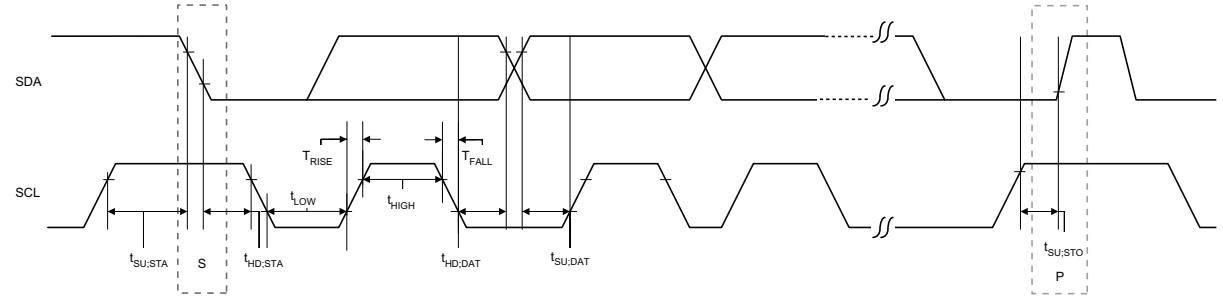

Figure 16 • **I^2C Timing Parameter Definition**

24.3 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 17 on page 102.

Table 159 • **SPI Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Symbol	Description	All Devices/Speed Grades			Unit	Notes
		Min	Typ	Max		
sp1	**SPI_[0|1]_CLK minimum period**					
	SPI_[0|1]_CLK = PCLK/2	12	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	48.2	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	0.1	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	0.19	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	0.39	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	0.77	–	–	µs	–
sp2	**SPI_[0|1]_CLK minimum pulse width high**					
	SPI_[0|1]_CLK = PCLK/2	6	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/4	12.05	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/8	24.1	–	–	ns	–
	SPI_[0|1]_CLK = PCLK/16	0.05	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/32	0.095	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/64	0.195	–	–	µs	–
	SPI_[0|1]_CLK = PCLK/128	0.385	–	–	µs	–

Notes:

1. *For specific Rise/Fall Times board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/products/fpga-soc/design-resources/ibis-models.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the UG0331: SmartFusion2 Microcontroller Subsystem User Guide.*

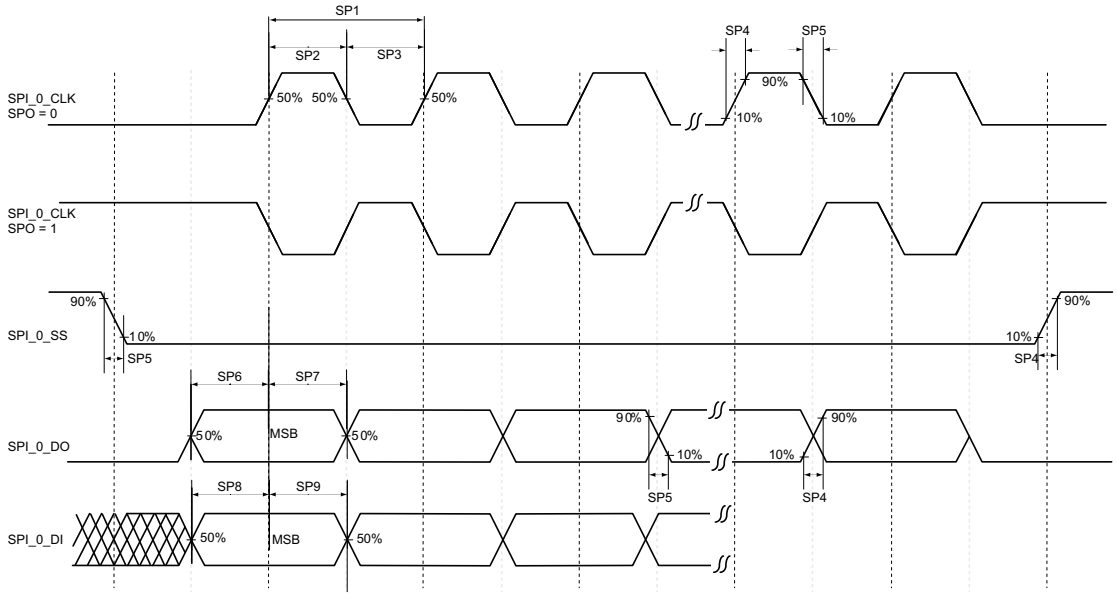

***Figure 17* • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

25. CAN Controller Characteristics

***Table 160* • CAN Controller Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units	Notes
FCANREFCLK	Internally Sourced CAN Reference Clock Frequency	–	–	128	MHz	*
BAUDCAN	CAN Performance Baud Rate	0.05	–	1	Mbps	–
Note: PCLK to CAN controller must be a multiple of 8 MHz.						

26. USB Characteristics

***Table 161* • USB Characteristics**
Worst-Case Automotive Grade 2 Conditions: T_J = 125°C, VDD = 1.14 V

Parameter	Description	Min	Typ	Max	Units
FUSBREFCLK	Internally Sourced USB Reference Clock Frequency	–	–	133	MHz
TUSBCLK	USB Clock Period	–	–	16.66	ns
TUSBPD	Clock to USB Data Propagation Delay	–	–	9.0	ns
TUSBSU	Setup Time for USB Data	–	–	6.0	ns
TUSBHD	Hold Time for USB Data	0	–	–	ns

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