What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
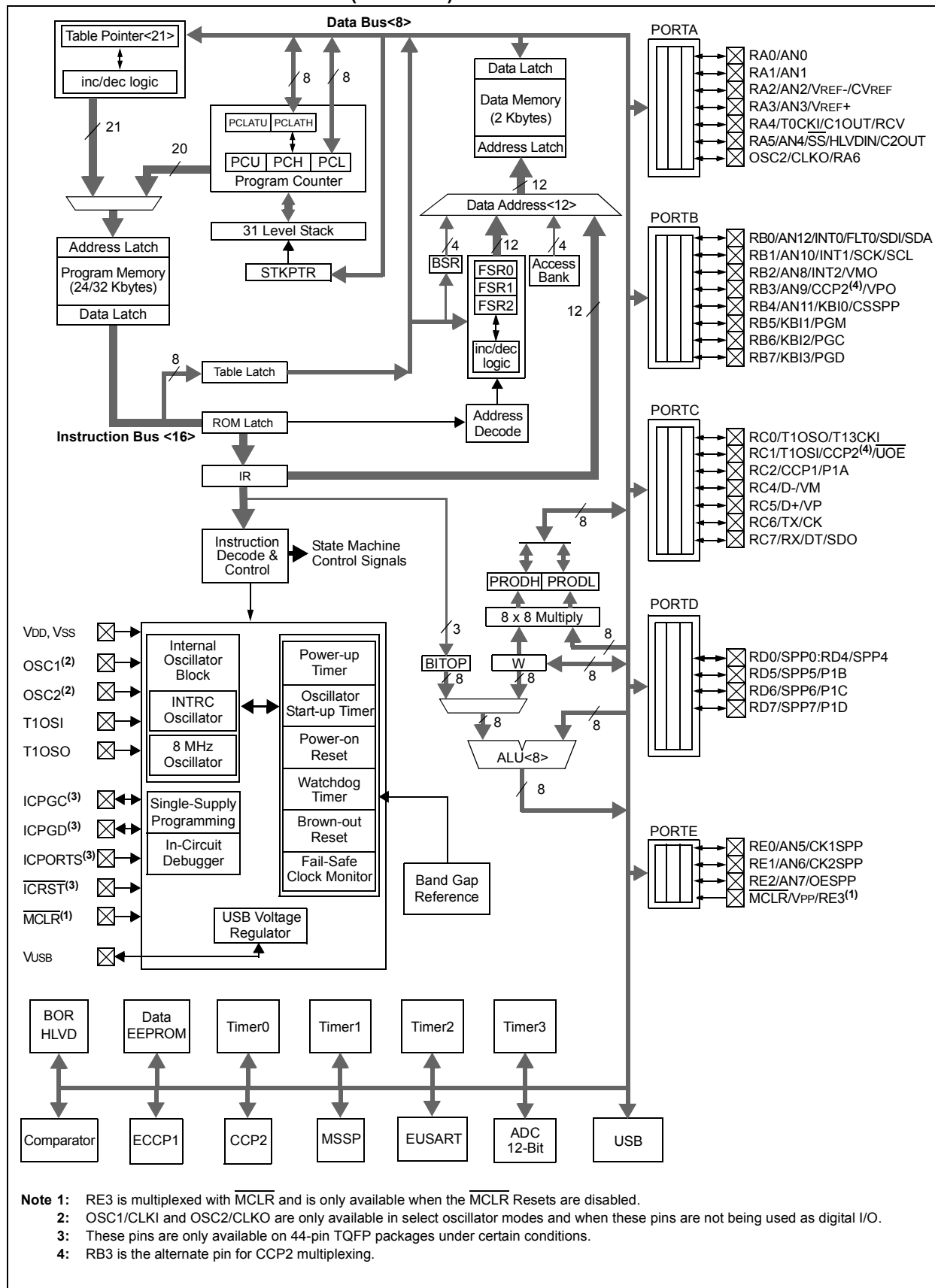
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2553-i-sp

FIGURE 1-2: PIC18F4458/4553(40/44-PIN) BLOCK DIAGRAM

Note 1: RE3 is multiplexed with $\overline{MCLR}$ and is only available when the $\overline{MCLR}$ Resets are disabled.
   2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O.
   3: These pins are only available on 44-pin TQFP packages under certain conditions.
   4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: **PIC18F2458/2553 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number SPDIP, SOIC	Pin Type	Buffer Type	Description
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
    2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

PIC18F2458/2553/4458/4553

TABLE 1-3: **PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/V$_{REF}$-/ CV$_{REF}$	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
V$_{REF}$-				I	Analog	A/D reference voltage (low) input.
CV$_{REF}$				O	Analog	Analog comparator reference output.
RA3/AN3/V$_{REF}$+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
V$_{REF}$+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/ RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3:   PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RB0/AN12/INT0/ FLT0/SDI/SDA	33	9	8			PORTB is a bidirectional I/O port. PORTB can be soft-ware programmed for internal weak pull-ups on all inputs.
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog input 12.
INT0				I	ST	External interrupt 0.
FLT0				I	ST	Enhanced PWM Fault input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/ SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog input 10.
INT1				I	ST	External interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog input 8.
INT2				I	ST	External interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2[1]				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
          ST = Schmitt Trigger input with CMOS levels   I   = Input
          O = Output   P   = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
      2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
      3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

PIC18F2458/2553/4458/4553

TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RE0/AN5/CK1SPP RE0 AN5 CK1SPP	8	25	25	 I/O I O	 ST Analog —	PORTE is a bidirectional I/O port. Digital I/O. Analog input 5. SPP clock 1 output.
RE1/AN6/CK2SPP RE1 AN6 CK2SPP	9	26	26	 I/O I O	 ST Analog —	 Digital I/O. Analog input 6. SPP clock 2 output.
RE2/AN7/OESPP RE2 AN7 OESPP	10	27	27	 I/O I O	 ST Analog —	 Digital I/O. Analog input 7. SPP output enable output.
RE3	—	—	—	—	—	See $\overline{\text{MCLR}}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	 O P	 — —	Internal USB transceiver power supply. When the internal USB regulator is enabled, VUSB is the regulator output. When the internal USB regulator is disabled, VUSB is the power input for the USB transceiver.
NC/ICCK/ICPGC[3] ICCK ICPGC	—	—	12	 I/O I/O	 ST ST	No Connect or dedicated ICD/ICSP™ port clock. In-Circuit Debugger clock. ICSP programming clock.
NC/ICDT/ICPGD[3] ICDT ICPGD	—	—	13	 I/O I/O	 ST ST	No Connect or dedicated ICD/ICSP port clock. In-Circuit Debugger data. ICSP programming data.
NC/$\overline{\text{ICRST}}$/ICVPP[3] ICRST ICVPP	—	—	33	 I P	 — —	No Connect or dedicated ICD/ICSP port Reset. Master Clear (Reset) input. Programming voltage input.
NC/ICPORTS[3] ICPORTS	—	—	34	P	—	No Connect or 28-pin device emulation. Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
    2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
    3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{\text{DEBUG}}$ Configuration bit is cleared.

2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40-pin and 44-pin devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6   **Unimplemented:** Read as '0'

bit 5-2   **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)[1,2]
0110 = Channel 6 (AN6)[1,2]
0111 = Channel 7 (AN7)[1,2]
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented[2]
1110 = Unimplemented[2]
1111 = Unimplemented[2]

bit 1   **GO/$\overline{DONE}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0   **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
    2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 2-2: **ADCON1: A/D CONTROL REGISTER 1**

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W[1]	R/W[1]	R/W[1]
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF}- source)

1 = V_{REF}- (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF}+ source)

1 = V_{REF}+ (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7[2]	AN6[2]	AN5[2]	AN4	AN3	AN2	AN1	AN0
0000[1]	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111[1]	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input   D = Digital I/O

Note 1: The Reset value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are available only on 40-pin and 44-pin devices.

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7   **ADFM:** A/D Result Format Select bit

1 = Right justified
0 = Left justified

bit 6   **Unimplemented:** Read as '0'

bit 5-3   **ACQT2:ACQT0:** A/D Acquisition Time Select bits

111 = 20 T_{AD}
110 = 16 T_{AD}
101 = 12 T_{AD}
100 = 8 T_{AD}
011 = 6 T_{AD}
010 = 4 T_{AD}
001 = 2 T_{AD}
000 = 0 T_{AD}[1]

bit 2-0   **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = F_{RC} (clock derived from A/D RC oscillator)[1]
110 = F_{OSC}/64
101 = F_{OSC}/16
100 = F_{OSC}/4
011 = F_{RC} (clock derived from A/D RC oscillator)[1]
010 = F_{OSC}/32
001 = F_{OSC}/8
000 = F_{OSC}/2

Note 1: If the A/D F_{RC} clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the T_{AD} time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits ACQT2:ACQT0 are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1:	When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
2:	Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.
3:	The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG3:PCFG0 bits in ADCON1 are reset.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT2:ACQT0 bits are set to '010', and selecting a 4 T$_{AD}$ acquisition time before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers).

After the A/D conversion is completed or aborted, a 2 T$_{CY}$ wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D. Code should wait at least 2 μs after enabling the A/D before beginning an acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

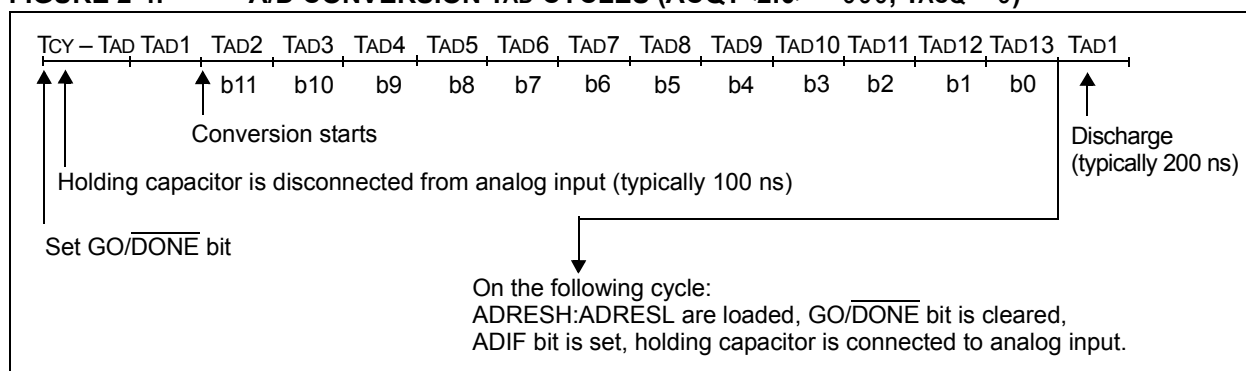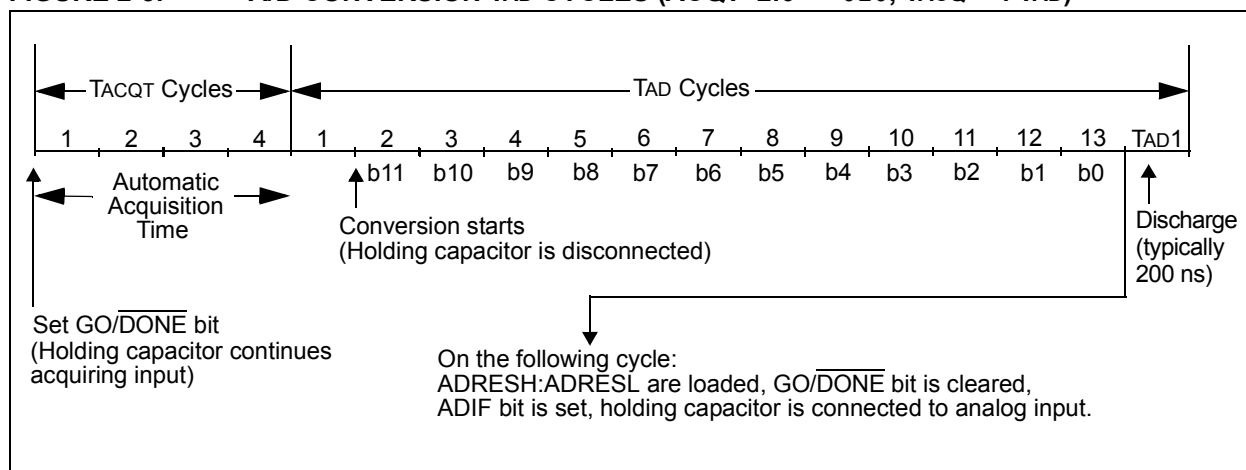**FIGURE 2-4:** A/D CONVERSION T$_{AD}$ CYCLES (ACQT<2:0> = 000, TACQ = 0)

FIGURE 2-5: A/D CONVERSION T$_{AD}$ CYCLES (ACQT<2:0> = 010, TACQ = 4 T$_{AD}$)

PIC18F2458/2553/4458/4553

2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (firmware must move ADRESH:ADRESL to

the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	[4]
PIR1	SPPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	[4]
PIE1	SPPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	[4]
IPR1	SPPIP[1]	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	[4]
PIR2	OSCFIF	CMIF	USBIF	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	[4]
PIE2	OSCFIE	CMIE	USBIE	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	[4]
IPR2	OSCFIP	CMIP	USBIP	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	[4]
ADRESH	A/D Result Register High Byte								[4]
ADRESL	A/D Result Register Low Byte								[4]
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	21
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	22
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	23
PORTA	—	RA6[2]	RA5	RA4	RA3	RA2	RA1	RA0	[4]
TRISA	—	TRISA6[2]	PORTA Data Direction Control Register						[4]
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	[4]
TRISB	PORTB Data Direction Control Register								[4]
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								[4]
PORTE[1]	RDPU	—	—	—	RE3[3]	RE2[1]	RE1[1]	RE0[1]	[4]
TRISE[1]	—	—	—	—	—	TRISE2	TRISE1	TRISE0	[4]
LATE[1]	—	—	—	—	—	PORTE Data Latch Register			[4]

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers and/or bits are not implemented on 28-pin devices and are read as '0'.

2: RA6 and its associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.

3: RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

4: For these Reset values, see the *"PIC18F2455/2550/4455/4550 Data Sheet"*.

3.0 SPECIAL FEATURES OF THE CPU

> **Note:** For additional details on the Configuration bits, refer to the *"PIC18F2455/2550/4455/4550 Data Sheet"*, **Section 25.1 "Configuration Bits"**. Device ID information presented in this section is for PIC18F2458/2553/4458/4553 only.

PIC18F2458/2553/4458/4553 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

• Device ID Registers

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers, and can be read by firmware using table reads.

TABLE 3-1: DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx[1]
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx[1]

Legend: x = unknown, u = unchanged

Note 1: See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

PIC18F2458/2553/4458/4553

REGISTER 3-1:   **DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2458/2553/4458/4553 DEVICES**

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-5   **DEV2:DEV0:** Device ID bits

             See Register 3-2 for a complete listing.

bit 4-0   **REV3:REV0:** Revision ID bits

             These bits are used to indicate the device revision.

REGISTER 3-2:   **DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2458/2553/4458/4553 DEVICES**

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

Legend:		
R = Read-only bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state

bit 7-0   **DEV10:DEV3:** Device ID bits

DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)	Device
0010 1010	011	PIC18F2458
0010 1010	010	PIC18F2553
0010 1010	001	PIC18F4458
0010 1010	000	PIC18F4553

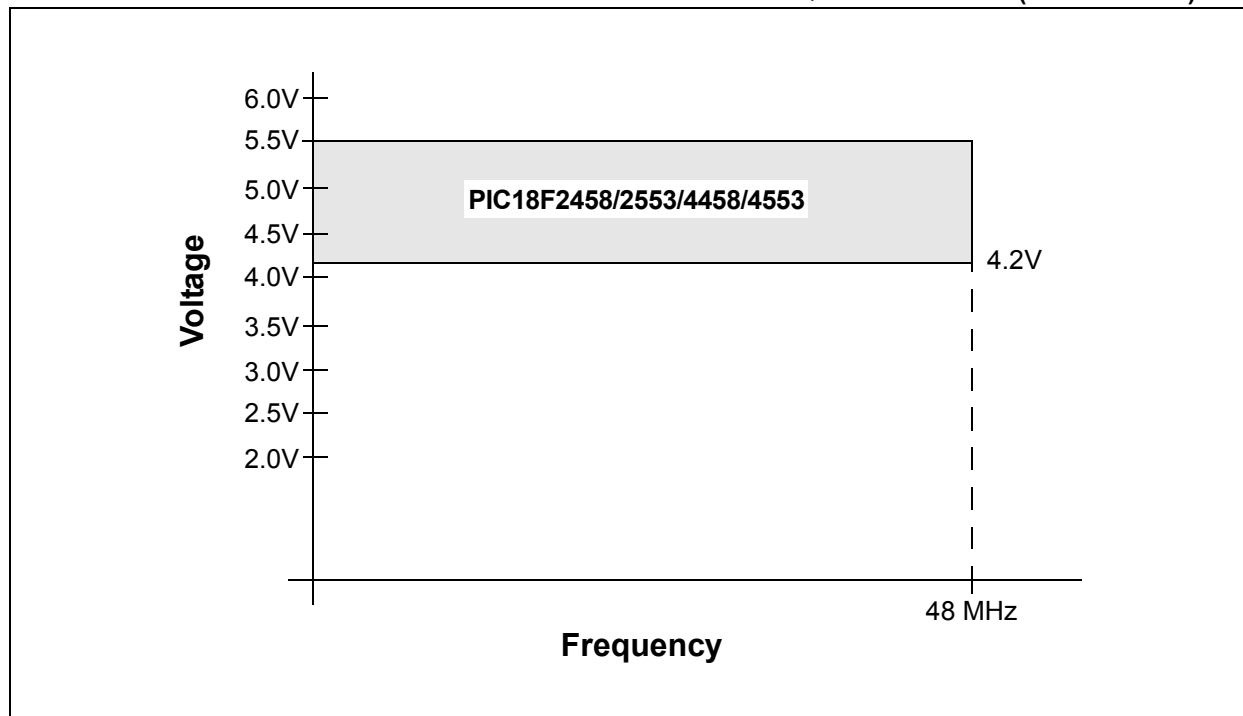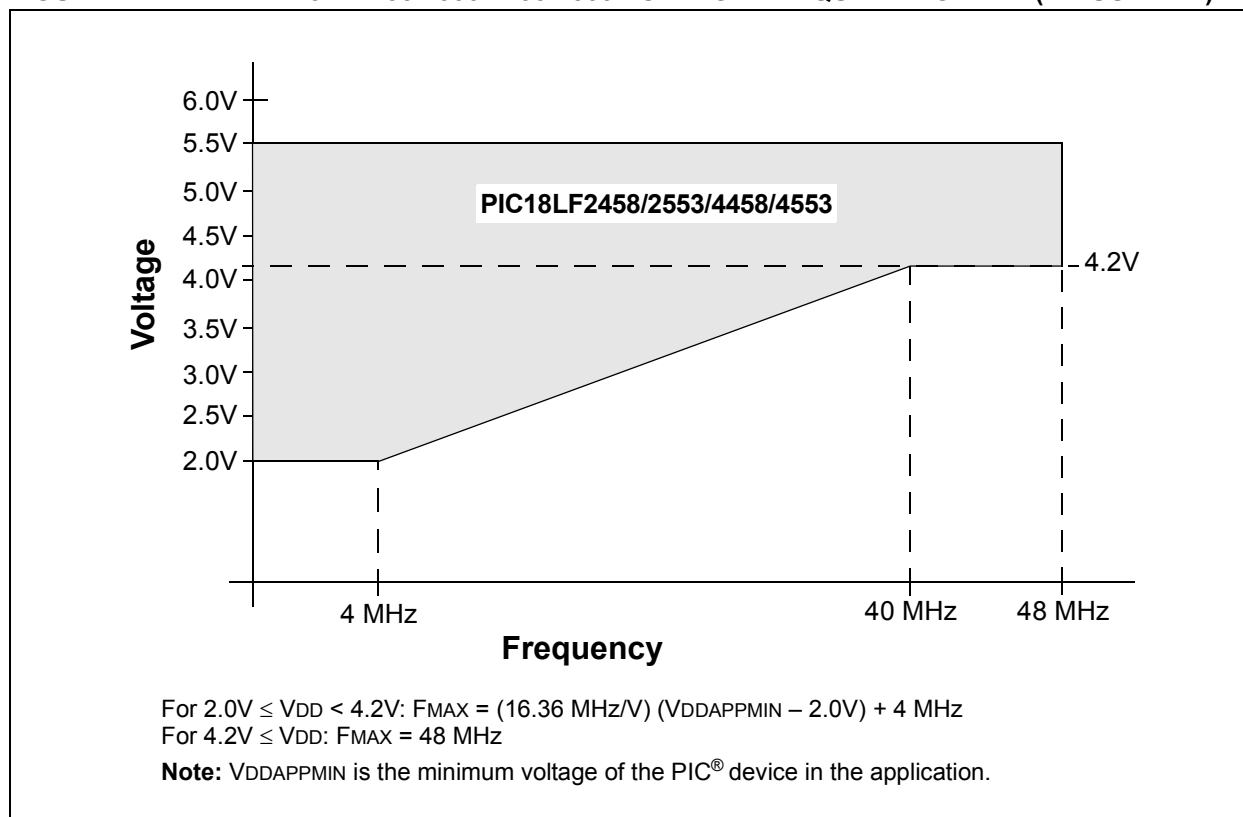**FIGURE 4-1:**   **PIC18F2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**

FIGURE 4-2:   **PIC18LF2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**

For $2.0V \leq V_{DD} < 4.2V$: $F_{MAX} = (16.36\ MHz/V)\ (V_{DDAPPMIN} - 2.0V) + 4\ MHz$
For $4.2V \leq V_{DD}$: $F_{MAX} = 48\ MHz$

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PIC® device in the application.

PIC18F2458/2553/4458/4553

FIGURE 4-3: **A/D CONVERSION TIMING**

Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed.

2: This is a minimal RC delay (typically 100 ns), which also disconnects the holding capacitor from the analog input.
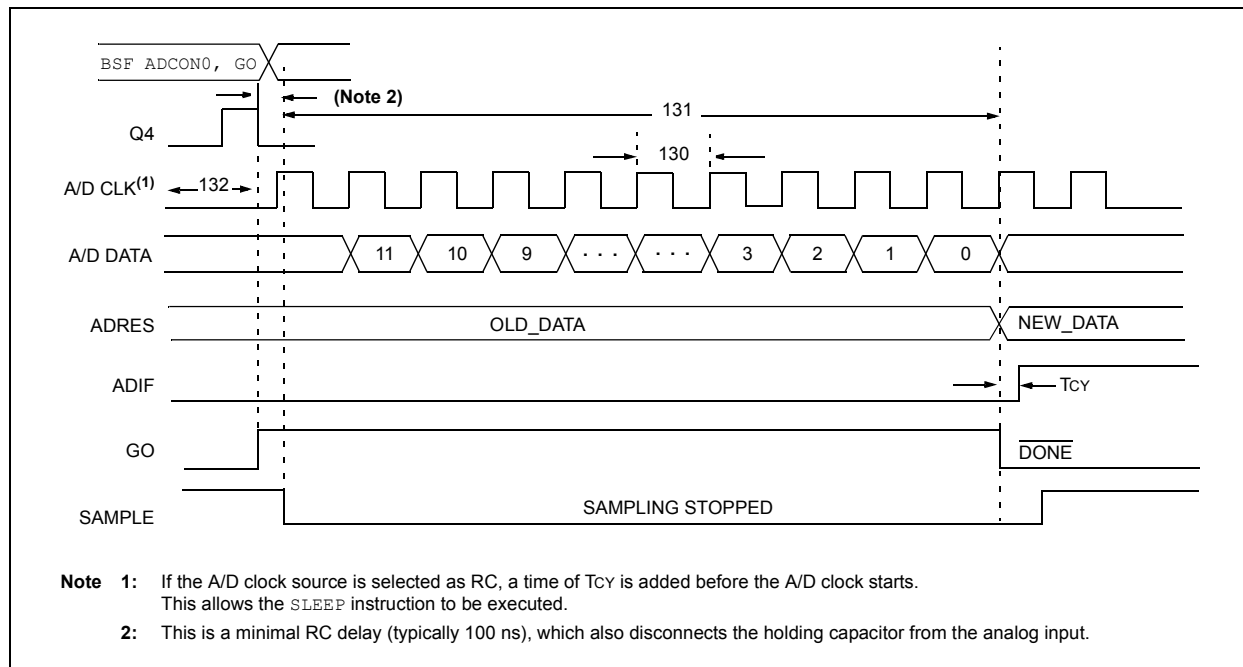
TABLE 4-2: **A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	T_{AD}	A/D Clock Period	PIC18**F**XXXX	0.8	12.5[1]	µs	T_{OSC} based, $V_{REF} \geq 3.0$V
			PIC18**LF**XXXX	1.4	25.0[1]	µs	V_{DD} = 3.0V; T_{OSC} based, V_{REF} full range
			PIC18**F**XXXX	—	1	µs	A/D RC mode
			PIC18**LF**XXXX	—	3	µs	V_{DD} = 3.0V; A/D RC mode
131	T_{CNV}	Conversion Time (not including acquisition time)[2]		13	14	T_{AD}	
132	T_{ACQ}	Acquisition Time[3]		1.4	—	µs	
135	T_{SWC}	Switching Time from Convert → Sample		—	**(Note 4)**		
137	T_{DIS}	Discharge Time		0.2	—	µs	

Note 1: The time of the A/D clock period is dependent on the device frequency and the T_{AD} clock divider.

2: ADRES registers may be read on the following T_{CY} cycle.

3: The time for the holding capacitor to acquire the "New" input voltage when the voltage changes full scale after the conversion (V_{DD} to V_{SS} or V_{SS} to V_{DD}). The source impedance (R_S) on the input channels is 50Ω.

4: On the following cycle of the device clock.

5.0   PACKAGING INFORMATION

For packaging information, see the *"PIC18F2455/ 2550/4455/4550 Data Sheet"* (DS39632).

PIC18F2458/2553/4458/4553

APPENDIX C: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN716, "Migrating Designs from PIC16C74A/74B to PIC18C442"*. The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX D: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in *AN726, "PIC17CXXX to PIC18CXXX Migration"*.

This Application Note is available as Literature Number DS00726.

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PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC18F2458/2553[1], PIC18F4458/4553[1], PIC18F2458/2553T[2], PIC18F4458/4553T[2]; V$_{DD}$ range 4.2V to 5.5V PIC18LF2458/2553[1], PIC18LF4458/4553[1], PIC18LF2458/2553T[2], PIC18LF4458/4553T[2]; V$_{DD}$ range 2.0V to 5.5V
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny PDIP P = PDIP ML = QFN
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)

Examples:

a)   PIC18LF4553-I/P 301 = Industrial temp., PDIP package, Extended V$_{DD}$ limits, QTP pattern #301.

b)   PIC18LF2458-I/SO = Industrial temp., SOIC package, Extended V$_{DD}$ limits.

c)   PIC18F4458-I/P = Industrial temp., PDIP package, normal V$_{DD}$ limits.

Note 1:   F   =   Standard Voltage Range
             LF   =   Wide Voltage Range
    2:   T   =   In tape and reel TQFP packages only.