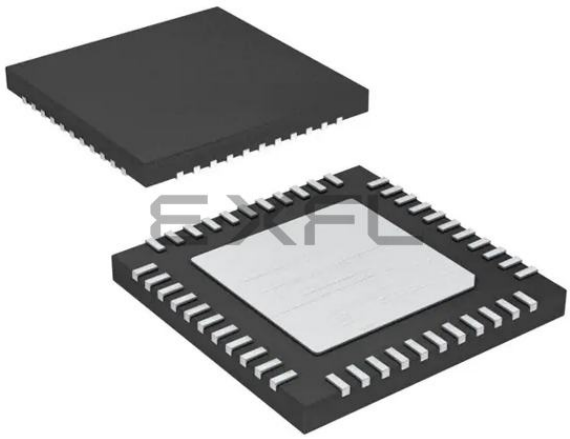

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## What is "Embedded - Microcontrollers"?

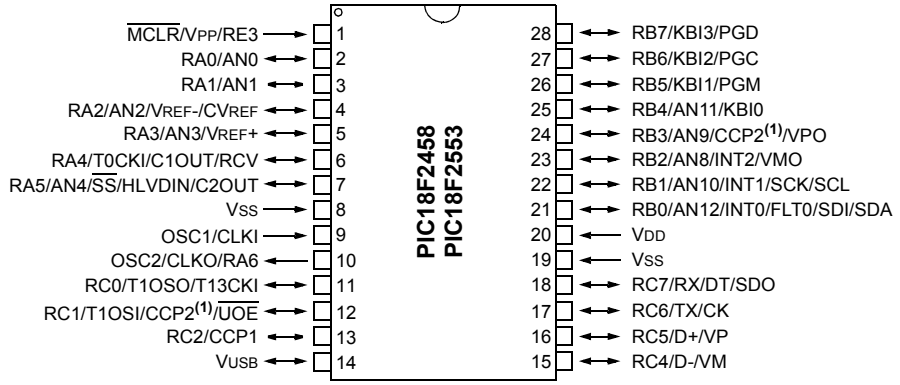
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

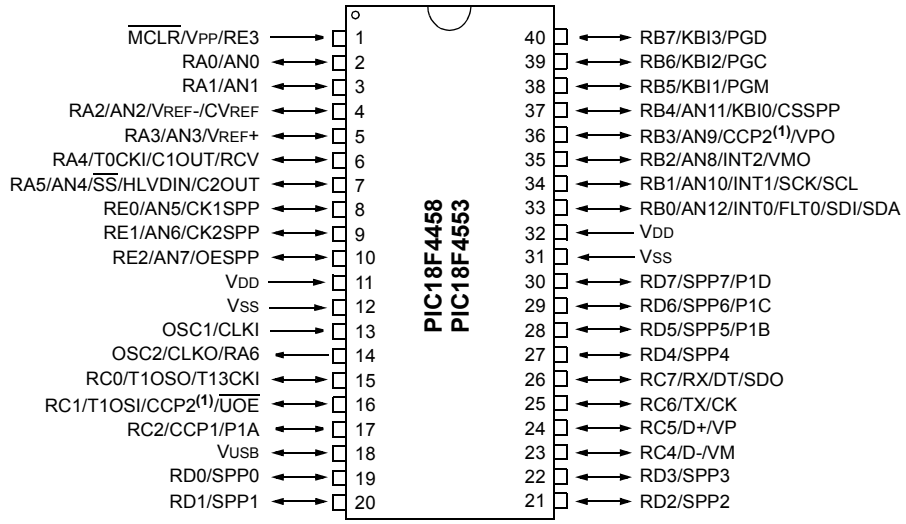
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 48MHz |
| Connectivity | I²C, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 24KB (12K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | 256 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.2V ~ 5.5V |
| Data Converters | A/D 13x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic18f4458-i-ml |

## Pin Diagrams

### 28-Pin SPDIP, SOIC




### 40-Pin PDIP




**Note 1:** RB3 is the alternate pin for CCP2 multiplexing.

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2458
- PIC18F2553
- PIC18F4458
- PIC18F4553

| | |
|---|---|
| **Note:** | This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F2455/2550/4455/4550 devices. For information on the features and specifications shared by the PIC18F2458/2553/4458/4553 and PIC18F2455/2550/4455/4550 devices, see the *"PIC18F2455/2550/4455/4550 Data Sheet"* (DS39632). |

The PIC18F4553 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F4553 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F4553 family implements a 12-bit A/D Converter. The A/D Converter incorporates programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

### 1.2 Details on Individual Family Members

The PIC18F2458/2553/4458/4553 devices are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

1. Flash program memory (24 Kbytes for PIC18FX458 devices, 32 Kbytes for PIC18FX553).
2. A/D channels (10 for 28-pin devices, 13 for 40-pin and 44-pin devices).
3. I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40-pin and 44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40-pin and 44-pin devices have one standard CCP module and one ECCP module).
5. Streaming Parallel Port (present only on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F4553 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18**F**2458), accommodate an operating $V_{DD}$ range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18**LF**2458), function over an extended $V_{DD}$ range of 2.0V to 5.5V.

**TABLE 1-1: DEVICE FEATURES**

| Features | PIC18F2458 | PIC18F2553 | PIC18F4458 | PIC18F4553 |
|---|---|---|---|---|
| Operating Frequency | DC – 48 MHz | DC – 48 MHz | DC – 48 MHz | DC – 48 MHz |
| Program Memory (Bytes) | 24576 | 32768 | 24576 | 32768 |
| Program Memory (Instructions) | 12288 | 16384 | 12288 | 16384 |
| Data Memory (Bytes) | 2048 | 2048 | 2048 | 2048 |
| Data EEPROM Memory (Bytes) | 256 | 256 | 256 | 256 |
| Interrupt Sources | 19 | 19 | 20 | 20 |
| I/O Ports | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, D, E | Ports A, B, C, D, E |
| Timers | 4 | 4 | 4 | 4 |
| Capture/Compare/PWM Modules | 2 | 2 | 1 | 1 |
| Enhanced Capture/ Compare/PWM Modules | 0 | 0 | 1 | 1 |
| Serial Communications | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART | MSSP, Enhanced USART |
| Universal Serial Bus (USB) Module | 1 | 1 | 1 | 1 |
| Streaming Parallel Port (SPP) | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Converter Module | 10 Input Channels | 10 Input Channels | 13 Input Channels | 13 Input Channels |
| Comparators | 2 | 2 | 2 | 2 |
| Resets (and Delays) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) | POR, BOR, WDT, RESET Instruction, Stack Full, Stack Underflow, MCLR (optional), (PWRT, OST) |
| Programmable High/ Low-Voltage Detect | Yes | Yes | Yes | Yes |
| Programmable Brown-out Reset | Yes | Yes | Yes | Yes |
| Instruction Set | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled | 75 Instructions; 83 with Extended Instruction Set Enabled |
| Packages | 28-Pin SPDIP 28-Pin SOIC | 28-Pin SPDIP 28-Pin SOIC | 40-Pin PDIP 44-Pin QFN 44-Pin TQFP | 40-Pin PDIP 44-Pin QFN 44-Pin TQFP |
| Corresponding Devices with 10-Bit A/D | PIC18F2455 | PIC18F2550 | PIC18F4455 | PIC18F4550 |

**TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | SPDIP, SOIC | | | |
| | | | | PORTA is a bidirectional I/O port. |
| RA0/AN0 | 2 | | | |
| RA0 | | I/O | TTL | Digital I/O. |
| AN0 | | I | Analog | Analog input 0. |
| RA1/AN1 | 3 | | | |
| RA1 | | I/O | TTL | Digital I/O. |
| AN1 | | I | Analog | Analog input 1. |
| RA2/AN2/VREF-/CVREF | 4 | | | |
| RA2 | | I/O | TTL | Digital I/O. |
| AN2 | | I | Analog | Analog input 2. |
| VREF- | | I | Analog | A/D reference voltage (low) input. |
| CVREF | | O | Analog | Analog comparator reference output. |
| RA3/AN3/VREF+ | 5 | | | |
| RA3 | | I/O | TTL | Digital I/O. |
| AN3 | | I | Analog | Analog input 3. |
| VREF+ | | I | Analog | A/D reference voltage (high) input. |
| RA4/T0CKI/C1OUT/RCV | 6 | | | |
| RA4 | | I/O | ST | Digital I/O. |
| T0CKI | | I | ST | Timer0 external clock input. |
| C1OUT | | O | — | Comparator 1 output. |
| RCV | | I | TTL | External USB transceiver RCV input. |
| RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT | 7 | | | |
| RA5 | | I/O | TTL | Digital I/O. |
| AN4 | | I | Analog | Analog input 4. |
| $\overline{SS}$ | | I | TTL | SPI slave select input. |
| HLVDIN | | I | Analog | High/Low-Voltage Detect input. |
| C2OUT | | O | — | Comparator 2 output. |
| RA6 | — | — | — | See the OSC2/CLKO/RA6 pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

**TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | Pin Type | Buffer Type | Description |
|---|---|---|---|---|
| | SPDIP, SOIC | | | |
| | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/AN12/INT0/FLT0/ SDI/SDA | 21 | | | |
| RB0 | | I/O | TTL | Digital I/O. |
| AN12 | | I | Analog | Analog input 12. |
| INT0 | | I | ST | External interrupt 0. |
| FLT0 | | I | ST | PWM Fault input (CCP1 module). |
| SDI | | I | ST | SPI data in. |
| SDA | | I/O | ST | $I^2C$™ data I/O. |
| RB1/AN10/INT1/SCK/ SCL | 22 | | | |
| RB1 | | I/O | TTL | Digital I/O. |
| AN10 | | I | Analog | Analog input 10. |
| INT1 | | I | ST | External interrupt 1. |
| SCK | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | I/O | ST | Synchronous serial clock input/output for $I^2C$ mode. |
| RB2/AN8/INT2/VMO | 23 | | | |
| RB2 | | I/O | TTL | Digital I/O. |
| AN8 | | I | Analog | Analog input 8. |
| INT2 | | I | ST | External interrupt 2. |
| VMO | | O | — | External USB transceiver VMO output. |
| RB3/AN9/CCP2/VPO | 24 | | | |
| RB3 | | I/O | TTL | Digital I/O. |
| AN9 | | I | Analog | Analog input 9. |
| CCP2(1) | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| VPO | | O | — | External USB transceiver VPO output. |
| RB4/AN11/KBI0 | 25 | | | |
| RB4 | | I/O | TTL | Digital I/O. |
| AN11 | | I | Analog | Analog input 11. |
| KBI0 | | I | TTL | Interrupt-on-change pin. |
| RB5/KBI1/PGM | 26 | | | |
| RB5 | | I/O | TTL | Digital I/O. |
| KBI1 | | I | TTL | Interrupt-on-change pin. |
| PGM | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 27 | | | |
| RB6 | | I/O | TTL | Digital I/O. |
| KBI2 | | I | TTL | Interrupt-on-change pin. |
| PGC | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 28 | | | |
| RB7 | | I/O | TTL | Digital I/O. |
| KBI3 | | I | TTL | Interrupt-on-change pin. |
| PGD | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. |
| RB0/AN12/INT0/FLT0/SDI/SDA | 33 | 9 | 8 | | | |
| RB0 | | | | I/O | TTL | Digital I/O. |
| AN12 | | | | I | Analog | Analog input 12. |
| INT0 | | | | I | ST | External interrupt 0. |
| FLT0 | | | | I | ST | Enhanced PWM Fault input (ECCP1 module). |
| SDI | | | | I | ST | SPI data in. |
| SDA | | | | I/O | ST | $I^2C$™ data I/O. |
| RB1/AN10/INT1/SCK/SCL | 34 | 10 | 9 | | | |
| RB1 | | | | I/O | TTL | Digital I/O. |
| AN10 | | | | I | Analog | Analog input 10. |
| INT1 | | | | I | ST | External interrupt 1. |
| SCK | | | | I/O | ST | Synchronous serial clock input/output for SPI mode. |
| SCL | | | | I/O | ST | Synchronous serial clock input/output for $I^2C$ mode. |
| RB2/AN8/INT2/VMO | 35 | 11 | 10 | | | |
| RB2 | | | | I/O | TTL | Digital I/O. |
| AN8 | | | | I | Analog | Analog input 8. |
| INT2 | | | | I | ST | External interrupt 2. |
| VMO | | | | O | — | External USB transceiver VMO output. |
| RB3/AN9/CCP2/VPO | 36 | 12 | 11 | | | |
| RB3 | | | | I/O | TTL | Digital I/O. |
| AN9 | | | | I | Analog | Analog input 9. |
| CCP2(1) | | | | I/O | ST | Capture 2 input/Compare 2 output/PWM 2 output. |
| VPO | | | | O | — | External USB transceiver VPO output. |
| RB4/AN11/KBI0/CSSPP | 37 | 14 | 14 | | | |
| RB4 | | | | I/O | TTL | Digital I/O. |
| AN11 | | | | I | Analog | Analog input 11. |
| KBI0 | | | | I | TTL | Interrupt-on-change pin. |
| CSSPP | | | | O | — | SPP chip select control output. |
| RB5/KBI1/PGM | 38 | 15 | 15 | | | |
| RB5 | | | | I/O | TTL | Digital I/O. |
| KBI1 | | | | I | TTL | Interrupt-on-change pin. |
| PGM | | | | I/O | ST | Low-Voltage ICSP™ Programming enable pin. |
| RB6/KBI2/PGC | 39 | 16 | 16 | | | |
| RB6 | | | | I/O | TTL | Digital I/O. |
| KBI2 | | | | I | TTL | Interrupt-on-change pin. |
| PGC | | | | I/O | ST | In-Circuit Debugger and ICSP programming clock pin. |
| RB7/KBI3/PGD | 40 | 17 | 17 | | | |
| RB7 | | | | I/O | TTL | Digital I/O. |
| KBI3 | | | | I | TTL | Interrupt-on-change pin. |
| PGD | | | | I/O | ST | In-Circuit Debugger and ICSP programming data pin. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

**3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). PORTD can be software programmed for internal weak pull-ups on all inputs. These pins have TTL input buffers when the SPP module is enabled. |
| RD0/SPP0 | 19 | 38 | 38 | | | |
| RD0 | | | | I/O | ST | Digital I/O. |
| SPP0 | | | | I/O | TTL | Streaming Parallel Port data. |
| RD1/SPP1 | 20 | 39 | 39 | | | |
| RD1 | | | | I/O | ST | Digital I/O. |
| SPP1 | | | | I/O | TTL | Streaming Parallel Port data. |
| RD2/SPP2 | 21 | 40 | 40 | | | |
| RD2 | | | | I/O | ST | Digital I/O. |
| SPP2 | | | | I/O | TTL | Streaming Parallel Port data. |
| RD3/SPP3 | 22 | 41 | 41 | | | |
| RD3 | | | | I/O | ST | Digital I/O. |
| SPP3 | | | | I/O | TTL | Streaming Parallel Port data. |
| RD4/SPP4 | 27 | 2 | 2 | | | |
| RD4 | | | | I/O | ST | Digital I/O. |
| SPP4 | | | | I/O | TTL | Streaming Parallel Port data. |
| RD5/SPP5/P1B | 28 | 3 | 3 | | | |
| RD5 | | | | I/O | ST | Digital I/O. |
| SPP5 | | | | I/O | TTL | Streaming Parallel Port data. |
| P1B | | | | O | — | ECCP1 PWM output, channel B. |
| RD6/SPP6/P1C | 29 | 4 | 4 | | | |
| RD6 | | | | I/O | ST | Digital I/O. |
| SPP6 | | | | I/O | TTL | Streaming Parallel Port data. |
| P1C | | | | O | — | ECCP1 PWM output, channel C. |
| RD7/SPP7/P1D | 30 | 5 | 5 | | | |
| RD7 | | | | I/O | ST | Digital I/O. |
| SPP7 | | | | I/O | TTL | Streaming Parallel Port data. |
| P1D | | | | O | — | ECCP1 PWM output, channel D. |

**Legend:** TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels I = Input
O = Output P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

**3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | PDIP | QFN | TQFP | | | |
| | | | | | | PORTE is a bidirectional I/O port. |
| RE0/AN5/CK1SPP | 8 | 25 | 25 | | | |
| RE0 | | | | I/O | ST | Digital I/O. |
| AN5 | | | | I | Analog | Analog input 5. |
| CK1SPP | | | | O | — | SPP clock 1 output. |
| RE1/AN6/CK2SPP | 9 | 26 | 26 | | | |
| RE1 | | | | I/O | ST | Digital I/O. |
| AN6 | | | | I | Analog | Analog input 6. |
| CK2SPP | | | | O | — | SPP clock 2 output. |
| RE2/AN7/OESPP | 10 | 27 | 27 | | | |
| RE2 | | | | I/O | ST | Digital I/O. |
| AN7 | | | | I | Analog | Analog input 7. |
| OESPP | | | | O | — | SPP output enable output. |
| RE3 | — | — | — | — | — | See $\overline{MCLR}$/VPP/RE3 pin. |
| VSS | 12, 31 | 6, 30, 31 | 6, 29 | P | — | Ground reference for logic and I/O pins. |
| VDD | 11, 32 | 7, 8, 28, 29 | 7, 28 | P | — | Positive supply for logic and I/O pins. |
| VUSB | 18 | 37 | 37 | | | Internal USB transceiver power supply. |
| | | | | O | — | When the internal USB regulator is enabled, VUSB is the regulator output. |
| | | | | P | — | When the internal USB regulator is disabled, VUSB is the power input for the USB transceiver. |
| NC/ICCK/ICPGC(3) | — | — | 12 | | | No Connect or dedicated ICD/ICSP™ port clock. |
| ICCK | | | | I/O | ST | In-Circuit Debugger clock. |
| ICPGC | | | | I/O | ST | ICSP programming clock. |
| NC/ICDT/ICPGD(3) | — | — | 13 | | | No Connect or dedicated ICD/ICSP port clock. |
| ICDT | | | | I/O | ST | In-Circuit Debugger data. |
| ICPGD | | | | I/O | ST | ICSP programming data. |
| NC/$\overline{ICRST}$/ICVPP(3) | — | — | 33 | | | No Connect or dedicated ICD/ICSP port Reset. |
| $\overline{ICRST}$ | | | | I | — | Master Clear (Reset) input. |
| ICVPP | | | | P | — | Programming voltage input. |
| NC/ICPORTS(3) | — | — | 34 | P | — | No Connect or 28-pin device emulation. |
| ICPORTS | | | | | | Enable 28-pin device emulation when connected to VSS. |
| NC | — | 13 | — | — | — | No Connect. |

**Legend:** TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

**3:** These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

## 2.0 12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40-pin and 44-pin devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

**REGISTER 2-1: ADCON0: A/D CONTROL REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{\text{DONE}}$ | ADON |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)**(1,2)**
0110 = Channel 6 (AN6)**(1,2)**
0111 = Channel 7 (AN7)**(1,2)**
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12
1101 = Unimplemented**(2)**
1110 = Unimplemented**(2)**
1111 = Unimplemented**(2)**

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

**Note 1:** These channels are not implemented on 28-pin devices.
**2:** Performing a conversion on unimplemented channels will return a floating input measurement.

**REGISTER 2-2: ADCON1: A/D CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W(1) | R/W(1) | R/W(1) |
|---|---|---|---|---|---|---|---|
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit ($V_{REF-}$ source)
1 = $V_{REF-}$ (AN2)
0 = $V_{SS}$

bit 4 **VCFG0:** Voltage Reference Configuration bit ($V_{REF+}$ source)
1 = $V_{REF+}$ (AN3)
0 = $V_{DD}$

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

| PCFG3: PCFG0 | AN12 | AN11 | AN10 | AN9 | AN8 | AN7(2) | AN6(2) | AN5(2) | AN4 | AN3 | AN2 | AN1 | AN0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000(1) | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111(1) | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input D = Digital I/O

**Note 1:** The Reset value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

**2:** AN5 through AN7 are available only on 40-pin and 44-pin devices.

**REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADFM | — | ACQT2 | ACQT1 | ACQT0 | ADCS2 | ADCS1 | ADCS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage ($V_{DD}$ and $V_{SS}$), or the voltage level on the RA3/AN3/$V_{REF+}$ and RA2/AN2/$V_{REF-}$/C$V_{REF}$ pins.

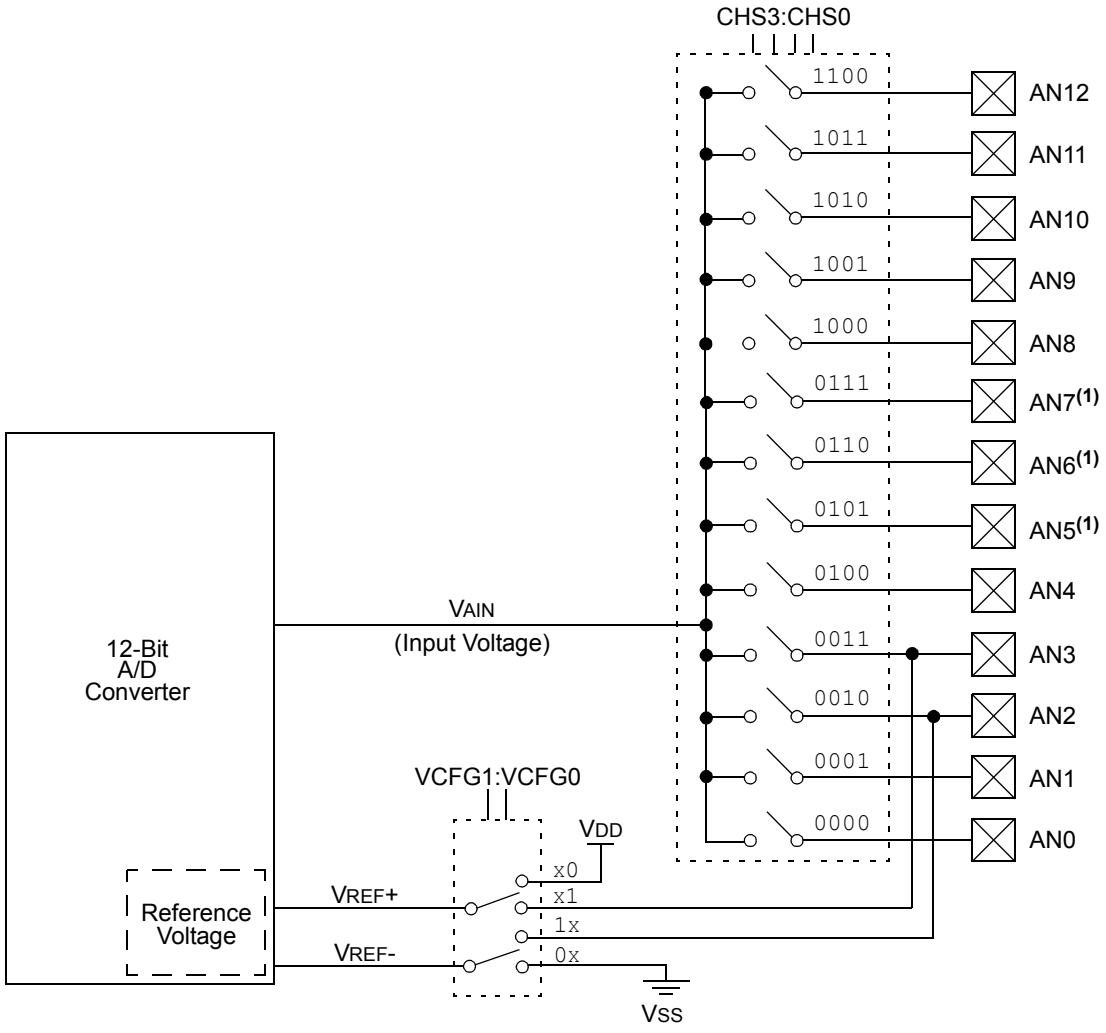
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the Converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/$\overline{\text{DONE}}$ bit (ADCON0 register) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.

**FIGURE 2-1: A/D BLOCK DIAGRAM**




**Note 1:** Channels AN5 through AN7 are not available on 28-pin devices.

The value in the ADRESH:ADRESL registers is unknown following Power-on and Brown-out Resets, and is not affected by any other Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 2.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/$\overline{\text{DONE}}$ bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0 register)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

**FIGURE 2-2: A/D TRANSFER FUNCTION**

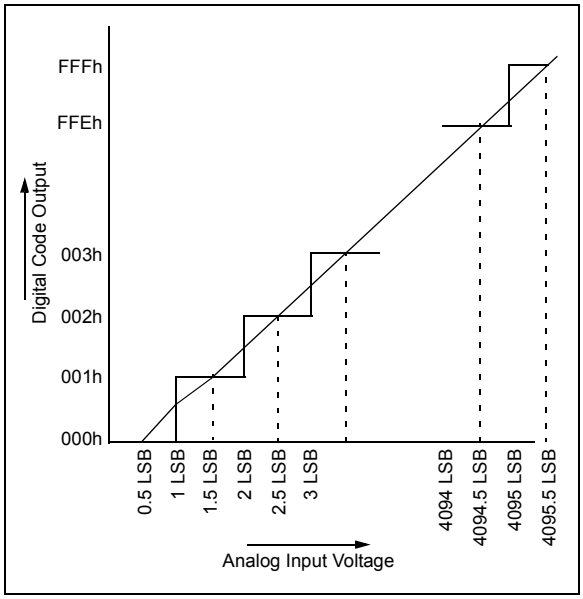
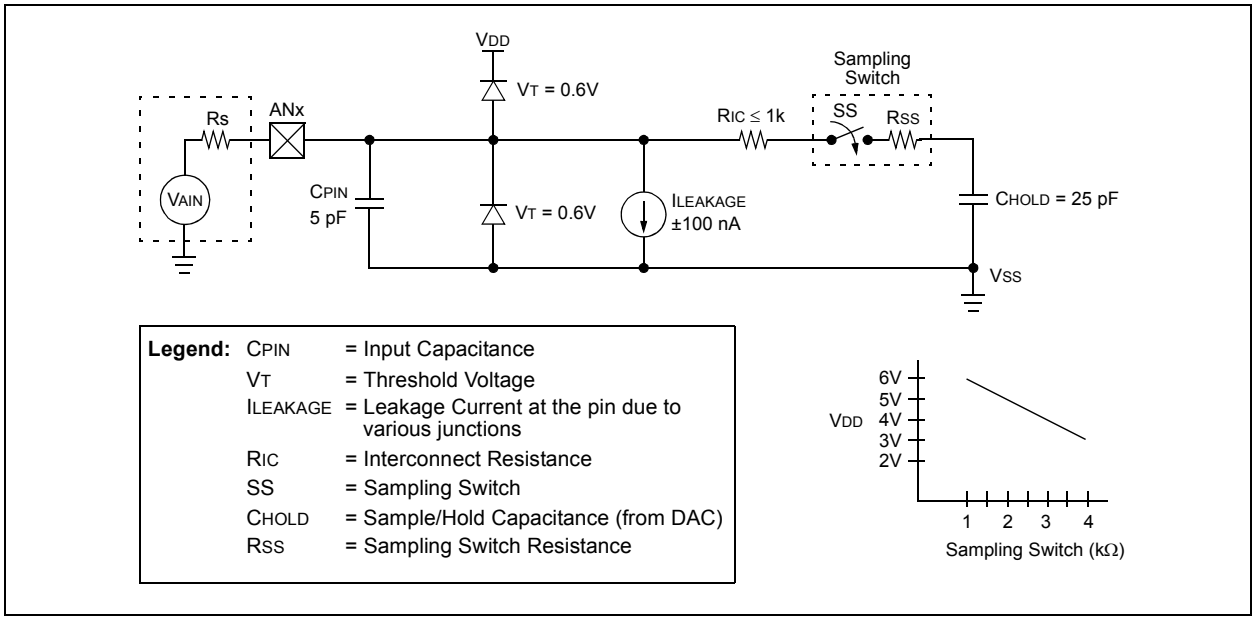



**FIGURE 2-3: ANALOG INPUT MODEL**



## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provides a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

| A/D Clock Source (TAD) | | Assumes TAD Min. = 0.8 μs |
|---|---|---|
| **Operation** | **ADCS2:ADCS0** | **Maximum FOSC** |
| 2 TOSC | 000 | 2.50 MHz |
| 4 TOSC | 100 | 5.00 MHz |
| 8 TOSC | 001 | 10.00 MHz |
| 16 TOSC | 101 | 20.00 MHz |
| 32 TOSC | 010 | 40.00 MHz |
| 64 TOSC | 110 | 48.00 MHz |
| RC(1) | x11 | 1.00 MHz(2) |

**Note 1:** The RC source has a typical TAD time of 2.5 μs.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

## 2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the $T_{AD}$ time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D $F_{RC}$ clock to be selected. If bits ACQT2:ACQT0 are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

## 2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level ($V_{OH}$ or $V_{OL}$) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

**Note 1:** When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.

**2:** Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.

**3:** The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG3:PCFG0 bits in ADCON1 are reset.

**NOTES:**

## APPENDIX A: REVISION HISTORY

### Revision A (May 2007)

Original data sheet for the PIC18F2458/2553/4458/4553 devices.

### Revision B (June 2007)

Changes to Figure 4-2: PIC18LF2458/2553/4458/4553 Voltage-Frequency Graph (Industrial).

### Revision C (October 2009)

Removed “Preliminary” marking.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

| Features | PIC18F2458 | PIC18F2553 | PIC18F4458 | PIC18F4553 |
|---|---|---|---|---|
| Program Memory (Bytes) | 24576 | 32768 | 24576 | 32768 |
| Program Memory (Instructions) | 12288 | 16384 | 12288 | 16384 |
| Interrupt Sources | 19 | 19 | 20 | 20 |
| I/O Ports | Ports A, B, C, (E) | Ports A, B, C, (E) | Ports A, B, C, D, E | Ports A, B, C, D, E |
| Capture/Compare/PWM Modules | 2 | 2 | 1 | 1 |
| Enhanced Capture/Compare/ PWM Modules | 0 | 0 | 1 | 1 |
| Parallel Communications (SPP) | No | No | Yes | Yes |
| 12-Bit Analog-to-Digital Module | 10 Input Channels | 10 Input Channels | 13 Input Channels | 13 Input Channels |
| Packages | 28-Pin SPDIP<br>28-Pin SOIC | 28-Pin SPDIP<br>28-Pin SOIC | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN | 40-Pin PDIP<br>44-Pin TQFP<br>44-Pin QFN |

# INDEX

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## PRODUCT IDENTIFICATION SYSTEM

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| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | | |
|---|---|---|
| Device | PIC18F2458/2553(1), PIC18F4458/4553(1), PIC18F2458/2553T(2), PIC18F4458/4553T(2); VDD range 4.2V to 5.5V<br>PIC18LF2458/2553(1), PIC18LF4458/4553(1), PIC18LF2458/2553T(2), PIC18LF4458/4553T(2); VDD range 2.0V to 5.5V | |
| Temperature Range | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) | |
| Package | PT = TQFP (Thin Quad Flatpack)<br>SO = SOIC<br>SP = Skinny PDIP<br>P = PDIP<br>ML = QFN | |
| Pattern | QTP, SQTP, Code or Special Requirements (blank otherwise) | |

**Examples:**

a) PIC18LF4553-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.

b) PIC18LF2458-I/SO = Industrial temp., SOIC package, Extended VDD limits.

c) PIC18F4458-I/P = Industrial temp., PDIP package, normal VDD limits.

**Note 1:** F = Standard Voltage Range
LF = Wide Voltage Range

**2:** T = In tape and reel TQFP packages only.