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Core Size	8-Bit
Speed	48MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18f4553-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic18f4553-i-pt</a>

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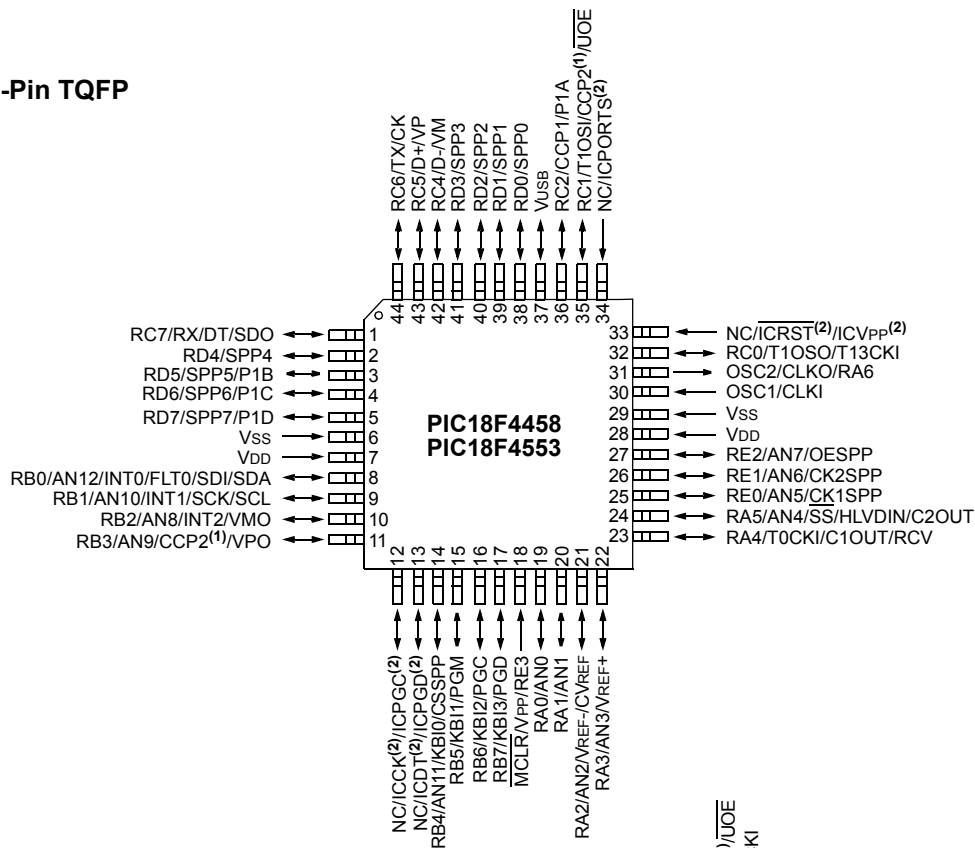
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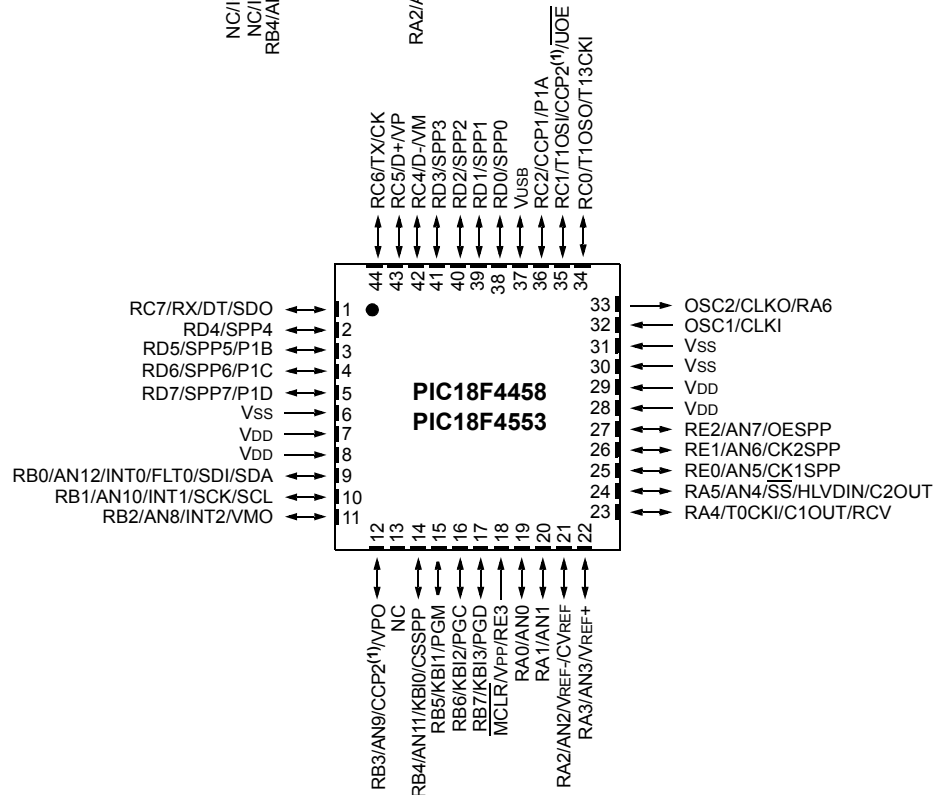
# PIC18F2458/2553/4458/4553

## Pin Diagrams (Continued)

### 44-Pin TQFP



### 44-Pin QFN



- Note**
- 1: RB3 is the alternate pin for CCP2 multiplexing.
  - 2: Special ICPORT features are available only in 44-pin TQFP packages. See Section 25.9 "Special ICPORT Features" in the "PIC18F2455/2550/4455/4550 Data Sheet".

# PIC18F2458/2553/4458/4553

## 1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F2458
- PIC18F4458
- PIC18F2553
- PIC18F4553

**Note:** This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F2455/2550/4455/4550 devices. For information on the features and specifications shared by the PIC18F2458/2553/4458/4553 and PIC18F2455/2550/4455/4550 devices, see the "PIC18F2455/2550/4455/4550 Data Sheet" (DS39632).

The PIC18F4553 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F4553 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

### 1.1 Special Features

- **12-Bit A/D Converter:** The PIC18F4553 family implements a 12-bit A/D Converter. The A/D Converter incorporates programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

## 1.2 Details on Individual Family Members

The PIC18F2458/2553/4458/4553 devices are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in the following ways:

1. Flash program memory (24 Kbytes for PIC18FX458 devices, 32 Kbytes for PIC18FX553).
2. A/D channels (10 for 28-pin devices, 13 for 40-pin and 44-pin devices).
3. I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40-pin and 44-pin devices).
4. CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40-pin and 44-pin devices have one standard CCP module and one ECCP module).
5. Streaming Parallel Port (present only on 40/44-pin devices).

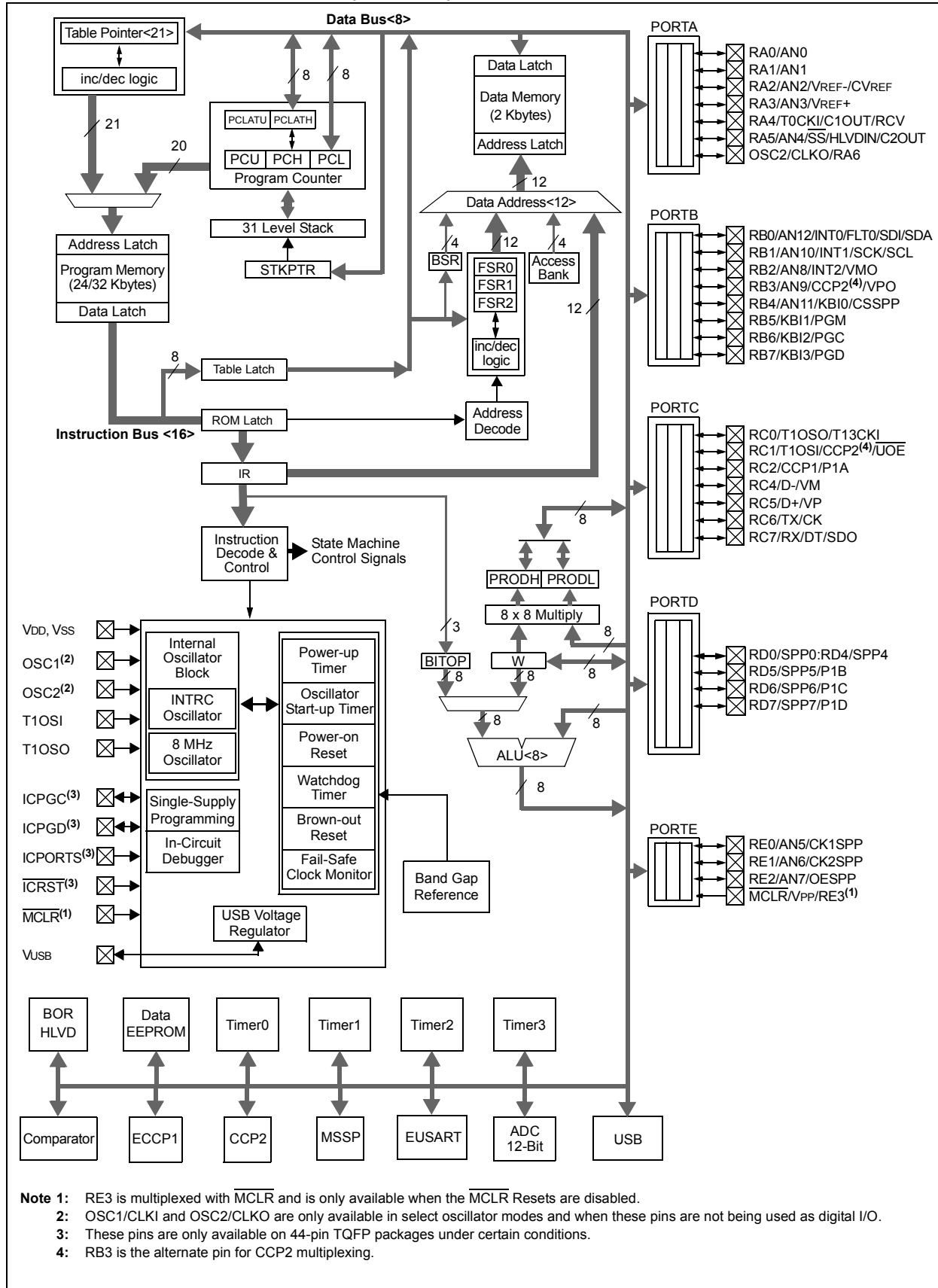
All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F4553 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2458), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2458), function over an extended VDD range of 2.0V to 5.5V.

# PIC18F2458/2553/4458/4553

**FIGURE 1-2: PIC18F4458/4553(40/44-PIN) BLOCK DIAGRAM**





# PIC18F2458/2553/4458/4553

**TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	SPDIP, SOIC			
RA0/AN0	2	I/O I	TTL Analog	PORTA is a bidirectional I/O port.  Digital I/O. Analog input 0.
RA1/AN1	3			Digital I/O. Analog input 1.
RA2/AN2/VREF-/CVREF	4	I/O I I O	TTL Analog Analog Analog	Digital I/O. Analog input 2. A/D reference voltage (low) input. Analog comparator reference output.
RA3/AN3/VREF+	5			Digital I/O. Analog input 3. A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			Digital I/O. Timer0 external clock input. Comparator 1 output. External USB transceiver RCV input.
RA5/AN4/ $\overline{SS}$ /HLVDIN/C2OUT	7			Digital I/O. Analog input 4. SPI slave select input. High/Low-Voltage Detect input. Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power

**Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.

# PIC18F2458/2553/4458/4553

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3 MCLR  VPP RE3	1	18	18	I  P I	ST  ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI OSC1 CLKI	13	32	30	I I	Analog Analog	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6 OSC2  CLKO  RA6	14	33	31	O  O  I/O	—  — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels I = Input  
O = Output P = Power

- Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.  
**3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.



# PIC18F2458/2553/4458/4553

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RD0/SPP0	19	38	38			PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). PORTD can be software programmed for internal weak pull-ups on all inputs. These pins have TTL input buffers when the SPP module is enabled.
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	ECCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	ECCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	ECCP1 PWM output, channel D.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input  
O = Output      P = Power

- Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.  
**3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

# PIC18F2458/2553/4458/4553

**TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RE0/AN5/CK1SPP RE0 AN5 CK1SPP	8	25	25	I/O I O	ST Analog —	PORTC is a bidirectional I/O port.  Digital I/O. Analog input 5. SPP clock 1 output.
RE1/AN6/CK2SPP RE1 AN6 CK2SPP	9	26	26	I/O I O	ST Analog —	Digital I/O. Analog input 6. SPP clock 2 output.
RE2/AN7/OESPP RE2 AN7 OESPP	10	27	27	I/O I O	ST Analog —	Digital I/O. Analog input 7. SPP output enable output.
RE3	—	—	—	—	—	See MCLR/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O  P	—  —	Internal USB transceiver power supply. When the internal USB regulator is enabled, VUSB is the regulator output. When the internal USB regulator is disabled, VUSB is the power input for the USB transceiver.
NC/ICCK/ICPGC <sup>(3)</sup> ICCK ICPGC	—	—	12	I/O I/O	ST ST	No Connect or dedicated ICD/ICSP™ port clock. In-Circuit Debugger clock. ICSP programming clock.
NC/ICDT/ICPGD <sup>(3)</sup> ICDT ICPGD	—	—	13	I/O I/O	ST ST	No Connect or dedicated ICD/ICSP port clock. In-Circuit Debugger data. ICSP programming data.
NC/ICRST/ICVPP <sup>(3)</sup> ICRST ICVPP	—	—	33	I P	— —	No Connect or dedicated ICD/ICSP port Reset. Master Clear (Reset) input. Programming voltage input.
NC/ICPORTS <sup>(3)</sup> ICPORTS	—	—	34	P	—	No Connect or 28-pin device emulation. Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

**Legend:** TTL = TTL compatible input  
ST = Schmitt Trigger input with CMOS levels  
O = Output  
CMOS = CMOS compatible input or output  
I = Input  
P = Power

- Note 1:** Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.  
**2:** Default assignment for CCP2 when CCP2MX Configuration bit is set.  
**3:** These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

# PIC18F2458/2553/4458/4553

## REGISTER 2-3:     ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7     **ADFM:** A/D Result Format Select bit

1 = Right justified

0 = Left justified

bit 6     **Unimplemented:** Read as '0'

bit 5-3   **ACQT2:ACQT0:** A/D Acquisition Time Select bits

111 = 20 TAD

110 = 16 TAD

101 = 12 TAD

100 = 8 TAD

011 = 6 TAD

010 = 4 TAD

001 = 2 TAD

000 = 0 TAD<sup>(1)</sup>

bit 2-0   **ADCS2:ADCS0:** A/D Conversion Clock Select bits

111 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

110 = FOSC/64

101 = FOSC/16

100 = FOSC/4

011 = FRC (clock derived from A/D RC oscillator)<sup>(1)</sup>

010 = FOSC/32

001 = FOSC/8

000 = FOSC/2

**Note 1:** If the A/D FRC clock source is selected, a delay of one T<sub>CY</sub> (instruction cycle) is added before the A/D clock starts. This allows the **SLEEP** instruction to be executed before starting a conversion.

# PIC18F2458/2553/4458/4553

## 2.1 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 2-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

**Note:** When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 2-1 may be used. This equation assumes that 1/2 LSB error is used (4096 steps for the 12-bit A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Example 2-3 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	25 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	3V → Rss = 4 kΩ
Temperature	=	85°C (system max.)

### EQUATION 2-1: ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= \text{TAMP} + \text{TC} + \text{TCOFF} \end{aligned}$$

### EQUATION 2-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} \text{V}_{\text{HOLD}} &= (\text{V}_{\text{REF}} - (\text{V}_{\text{REF}}/4096)) \cdot (1 - e^{-(\text{TC}/\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS})}) \\ \text{or} \\ \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \end{aligned}$$

### EQUATION 2-3: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} \text{TACQ} &= \text{TAMP} + \text{TC} + \text{TCOFF} \\ \text{TAMP} &= 0.2 \mu\text{s} \\ \text{TCOFF} &= (\text{Temp} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad (85^\circ\text{C} - 25^\circ\text{C})(0.02 \mu\text{s}/^\circ\text{C}) \\ &\quad 1.2 \mu\text{s} \end{aligned}$$

Temperature coefficient is only required for temperatures > 25°C. Below 25°C, TCOFF = 0 μs.

$$\begin{aligned} \text{TC} &= -(\text{CHOLD})(\text{RIC} + \text{RSS} + \text{RS}) \ln(1/4096) \mu\text{s} \\ &\quad -(25 \text{ pF})(1 \text{ k}\Omega + 4 \text{ k}\Omega + 2.5 \text{ k}\Omega) \ln(0.0002441) \mu\text{s} \\ &\quad 1.56 \mu\text{s} \\ \text{TACQ} &= 0.2 \mu\text{s} + 1.56 \mu\text{s} + 1.2 \mu\text{s} \\ &\quad 2.96 \mu\text{s} \end{aligned}$$

## 2.2 Selecting and Configuring Acquisition Time

The ADCON2 register allows the user to select an acquisition time that occurs each time the GO/DONE bit is set. It also gives users the option to use an automatically determined acquisition time.

Acquisition time may be set with the ACQT2:ACQT0 bits (ADCON2<5:3>), which provides a range of 2 to 20 TAD. When the GO/DONE bit is set, the A/D module continues to sample the input for the selected acquisition time, then automatically begins a conversion. Since the acquisition time is programmed, there may be no need to wait for an acquisition time between selecting a channel and setting the GO/DONE bit.

Manual acquisition is selected when ACQT2:ACQT0 = 000. When the GO/DONE bit is set, sampling is stopped and a conversion begins. The user is responsible for ensuring the required acquisition time has passed between selecting the desired input channel and setting the GO/DONE bit. This option is also the default Reset state of the ACQT2:ACQT0 bits and is compatible with devices that do not offer programmable acquisition times.

In either case, when the conversion is completed, the GO/DONE bit is cleared, the ADIF flag is set and the A/D begins sampling the currently selected channel again. If an acquisition time is programmed, there is nothing to indicate if the acquisition time has ended or if the conversion has begun.

## 2.3 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 13 TAD per 12-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2 TOSC
- 4 TOSC
- 8 TOSC
- 16 TOSC
- 32 TOSC
- 64 TOSC
- Internal RC Oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be as short as possible, but greater than the minimum TAD (see parameter 130 for more information).

Table 2-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

**TABLE 2-1: TAD vs. DEVICE OPERATING FREQUENCIES**

A/D Clock Source (TAD)		Assumes TAD Min. = 0.8 $\mu$ s
Operation	ADCS2:ADCS0	Maximum Fosc
2 TOSC	000	2.50 MHz
4 TOSC	100	5.00 MHz
8 TOSC	001	10.00 MHz
16 TOSC	101	20.00 MHz
32 TOSC	010	40.00 MHz
64 TOSC	110	48.00 MHz
RC <sup>(1)</sup>	x11	1.00 MHz <sup>(2)</sup>

**Note 1:** The RC source has a typical TAD time of 2.5  $\mu$ s.

**2:** For device frequencies above 1 MHz, the device must be in Sleep for the entire conversion or a FOSC divider should be used instead; otherwise, the A/D accuracy specification may not be met.

# PIC18F2458/2553/4458/4553

## 2.8 Use of the CCP2 Trigger

An A/D conversion can be started by the Special Event Trigger of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as '1011' and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D acquisition and conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (firmware must move ADRESH:ADRESL to

the desired location). The appropriate analog input channel must be selected and the minimum acquisition period is either timed by the user, or an appropriate TACQ time selected before the Special Event Trigger sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the Special Event Trigger will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

**TABLE 2-2: REGISTERS ASSOCIATED WITH A/D OPERATION**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	(4)
PIR1	SPPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	(4)
PIE1	SPPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	(4)
IPR1	SPPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	(4)
PIR2	OSCFIF	CMIF	USBIF	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF	(4)
PIE2	OSCFIE	CMIE	USBIE	EEIE	BCLIE	HLVDIE	TMR3IE	CCP2IE	(4)
IPR2	OSCFIP	CMIP	USBIP	EEIP	BCLIP	HLVDIP	TMR3IP	CCP2IP	(4)
ADRESH	A/D Result Register High Byte								(4)
ADRESL	A/D Result Register Low Byte								(4)
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	21
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	22
ADCON2	ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	23
PORTA	—	RA6 <sup>(2)</sup>	RA5	RA4	RA3	RA2	RA1	RA0	(4)
TRISA	—	TRISA6 <sup>(2)</sup>	PORTA Data Direction Control Register						(4)
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	(4)
TRISB	PORTB Data Direction Control Register								(4)
LATB	PORTB Data Latch Register (Read and Write to Data Latch)								(4)
PORTE <sup>(1)</sup>	RDPU	—	—	—	RE3 <sup>(3)</sup>	RE2 <sup>(1)</sup>	RE1 <sup>(1)</sup>	RE0 <sup>(1)</sup>	(4)
TRISE <sup>(1)</sup>	—	—	—	—	—	TRISE2	TRISE1	TRISE0	(4)
LATE <sup>(1)</sup>	—	—	—	—	—	PORTE Data Latch Register			(4)

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

**Note 1:** These registers and/or bits are not implemented on 28-pin devices and are read as '0'.

**2:** RA6 and its associated latch and data direction bits are enabled as I/O pins based on oscillator configuration; otherwise, they are read as '0'.

**3:** RE3 port bit is available only as an input pin when the MCLRE Configuration bit is '0'.

**4:** For these Reset values, see the "PIC18F2455/2550/4455/4550 Data Sheet".

# PIC18F2458/2553/4458/4553

## 3.0 SPECIAL FEATURES OF THE CPU

**Note:** For additional details on the Configuration bits, refer to the “PIC18F2455/2550/4455/4550 Data Sheet”, Section 25.1 “Configuration Bits”. Device ID information presented in this section is for PIC18F2458/2553/4458/4553 only.

PIC18F2458/2553/4458/4553 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

- Device ID Registers

## 3.1 Device ID Registers

The Device ID registers are “read-only” registers. They identify the device type and revision to device programmers, and can be read by firmware using table reads.

**TABLE 3-1: DEVICE IDs**

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx <sup>(1)</sup>
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx <sup>(1)</sup>

**Legend:** x = unknown, u = unchanged

**Note 1:** See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

# PIC18F2458/2553/4458/4553

## REGISTER 3-1: DEVID1: DEVICE ID REGISTER 1 FOR PIC18F2458/2553/4458/4553 DEVICES

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-5

**DEV2:DEV0:** Device ID bits

See Register 3-2 for a complete listing.

bit 4-0

**REV3:REV0:** Revision ID bits

These bits are used to indicate the device revision.

## REGISTER 3-2: DEVID2: DEVICE ID REGISTER 2 FOR PIC18F2458/2553/4458/4553 DEVICES

R	R	R	R	R	R	R	R
DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 7							bit 0

### Legend:

R = Read-only bit

P = Programmable bit

U = Unimplemented bit, read as '0'

-n = Value when device is unprogrammed

u = Unchanged from programmed state

bit 7-0

**DEV10:DEV3:** Device ID bits

DEV10:DEV3 (DEVID2<7:0>)	DEV2:DEV0 (DEVID1<7:5>)	Device
0010 1010	011	PIC18F2458
0010 1010	010	PIC18F2553
0010 1010	001	PIC18F4458
0010 1010	000	PIC18F4553



# PIC18F2458/2553/4458/4553

FIGURE 4-1: PIC18F2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

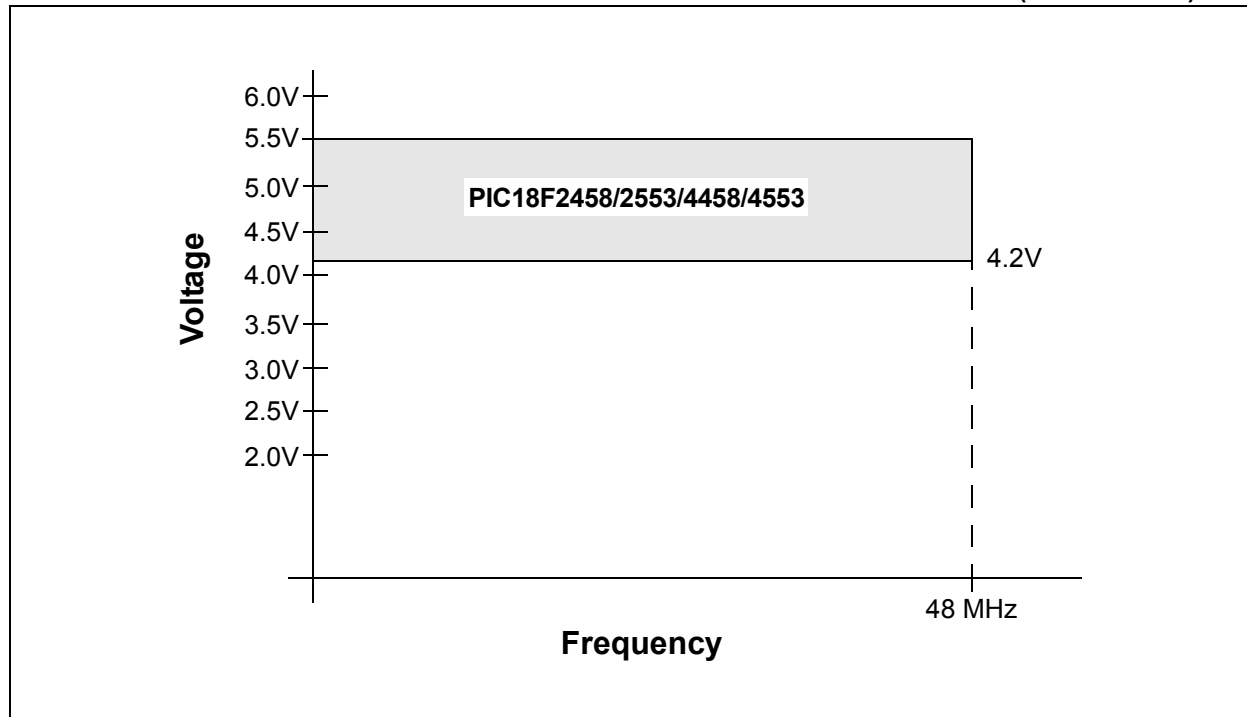
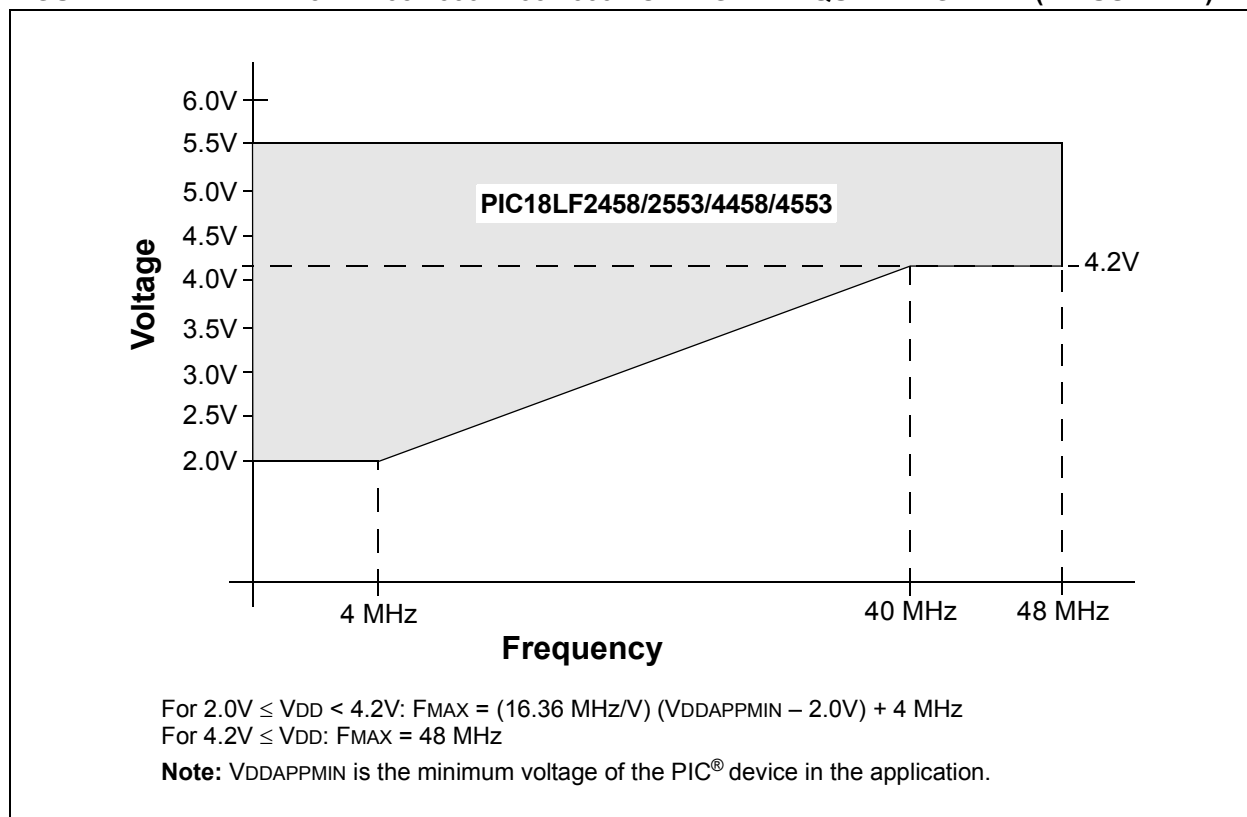
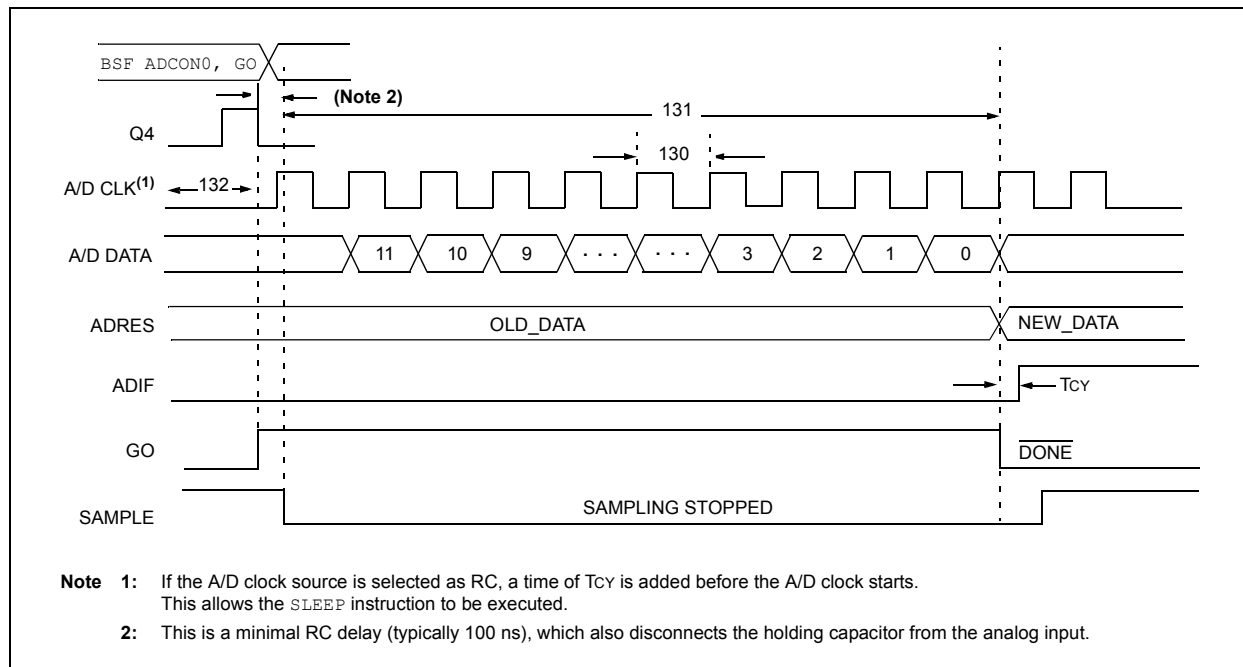


FIGURE 4-2: PIC18LF2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



# PIC18F2458/2553/4458/4553

**FIGURE 4-3: A/D CONVERSION TIMING**



**TABLE 4-2: A/D CONVERSION REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC18FXXXX	0.8	12.5 <sup>(1)</sup>	μs	TOSC based, VREF ≥ 3.0V
			PIC18LFXXXX	1.4	25.0 <sup>(1)</sup>	μs	VDD = 3.0V; TOSC based, VREF full range
			PIC18FXXXX	—	1	μs	A/D RC mode
			PIC18LFXXXX	—	3	μs	VDD = 3.0V; A/D RC mode
131	TCNV	Conversion Time (not including acquisition time) <sup>(2)</sup>		13	14	TAD	
132	TACQ	Acquisition Time <sup>(3)</sup>		1.4	—	μs	
135	TSWC	Switching Time from Convert → Sample		—	(Note 4)		
137	TDIS	Discharge Time		0.2	—	μs	

- Note 1:** The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.
- Note 2:** ADRES registers may be read on the following  $T_{CY}$  cycle.
- Note 3:** The time for the holding capacitor to acquire the “New” input voltage when the voltage changes full scale after the conversion (VDD to VSS or VSS to VDD). The source impedance ( $R_S$ ) on the input channels is 50 $\Omega$ .
- Note 4:** On the following cycle of the device clock.

## 5.0 PACKAGING INFORMATION

For packaging information, see the “*PIC18F2455/2550/4455/4550 Data Sheet*” (DS39632).

# PIC18F2458/2553/4458/4553

## APPENDIX A: REVISION HISTORY

### Revision A (May 2007)

Original data sheet for the PIC18F2458/2553/4458/4553 devices.

### Revision B (June 2007)

Changes to Figure 4-2: PIC18LF2458/2553/4458/4553 Voltage-Frequency Graph (Industrial).

### Revision C (October 2009)

Removed "Preliminary" marking.

## APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

**TABLE B-1: DEVICE DIFFERENCES**

Features	PIC18F2458	PIC18F2553	PIC18F4458	PIC18F4553
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Parallel Communications (SPP)	No	No	Yes	Yes
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Packages	28-Pin SPDIP 28-Pin SOIC	28-Pin SPDIP 28-Pin SOIC	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN

# PIC18F2458/2553/4458/4553

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	PIC18F2458/2553 <sup>(1)</sup> , PIC18F4458/4553 <sup>(1)</sup> , PIC18F2458/2553T <sup>(2)</sup> , PIC18F4458/4553T <sup>(2)</sup> ; VDD range 4.2V to 5.5V PIC18LF2458/2553 <sup>(1)</sup> , PIC18LF4458/4553 <sup>(1)</sup> , PIC18LF2458/2553T <sup>(2)</sup> , PIC18LF4458/4553T <sup>(2)</sup> ; VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SP = Skinny PDIP P = PDIP ML = QFN		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

**Examples:**

- a) PIC18LF4553-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.
- b) PIC18LF2458-I/SO = Industrial temp., SOIC package, Extended VDD limits.
- c) PIC18F4458-I/P = Industrial temp., PDIP package, normal VDD limits.

  
**Note 1:** F = Standard Voltage Range  
LF = Wide Voltage Range  
**2:** T = In tape and reel TQFP packages only.