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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	35
Program Memory Size	24KB (12K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4458t-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Diagrams

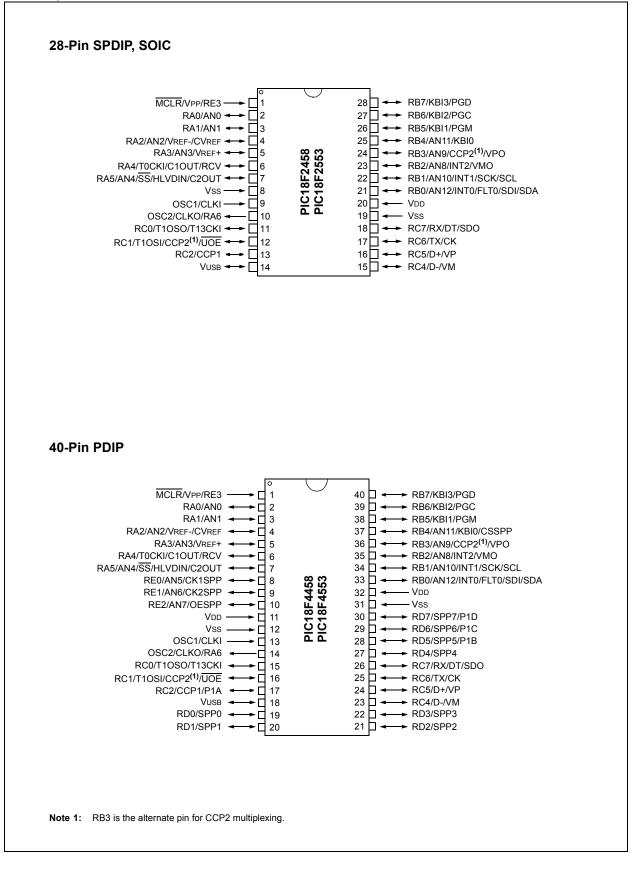


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To determine if an errata sheet exists for a particular device, please check with one of the following:

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

• PIC18F2458 •	PIC18F4458
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• PIC18F2553 • PIC18F4553

Note: This data sheet documents only the devices' features and specifications that are in addition to the features and specifications of the PIC18F2455/2550/4455/4550 devices. For information on the features and specifications shared by the PIC18F2458/2553/4458/4553 and PIC18F2455/2550/4455/4550 devices see the "PIC18F2455/2550/4455/4550 Data Sheet" (DS39632).

The PIC18F4553 family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high-endurance, Enhanced Flash program memory. In addition to these features, the PIC18F4553 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 Special Features

 12-Bit A/D Converter: The PIC18F4553 family implements a 12-bit A/D Converter. The A/D Converter incorporates programmable acquisition time. This allows for a channel to be selected and a conversion to be initiated, without waiting for a sampling period and thus, reducing code overhead.

1.2 Details on Individual Family Members

The PIC18F2458/2553/4458/4553 devices are available in 28-pin and 40/44-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

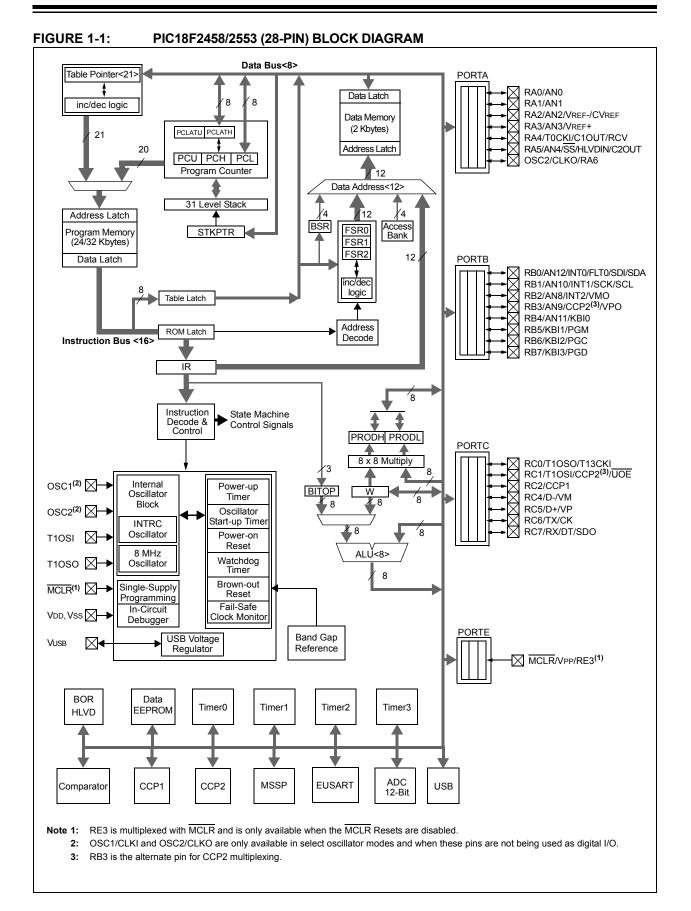
The devices are differentiated from each other in the following ways:

- 1. Flash program memory (24 Kbytes for PIC18FX458 devices, 32 Kbytes for PIC18FX553).
- 2. A/D channels (10 for 28-pin devices, 13 for 40-pin and 44-pin devices).
- I/O ports (3 bidirectional ports and 1 input only port on 28-pin devices, 5 bidirectional ports on 40-pin and 44-pin devices).
- CCP and Enhanced CCP implementation (28-pin devices have two standard CCP modules, 40-pin and 44-pin devices have one standard CCP module and one ECCP module).
- 5. Streaming Parallel Port (present only on 40/44-pin devices).

All other features for devices in this family are identical. These are summarized in Table 1-1.

The pinouts for all devices are listed in Table 1-2 and Table 1-3.

Members of the PIC18F4553 family are available as both standard and low-voltage devices. Standard devices with Enhanced Flash memory, designated with an "F" in the part number (such as PIC18F2458), accommodate an operating VDD range of 4.2V to 5.5V. Low-voltage parts, designated by "LF" (such as PIC18LF2458), function over an extended VDD range of 2.0V to 5.5V.



Pin Name	Pin Number	Pin	Buffer	Description	
Pin Name	SPDIP, SOIC	Туре	Туре	Description	
MCLR/VPP/RE3 MCLR	1	I	ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device.	
VPP		Р		Programming voltage input.	
RE3		I	ST	Digital input.	
OSC1/CLKI OSC1 CLKI	9		Analog Analog	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)	
OSC2/CLKO/RA6 OSC2	10	0	_	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.	
CLKO		0	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.	
RA6		I/O	TTL	General purpose I/O pin.	
Legend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels Output ST = Schmitt Trigger input with CMOS levels ST = Schmitt Trigger input with CMOS levels					

TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS

= Power Ρ

O = Output

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

Pin Name	Pin Number SPDIP, SOIC	Pin Type	Buffer Type	Description		
				PORTA is a bidirectional I/O port.		
RA0/AN0	2					
RA0	_	I/O	TTL	Digital I/O.		
AN0		I	Analog	Analog input 0.		
RA1/AN1	3					
RA1	, , , , , , , , , , , , , , , , , , ,	I/O	TTL	Digital I/O.		
AN1		I	Analog	Analog input 1.		
RA2/AN2/VREF-/CVREF	4		Ű			
RA2		I/O	TTL	Digital I/O.		
AN2			Analog	Analog input 2.		
VREF-		I	Analog	A/D reference voltage (low) input.		
CVREF		0	Analog	Analog comparator reference output.		
RA3/AN3/VREF+	5					
RA3	Ŭ	I/O	TTL	Digital I/O.		
AN3		I	Analog	Analog input 3.		
VREF+		I	Analog	A/D reference voltage (high) input.		
RA4/T0CKI/C1OUT/RCV	6					
RA4		I/O	ST	Digital I/O.		
TOCKI		I	ST	Timer0 external clock input.		
C1OUT		0	_	Comparator 1 output.		
RCV		I	TTL	External USB transceiver RCV input.		
RA5/AN4/SS/	7					
HLVDIN/C2OUT	-					
RA5		I/O	TTL	Digital I/O.		
AN4		Ι	Analog	Analog input 4.		
SS		I	TTL	SPI slave select input.		
HLVDIN		I	Analog	High/Low-Voltage Detect input.		
C2OUT		0	—	Comparator 2 output.		
RA6	_	_	—	See the OSC2/CLKO/RA6 pin.		
Legend: TTL = TTL cor	npatible in	put		CMOS = CMOS compatible input or output		
ST = Schmitt Trigger input with CMOS levels I = Input						
O = Output $P = Power$						

TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

RB0/AN12/INT0/FLT0/ SDI/SDA21rogrammed for internal weak pull-ups on all inputs.RB0/AN12/INT0/FLT0/ RB021ITTLDigital I/O.AN12IAnalog IAnalog input 12.AN12ISTExternal interrupt 0.FLT0ISTSPI data in.SDAI/OSTJPC M data I/O.SDAI/OSTJPC M data I/O.SDAI/OTTLDigital I/O.RB1I/OTTLDigital I/O.AN10IAnalog Analog input 10.INT1ISTSynchronous serial clock input/output for SPI mode.SCLI/OSTSynchronous serial clock input/output for IPC mode.SCKI/OSTSynchronous serial clock input/output for IPC mode.SCLI/OSTSynchronous serial clock input/output for IPC mode.SCLI/OTTLDigital I/O.AN8IAnalog Analog input 8.INT2ISTExternal interrupt 2.VMOO-External USB transceiver VMO output.RB3/AN9/CCP2/VPO24-RB4I/OTTLDigital I/O.AN9IAnalog Analog input 9.CCP2(1)I/OTTLDigital I/O.AN9ITTLDigital I/O.AN9ITTLDigital I/O.RB4I/OTTLDigital I/O.RB5I/OTTLDigital I/O.RB6/RB11/PGM26- <th>Pin Name</th> <th>Pin Number SPDIP, SOIC</th> <th>Pin Type</th> <th>Buffer Type</th> <th>Description</th>	Pin Name	Pin Number SPDIP, SOIC	Pin Type	Buffer Type	Description
RB0/AN12/INT0/FLT0/ SD/SDA 21 //O TTL Digital I/O. AM12 I Analog Analog input 12. INT0 I ST External interrupt 0. FLT0 I ST External interrupt 0. SDI I ST SPI data in. SDA I/O ST SPI data in. SDA I/O ST PCM fault input (CCP1 module). SDI I ST SPI data in. SDA I/O ST SPI data in. SCL I/O TTL Digital I/O. Analog I Analog Analog input 10. INT1 I ST Synchronous serial clock input/output for SPI mode. SCL I/O ST Synchronous serial clock input/output for SPI mode. SCL I/O ST Synchronous serial clock input/output for SPI mode. SCL I/O TTL Digital I/O. AN8 I ST External USB transceiver VMO output. RB3/AN9/CCP2/VPO 24 CCP2(1) CCP2(1) VPO O - External USB transceiver VMO output. RB4/AN11/KBI0 25 T Cop2(1) RB5/KB11/PGM 26					PORTB is a bidirectional I/O port. PORTB can be software
SDI/SDA RB0I/OTLDigital I/O. Analog input 12. External interrupt 0.NT0ISTExternal interrupt 0. PWM Fault input (CCP1 module). SDISD1ISTSPI data in. SPI data in.SDAI/OSTI/C™ data I/O.RB1/AN10/INT1/SCK/22IRB1I/OTTLDigital I/O. Analog input 10.RB1/AN10/INT1/SCK/22IRB1I/OTTLDigital I/O. Analog input 10.AN10IAnalog Analog input 10.INT1ISTExternal interrupt 1. SCLRB2I/OSTSynchronous serial clock input/output for SPI mode. SCLRB2/AN8/INT2/VMO23IRB2I/OSTRB3/AN9/CCP2/VPO24IRB3/AN9/CCP2/VPOIAnalog Analog input 8.RB3/AN9/CCP2/VPOVPOOCCP2(1)I/OVPOO-RB4I/OTTLDigital I/O. Analog input 9. CCP2(1)INT1IAnalog CCP2(1)IVPOOCRB4/AN11/KBI025RB4I/OITTLDigital I/O. Analog input 11.RB5/KB1/PGM26RB5I/ORB6/KB12/PGC27RB7I/ORB7I/ORB7I/ORB7I/ORB7I/ORB7I/ORB7I/O <t< td=""><td></td><td></td><td></td><td></td><td>programmed for internal weak pull-ups on all inputs.</td></t<>					programmed for internal weak pull-ups on all inputs.
RB0I/OTTLDigital I/O.AN12IAnalogAnalog input 12.INTOISTExternal interrupt 0.FLTOISTPWM Fault input (CCP1 module).SDIISTPI/OSDAI/OSTI ² C M data I/O.RB1/AN10/INT1/SCK/22IIRB1I/OTTLDigital I/O.AN10IAnalogAnalog input 10.INT1ISTExternal interrupt 1.SCKI/OSTSynchronous serial clock input/output for SP1 mode.SCLI/OSTSynchronous serial clock input/output for I ² C mode.RB2/AN8/INT2/VMO23External interrupt 2.RB2/AN8/INT2IAnalogNMOO-External interrupt 2.VMOO-External interrupt 2.VMOO-External interrupt 2.VMOO-External USB transceiver VMO output.RB3/AN9/CCP2/VPO24-RB4/AN11/KBI01AnalogAN11IAnalogAN11IAnalogAN11ICapture 2 input/Compare 2 output/PWM 2 output.VPOO-External USB transceiver VPO output.RB4/AN11/KBI0Z5-RB5I/OTTLDigital I/O.AN11IAnalogAN11ICAPTUP -on-change pin.PGMI/OTTLDigital I/O.RB6/KBI2/PGC2		21			
AN12IAnalogAnalog input 12.INT0ISTExternal interrupt 0.FLT0ISTPWM Fault input (CCP1 module).SDIISTSPI data in.SDAI/OSTI/C TM data I/O.RB1/AN10/INT1/SCK/22IISCLI/OTTLDigital I/O.AN10IAnalog input 10.INT1IAnalog input 10.INT1IAnalog input 10.SCLI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTRB2/AN8/INT2/VMO23External interrupt 2.RB2/AN8/INT2/VMO23External interrupt 2.RB3/AN9/CCP2/VPO24FRB3/AN9/CCP2/VPOIAnalog input 8.RB4I/OTTLDigital I/OAnalog input 9.CCP2(f)I/OTTLVPOO-RB4I/OITTLDigital I/O.RB4I/OTTLIRS/KB1/PGM26RB5I/ORB6/KB12/PGC27RB6I/ORB7I/ORB7/KB13/PGD28RB7I/ORB7I/ORB7I/ORB7I/ORB7I/O<			1/0	TTI	Digital I/O
INTOISTExternal interrupt 0.FLTOISTPWM Fault input (CCP1 module).SDIISTSPI data in.SDAI/OSTI²C™ data I/O.RB1/AN10/INT1/SCK/22ICLRB1I/OTTLAN10IAnalog input 10.INT1ISTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCKI/OSTSCLI/OSTSCLI/OSTSCLI/OSTSCKI/OSTSCLI/OSTSCLI/OSTSCLI/OSTSCLI/OSTRB2/AN8/INT2/VMO23RB3I/OTTLDigital I/O.AN8IAnalog input 8.INT2ISTCapture 2 input/Compare 2 output/PWM 2 output.VMOOCCP2(1)I/OVPOOVPOORB4/AN11/KBI025RB5I/ORB5/KBI1/PGM26RB5I/ORB6/KBI2/PGC27RB6I/ORB7/KBI3/PGD28RB7I/ORB7I/ORB7I/OSTIRB7I/ORB7I/ORB7 <tdi o<="" td="">RB7<tdi o<="" td="">RB7<tdi o<="" td=""><td></td><td></td><td></td><td></td><td></td></tdi></tdi></tdi>					
FLT0ISTPWM Fault input (CCP1 module).SD1ISTSPI data in.SDAI/OSTI ² C TM data I/O.RB1/AN10/INT1/SCK/22IISCLII/OTTLDigital I/O.AN10IAnalogAnalog input 10.INT1ISTExternal interrupt 1.SCKI/OSTSynchronous serial clock input/output for SPI mode.SCLI/OSTSynchronous serial clock input/output for I ² C mode.RB2/AN8/INT2/VMO23IIRB2I/OTTLDigital I/O.AN8IAnalogINT2ISTExternal interrupt 2.VMOO-External USB transceiver VMO output.RB3/AN9/CCP2/VPO24IRB4/AN11/KBI0IAnalogRB4/AN11/KBI0ITTLDigital I/O.Analog input 9.RB5/KBI1/PGM26RB5/KBI1/PGMIRB6/KBI2/PGCIRB6/KBI2/PGCIRB7I/ORB7/KBI3/PGD28RB7I/ORB7I/ORB7I/ORB7I/ORB7I/OSTISTISTISTISTIRB7I/OSTIRB7I/OSTISTISTISTI </td <td></td> <td></td> <td>-</td> <td></td> <td></td>			-		
SDA I/O ST I ² C™ data I/O. RB1/AN10/INT1/SCK/ 22 I Digital I/O. RB1 I/O TTL Digital I/O. AN10 I Analog Analog input 10. INT1 I ST Synchronous serial clock input/output for SPI mode. SCL I/O ST Synchronous serial clock input/output for I ² C mode. RB2/AN8/INT2/VMO 23 I Analog input 8. RB2/AN8/INT2/VMO 1 ST External interrupt 2. VMO O TTL Digital I/O. AN8 I Analog Analog input 8. INT2 I ST External USB transceiver VMO output. RB3/AN9/CCP2/VPO 24 VIO TTL Digital I/O. AN9 I Analog Analog input 9. CCP2(1) VPO ST Capture 2 input/Compare 2 output/PWM 2 output. VPO 0 T External USB transceiver VPO output. External USB transceiver VPO output. VPO RB4/AN11/KBI0 25 T Digital I/O. Digital I/O. TL Interrupt-on-chang	FLT0		Ι		
RB1/AN10/INT1/SCK/ 22 Image: constraint of the system of the syste			•		
SCL RB1 AN10IIIDigital I/O. Analog Analog input 10.INT1 SCK SCLISTExternal interrupt 1.SCK SCLI/OSTSynchronous serial clock input/output for SPI mode.RB2/AN8/INT2/VMO23IRB2 AN8 INT2IAnalog Analog input 8.RB1 AN8 INT2ISTSCK SCLI/OTTLDigital I/O.AN8 INT2IAnalog Analog input 8.IN72 VMOISTExternal interrupt 2.VMOO-External USB transceiver VMO output.RB3/AN9/CCP2/VPO24 IRB3 AN9 CCP2 ⁽¹⁾ IAnalog I Analog Analog input 9.CCP2 ⁽¹⁾ VPOIAnalog I Analog I Analog Analog input 9.RB4/AN11/KBI0 KBI025 I-RB4/AN11/KBI0 KBI026 I-RB5/KB11/PGM PGM26 I-RB5/KB11/PGM RB6/KB12/PGC27 IIRB6/KB12/PGC RB6/KB12/PGC27 I-RB7/KB13/PGD RB7/KB13/PGD28 I-RB7/KB13/PGD RB7/KB13/PGD28 I-RB7 RB7 RGDITTL I TTL INTI/OTTL TL I TTL Interrupt-on-change pin. I TTL Interrupt-on-change pin. I TTL I Interrupt-on-change pin. I Cricuit Debugger and ICSP programming data pin.	SDA		I/O	ST	I ² C™ data I/O.
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AN10 I Analog input 10. INT1 I ST External interrupt 1. SCK I/O ST Synchronous serial clock input/output for SPI mode. SCL I/O ST Synchronous serial clock input/output for SPI mode. RB2 I/O ST Synchronous serial clock input/output for I ² C mode. RB2 I/O TTL Digital I/O. AN8 I Analog input 8. INT2 I ST External interrupt 2. VMO O - External USB transceiver VMO output. RB3/AN9/CCP2/VPO 24 - External USB transceiver VMO output. RB3/AN9/CCP2/VPO 24 - - RB3 I/O TTL Digital I/O. AN9 I Analog Analog input 9. CCP2 ⁽¹⁾ I/O ST Capture 2 input/Compare 2 output/PWM 2 output. VPO O - External USB transceiver VPO output. RB4/AN11/KBI0 25 - - RB5/KB11/PGM 26 - - RB6/KB1/PGC 27 <t< td=""><td></td><td></td><td>I/O</td><td>TTL</td><td>Digital I/O.</td></t<>			I/O	TTL	Digital I/O.
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RB2/AN8/INT2/VMO 23 V TTL Digital I/O. RB2 I/O TTL Digital I/O. Analog input 8. INT2 I ST External interrupt 2. VMO O — External USB transceiver VMO output. RB3/AN9/CCP2/VPO 24 — External USB transceiver VMO output. RB3 I/O TTL Digital I/O. AN9 I Analog input 9. CCP2 ⁽¹⁾ VPO O — External USB transceiver VPO output. VPO O — External USB transceiver VPO output. RB4/AN11/KBI0 25 — — RB4/AN11/KBI0 25 — — RB4 I/O TTL Digital I/O. AN11 I Analog Analog input 11. KBI0 I TTL Interrupt-on-change pin. RB5/KBI1/PGM 26 — — RB6/KBI2/PGC 27 — — RB6/KBI2/PGC 27 — — RB6/KBI2/PGC 1 TTL Interrupt-on-change			-		Synchronous serial clock input/output for SPI mode.
RB2 AN8I/OTTLDigital I/O. Analog input 8.INT2 VMOISTExternal interrupt 2.VMOO-External USB transceiver VMO output.RB3/AN9/CCP2/VPO24-RB3I/OTTLDigital I/O. Analog input 9.CCP2 ⁽¹⁾ VPOI/OAnalogAnalog input 9.CCP2 ⁽¹⁾ VPOI/OSTCapture 2 input/Compare 2 output/PWM 2 output.RB4/AN11/KBI025-RB4/AN11/KBI025-RB5 KB10I/OTTLDigital I/O. Analog input 11.RB5/KBI1/PGM26-RB5 KB11 PGMI/OTTLDigital I/O. ITTLRB6/KB12/PGC27-RB6 KB12 PGCI/OTTLDigital I/O. ITTLRB6/KB12/PGD28-RB7/KB13/PGD28-RB7/KB13/PGD28-RB7 KB13 PGDI/OTTLDigital I/O. ITTLRB7/KB13/PGD28-RB7 KB13 PGDI/OTTLDigital I/O. ITTLRB7 KB13 PGDI/OTTLDigital I/O. ITTLRB7 KB13 PGDI/OTTLDigital I/O. ITTLRB7 KB13 PGDI/OTTLDigital I/O. ITTLRB7 KB13 PGDI/OTTLDigital I/O. In-Circuit Debugger and ICSP programming data pin.			1/0	51	Synchronous senal clock input/output for I-C mode.
AN8 INT2IAnalogAnalog input 8.INT2 VMOISTExternal interrupt 2.VMOO—External USB transceiver VMO output.RB3/AN9/CCP2/VPO24—RB3II/OTTLAN9 CCP2 ⁽¹⁾ IAnalogAN9 VPOIAnalogRB4/AN11/KBI025—RB4 AN11 KBI0IAnalogAN11 KBI0IAnalogRB5/KBI1/PGM26—RB5 KB11 PGMI/OTTLDigital I/O. KB11 PGMITTL PGCI/ORB6/KBI2/PGC27RB6 KB13/PGDI/ORB7/KBI3/PGD28RB7 KB13 PGDITTL KB13 PGDI/OTTL KB13 PGDIITTL TTL Digital I/O.RB7/KBI3/PGD28IIRB7 KB13 PGDIITTL TTL IITTL Digital I/O.RB7 KB13 PGDIITTL TTL Digital I/O.RB7 KB13 PGDII/OTTL TTL Digital I/O.RB7 KB13 PGDII/OTTL TTL Digital I/O.RB7 KB13 PGDII/OTTL TTL Digital I/O.RB7 KB13 PGDII/OTTL TTL Digital I/O.RB7 KB13 PGDII/OTTL TTL Digital I/O.R		23	1/0	דדו	
INT2 VMOISTExternal interrupt 2.VMO0External USB transceiver VMO output.RB3/AN9/CCP2/VPO24-RB3I/OTTLDigital I/O.AN9IAnalogCCP2 ⁽¹⁾ V/OSTCCP2 ⁽¹⁾ OExternal USB transceiver VPO output.VPOOORB4AN11/KBIO25RB4IAN11IAnalogAN11IKBIORB5/KBI1/PGM26RB5I/OTTLDigital I/O.RB6/KBI2/PGC27RB6/KBI2/PGC27RB6/KBI2/PGC27RB6/KBI2/PGC1TTLInterrupt-on-change pin.PGCI/OTTLDigital I/O.RB7/KBI3/PGD28RB7I/ORB7/KBI3/PGD28RB7I/ORB7I/ORB7I/OSTLDigital I/O.RB7/KBI3/PGD28RB7I/ORB7I/OSTLDigital I/O.RB7I/ORB7I/ORB7I/OSTLDigital I/O.RB7I/OSTLDigital I/O.RB7I/OSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.I/OS					
VMOOExternal USB transceiver VMO output.RB3/AN9/CCP2/VPO24-RB3I/OTTLDigital I/O.AN9IAnalogAnalog input 9.CCP2 ⁽¹⁾ OSTCapture 2 input/Compare 2 output/PWM 2 output.VPOOExternal USB transceiver VPO output.RB4/AN11/KBI025-RB4I/OTTLDigital I/O.AN11IAnalogKBI0ITTLDigital I/O.RB5/KBI1/PGM26-RB6/KBI2/PGC27-RB6/KBI2/PGC27-RB6/KBI2/PGCITTLNB6/KBI3/PGD28-RB7I/OTTLDigital I/O.RB7/KBI3/PGD28-RB7I/OTTLDigital I/O.RB7I/OTTLInterrupt-on-change pin.PGDI/OTTLDigital I/O.RB7I/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDI/OTTLInterrupt-o				-	
RB3 AN9 CCP2(1) VPOI/OTTLDigital I/O. Analog input 9. Capture 2 input/Compare 2 output/PWM 2 output. Capture 2 input/Compare 2 output/PWM 2 output. External USB transceiver VPO output.RB4/AN11/KBI025	VMO		0		
AN9 CCP2(1) VPOIAnalog I/OAnalog input 9. Capture 2 input/Compare 2 output/PWM 2 output.RB4/AN11/KBI025Capture 2 input/Compare 2 output/PWM 2 output.RB4/AN11/KBI025External USB transceiver VPO output.RB4I/OTTLDigital I/O.AN11IAnalog Analog input 11.KBI0ITTLInterrupt-on-change pin.RB5/KBI1/PGM26IRB5I/OTTLDigital I/O.KB11ITTLInterrupt-on-change pin.PGMI/OSTLow-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6I/OTTLDigital I/O.KB12ITTLInterrupt-on-change pin.PGCI/OTTLDigital I/O.RB7/KBI3/PGD28IRB7I/OTTLDigital I/O.KB13I/OTTLDigital I/O.KB13 <tdi< td="">ITTLPGDI/OTTLNB7/KBI3/PGD28IRB7<tdi< td="">I/OTTLNB7/KBI3/PGDSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.I/OSTInterrupt-on-change pin.PGDI/OTTLInterrupt-on-change pin.PGDSTI/OTTLNB7/KBI3/PGDSTRB7I/OTTLNB7I/ORB7I/ORB7I/ONDI<td>RB3/AN9/CCP2/VPO</td><td>24</td><td></td><td></td><td></td></tdi<></tdi<>	RB3/AN9/CCP2/VPO	24			
CCP2(1) VPOI/OST OCapture 2 input/Compare 2 output/PWM 2 output. External USB transceiver VPO output.RB4/AN11/KBI025-RB4I/OTTLDigital I/O. Analog input 11. Interrupt-on-change pin.RB5/KBI1/PGM26-RB5I/OTTLDigital I/O. Interrupt-on-change pin.RB5/KBI1ITTLDigital I/O. Interrupt-on-change pin.PGMI/OTTLDigital I/O. Interrupt-on-change pin.RB6/KBI2/PGC27-RB6I/OTTLDigital I/O. Interrupt-on-change pin.RB6/KBI2/PGC27-RB6I/OTTLDigital I/O. Interrupt-on-change pin.RB6/KBI2/PGC27-RB7I/OTTLDigital I/O. In-Circuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28-RB7I/OTTLDigital I/O. In-Circuit Debugger and ICSP programming data pin.PGDI/OSTIn-Circuit Debugger and ICSP programming data pin.	RB3		I/O	TTL	Digital I/O.
VPOO—External USB transceiver VPO output.RB4/AN11/KBI025–RB4I/OTTLDigital I/O.AN11IAnalogKBI0ITTLInterrupt-on-change pin.RB5/KBI1/PGM26–RB5I/OTTLDigital I/O.RB5I/OTTLDigital I/O.RB5I/OTTLDigital I/O.RB6I/OTTLDigital I/O.RB6/KBI2/PGC27–RB6I/OTTLDigital I/O.RB6/KBI2/PGC27–RB6I/OTTLDigital I/O.RB6/KBI2/PGC27–RB6I/OTTLDigital I/O.RB7/KBI3/PGD28–RB7I/OTTLDigital I/O.RB7I/OTTLDigital I/O.RB7I/OTTLDigital I/O.KBI3IITTLPGDI/OSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.					
RB4/AN11/KBI025I/OTTLDigital I/O.RB4II/OTTLDigital I/O.AN11IAnalogAnalog input 11.KBI0ITTLInterrupt-on-change pin.RB5/KBI1/PGM26IRB5I/OTTLDigital I/O.KB10ITTLDigital I/O.RB5I/OTTLDigital I/O.KB11ITTLInterrupt-on-change pin.PGMI/OSTLow-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6I/OTTLDigital I/O.KB12II/OSTPGCI/OSTInterrupt-on-change pin.RB7/KBI3/PGD28IIRB7I/OTTLDigital I/O.KB13IITTLPGDI/OSTI/OSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.RB7I/OSTInterrupt-on-change pin.PGDII/OTTLDigital I/O.KB13IITTLInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.INCITTLInterrupt-on-change pin.PGDII/OSTInterrupt-on-change pin.				ST	
RB4 AN11 KBI0I/OTTLDigital I/O.AN11 KBI0IIAnalog TTLAnalog input 11. Interrupt-on-change pin.RB5/KBI1/PGM26IRB5 KB1 PGMII/OTTLDigital I/O. IITTLRB6/KBI2/PGC27RB6 KB12 PGCI/OTTLRB6/KBI2/PGC27RB6 KB12 PGCI/ORB7/KBI3/PGD28RB7 KB13 PGDI/OTTLI/OI/OTTLI/OTTLDigital I/O. STRB7 KB13 PGDI/OI/OTTLI/OTTLI/OTTLI/OSTRB7 KB13I/OI/OTTLI/OSTI/OTTLI/OSTI/OTTLDigital I/O. IRB7 KB13I/OTTLI/OSTI/OTTLI/OSTI/OTTLDigital I/O. IKB13 PGDII/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OSTI/OS			0	—	External USB transceiver VPO output.
AN11 KBI0IAnalog IAnalog TTLAnalog input 11. Interrupt-on-change pin.RB5/KBI1/PGM26IIRB5I/OTTLDigital I/O. IKB1ITTLInterrupt-on-change pin. I/OPGMITTLInterrupt-on-change pin. I/ORB6/KBI2/PGC27IRB6I/OTTLDigital I/O. Low-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6I/OTTLDigital I/O. Interrupt-on-change pin. Incircuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IIIRB7I/OTTLDigital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.PGDIIVOSTInterrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.		25		TT 1	Digital I/O
KBI0ITTLInterrupt-on-change pin.RB5/KBI1/PGM26I/OTTLDigital I/O.RB5I/OTTLI Digital I/O.KBI1IITTLInterrupt-on-change pin.PGMI/OSTLow-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6I/OTTLDigital I/O.KBI2ITTLInterrupt-on-change pin.PGCI/OSTInterrupt-on-change pin.PGCI/OTTLInterrupt-on-change pin.RB7/KBI3/PGD28I/OTTLRB7I/OTTLDigital I/O.KBI3IITTLPGDI/OSTInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.					
RB5/KBI1/PGM RB526I/OTTLDigital I/O.RB5I/OTTLInterrupt-on-change pin.PGMITTLInterrupt-on-change pin.PGMI/OSTLow-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6I/OTTLDigital I/O.KBI2ITTLInterrupt-on-change pin.PGCI/OSTInterrupt-on-change pin.PGCI/OSTIncircuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IRB7I/OTTLDigital I/O.KBI3IITTLPGDI/OSTI/OSTIncircuit Debugger and ICSP programming data pin.			-	•	
RB5 KBI1 PGMI/OTTLDigital I/O. Interrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27-RB6 KBI2 PGC1/OTTLDigital I/O. I TTLRB7 KBI3 PGD28-I/OTTLInterrupt-on-change pin. I TTLI/OSTInterrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.		26			······································
KBI1 PGMITTLInterrupt-on-change pin. Low-Voltage ICSP™ Programming enable pin.RB6/KBI2/PGC27IRB6 KBI2 PGCI/OTTLDigital I/O. I TTLPGCI/OTTLInterrupt-on-change pin. I TTLPGCI/OSTInterrupt-on-change pin. In-Circuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IRB7 KBI3 PGDITTLI/OTTLDigital I/O. Interrupt-on-change pin. Interrupt-on-change pin.RB7 KBI3 PGDITTLI/OSTInterrupt-on-change pin. Interrupt-on-change pin.I/OSTInterrupt-on-change pin. Interrupt-on-change pin.		20	I/O	TTL	Digital I/O.
RB6/KBI2/PGC27I/OTTLDigital I/O.RB6I/OTTLDigital I/O.KB12ITTLInterrupt-on-change pin.PGCI/OSTIn-Circuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IRB7I/OTTLDigital I/O.KB13ITTLInterrupt-on-change pin.PGDI/OSTInterrupt-on-change pin.				TTL	Interrupt-on-change pin.
RB6 KBI2 PGCI/OTTLDigital I/O.PGCITTLInterrupt-on-change pin.RB7/KBI3/PGD28IRB7 KBI3 PGDI/OTTLDigital I/O.I/OTTLDigital I/O.I/OTTLDigital I/O.I/OTTLInterrupt-on-change pin.I/OTTLInterrupt-on-change pin.I/OSTInterrupt-on-change pin.I/OSTIncircuit Debugger and ICSP programming data pin.	PGM		I/O	ST	Low-Voltage ICSP™ Programming enable pin.
KBI2 PGCITTLInterrupt-on-change pin.PGCI/OSTIn-Circuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IRB7I/OTTLDigital I/O.KBI3ITTLInterrupt-on-change pin.PGDI/OSTIn-Circuit Debugger and ICSP programming data pin.	RB6/KBI2/PGC	27			
PGCI/OSTIn-Circuit Debugger and ICSP programming clock pin.RB7/KBI3/PGD28IRB7I/OTTLDigital I/O.KBI3ITTLInterrupt-on-change pin.PGDI/OSTIn-Circuit Debugger and ICSP programming data pin.					
RB7/KBI3/PGD 28 I/O TTL Digital I/O. RB7 I/O TTL Digital I/O. KBI3 I TTL Interrupt-on-change pin. PGD I/O ST In-Circuit Debugger and ICSP programming data pin.					
RB7I/OTTLDigital I/O.KBI3ITTLInterrupt-on-change pin.PGDI/OSTIn-Circuit Debugger and ICSP programming data pin.			1/0	51	In-Circuit Debugger and ICSP programming clock pin.
KBI3 I TTL Interrupt-on-change pin. PGD I/O ST In-Circuit Debugger and ICSP programming data pin.		28		TT 1	Digital I/O
PGD I/O ST In-Circuit Debugger and ICSP programming data pin.					
$L_{MUS} = L_{MUS} = L_{M$		I mpatible in			CMOS = CMOS compatible input or output

TABLE 1-2: PIC18F2458/2553 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

Pin Name	Pi	Pin Number			Buffer	Description
	PDIP	QFN	TQFP	Туре	Туре	Description
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI RC0	15	34	32	I/O	ST	Digital I/O.
T10S0				0		Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ UOE	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI CCP2 ⁽²⁾				 /O	CMOS ST	Timer1 oscillator input.
				0	51	Capture 2 input/Compare 2 output/PWM2 output. External USB transceiver OE output.
RC2/CCP1/P1A	17	36	36	Ŭ		
RC2		00	00	I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
P1A				0	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4					TTL	Digital input.
D- VM				I/O I	TTL	USB differential minus line (input/output). External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5	24	43	43	1	TTL	Digital input.
D+				I/O	_	USB differential plus line (input/output).
VP				Ι	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX CK				0 I/O	ST	EUSART asynchronous transmit. EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1	1/0	51	EUSART Synchronous clock (see RADT).
RC7	20	1		I/O	ST	Digital I/O.
RX				1	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO O — SPI data out.						
Legend: TTL = TTL o						CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels I = Input O = Output P = Power						
O = Output P = Power						

TABLE 1-3: PIC18F4458/4553 PINOUT I/O DESCRIPTIONS (CONTINUED)

O= OutputP= PowerNote 1:Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

2.0 **12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE**

The Analog-to-Digital (A/D) Converter module has 10 inputs for the 28-pin devices and 13 for the 40-pin and 44-pin devices. This module allows conversion of an analog input signal to a corresponding 12-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 2-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 2-2, configures the functions of the port pins. The ADCON2 register, shown in Register 2-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 2-1:	ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				
_	_	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON				
bit 7							bit 0				
Legend:											
R = Readab		W = Writable		•	mented bit, rea						
-n = Value a	it POR	'1' = Bit is set		'0' = Bit is cle	eared	x = Bit is unkn	own				
bit 7-6	Unimplemen	nted: Read as '	0'								
bit 5-2	CHS3:CHS0	: Analog Chanr	nel Select bits								
	0000 = Cha n	-									
	0001 = Chan	nel 1 (AN1)									
	0010 = Channel 2 (AN2)										
	0011 = Channel 3 (AN3)										
	0100 = Channel 4 (AN4)										
	$0101 = \text{Channel 5 (AN5)}^{(1,2)}$										
	0110 = Channel 6 (AN6) ^(1,2) 0111 = Channel 7 (AN7) ^(1,2)										
	$1111 = Channel 7 (AN7)^{(1)}$ 1000 = Channel 8 (AN8)										
	1001 = Channel 9 (AN9) 1010 = Channel 10 (AN10)										
	1010 = Channel 10 (AN10)										
		nel 12 AN12									
	1101 = Unim	plemented ⁽²⁾									
	1110 = Unim										
	1111 = Unim	•									
bit 1		VD Conversion	Status bit								
	When ADON										
		ersion in progr	ess								
	0 = A/D Idle										
bit 0	ADON: A/D (
	1 = A/D Converter module is enabled										
		/erter module is	haldesib s								

Performing a conversion on unimplemented channels will return a floating input measurement.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	_	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit (
Logondi							
Legend: R = Readab	le hit	W = Writable	hit	U = Unimpler	mented bit, read	1 as '0'	
-n = Value a		'1' = Bit is set		'0' = Bit is cle		x = Bit is unkr	nown
bit 7	ADFM: A/D R 1 = Right justi 0 = Left justifi		Select bit				
bit 6	•	eu ted: Read as '	o '				
bit 5-3	-	T0: A/D Acquis		loct hits			
	111 = 20 TAD 110 = 16 TAD 101 = 12 TAD 100 = 8 TAD 011 = 6 TAD 010 = 4 TAD 001 = 2 TAD 000 = 0 TAD ⁽¹))					
bit 2-0	111 = FRC (cl 110 = Fosc/6 101 = Fosc/1 100 = Fosc/4	6 ock derived fro 2	om A/D RC os	cillator) ⁽¹⁾			

REGISTER 2-3: ADCON2: A/D CONTROL REGISTER 2

Note 1: If the A/D FRC clock source is selected, a delay of one TcY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss), or the voltage level on the RA3/AN3/ VREF+ and RA2/AN2/VREF-/CVREF pins.

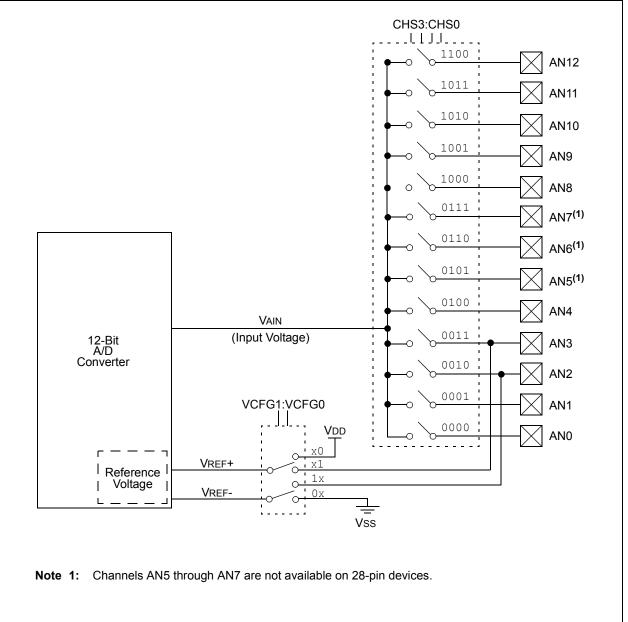
The A/D Converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the Converter, which generates the result via successive approximation.



A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D Converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and the A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 2-1.



2.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ADCS2:ADCS0 bits in ADCON2 should be updated in accordance with the clock source to be used. The ACQT2:ACQT0 bits do not need to be adjusted as the ADCS2:ADCS0 bits adjust the TAD time for the new clock speed. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits ACQT2:ACQT0 are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

2.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

- Note 1: When reading the PORT register, all pins configured as analog input channels will read as cleared (a low level). Analog conversion on pins configured as digital pins can be performed. The voltage on the pin will be accurately converted.
 - 2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.
 - The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG3:PCFG0 bits in ADCON1 are reset.

2.6 A/D Conversions

Figure 2-4 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT2:ACQT0 bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins.

Figure 2-5 shows the operation of the A/D Converter after the GO/DONE bit has been set and the ACQT2:ACQT0 bits are set to '010', and selecting a 4 TAD acquisition time before the conversion starts.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. This means the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is completed or aborted, a 2 TcY wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

Note:	The GO/DONE bit should NOT be set in
	the same instruction that turns on the A/D.
	Code should wait at least 2 µs after
	enabling the A/D before beginning an
	acquisition and conversion cycle.

2.7 Discharge

The discharge phase is used to initialize the value of the holding capacitor. The array is discharged before every sample. This feature helps to optimize the unity gain amplifier, as the circuit always needs to charge the capacitor array, rather than charge/discharge based on previous measure values.

FIGURE 2-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)

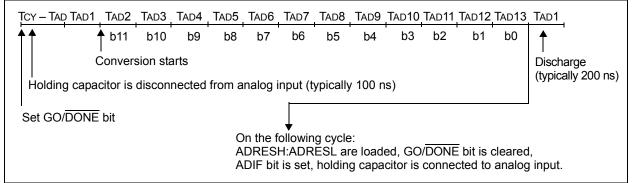
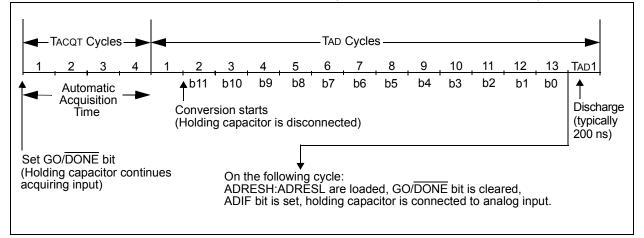


FIGURE 2-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



3.0 SPECIAL FEATURES OF THE CPU

Note:	For additional details on the Con-
	figuration bits, refer to the
	"PIC18F2455/2550/4455/4550 Data Sheet",
	Section 25.1 "Configuration Bits". Device
	ID information presented in this section is for
	PIC18F2458/2553/4458/4553 only.

PIC18F2458/2553/4458/4553 devices include several features intended to maximize reliability and minimize cost through elimination of external components. These include:

DEVICE IDs

Device ID Registers

TABLE 3-1:

3.1 Device ID Registers

The Device ID registers are "read-only" registers. They identify the device type and revision to device programmers, and can be read by firmware using table reads.

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
3FFFFEh	DEVID1	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	xxxx xxxx(1)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	xxxx xxxx(1)

Legend: x = unknown, u = unchanged

Note 1: See Register 3-1 and Register 3-2 for DEVID values. DEVID registers are read-only and cannot be programmed by the user.

4.0 ELECTRICAL CHARACTERISTICS

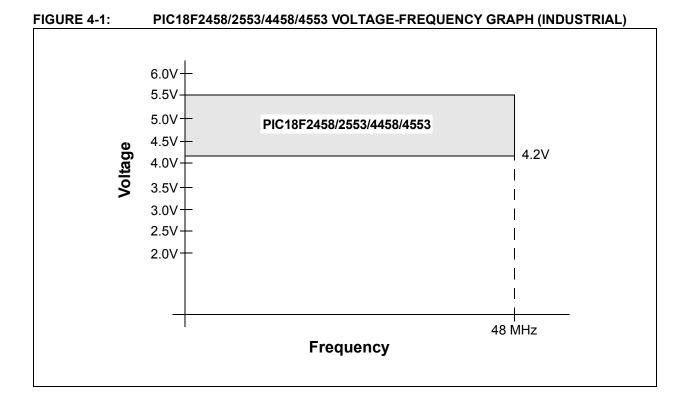
Absolute Maximum Ratings (†)

Ambient temperature under bias	40°C to +125°C
Storage temperature	65°C to +150°C
Voltage on any pin with respect to Vss (except VDD and MCLR)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +7.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, Iк (Vi < 0 or Vi > VDD)	±20 mA
Output clamp current, loк (Vo < 0 or Vo > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD $- \sum$ IOH} + \sum {(VDD - VOH) x IOH} + \sum (VOL x IOL)

2: Voltage spikes below Vss at the MCLR/VPP/RE3 pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR/VPP/ RE3 pin, rather than pulling this pin directly to Vss.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



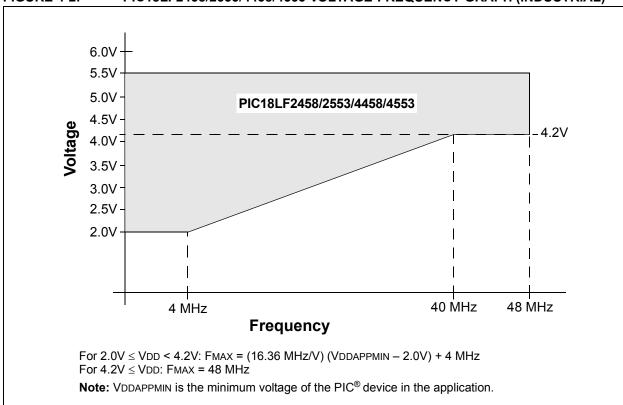


FIGURE 4-2: PIC18LF2458/2553/4458/4553 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

TABLE 4-1:A/D CONVERTER CHARACTERISTICS: PIC18F2458/2553/4458/4553 (INDUSTRIAL)PIC18LF2458/2553/4458/4553 (INDUSTRIAL)

Param No.	Sym	Characteristic	Min	Тур	Max	Units		Conditions
A01	NR	Resolution	-	—	12	bit		$\Delta V \text{REF} \geq 3.0 V$
A03	EIL	Integral Linearity Error	_	±1	±2.0	LSB	VDD = 3.0V	$\Delta VREF \ge 3.0V$
			_	_	±2.0	LSB	VDD = 5.0V	
A04	Edl	Differential Linearity Error	_	±1	+1.5/-1.0	LSB	VDD = 3.0V	$\Delta VREF \ge 3.0V$
			_		+1.5/-1.0	LSB	VDD = 5.0V	
A06	EOFF	Offset Error	_	±1	±5	LSB	VDD = 3.0V	$\Delta VREF \ge 3.0V$
			_		±3	LSB	VDD = 5.0V	
A07	Egn	Gain Error	_	±1	±1.25	LSB	VDD = 3.0V	$\Delta VREF \ge 3.0V$
			_	_	±2.00	LSB	VDD = 5.0V	
A10	_	Monotonicity	Guaranteed ⁽¹⁾			_		$VSS \leq VAIN \leq VREF$
A20	$\Delta VREF$	Reference Voltage Range (VREFH – VREFL)	3	—	Vdd – Vss	V		For 12-bit resolution
A21	Vrefh	Reference Voltage High	Vss + 3.0V		VDD + 0.3V	V		For 12-bit resolution
A22	Vrefl	Reference Voltage Low	Vss – 0.3V		VDD - 3.0V	V		For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL		VREFH	V		
A30	Zain	Recommended Impedance of Analog Voltage Source		—	2.5	kΩ		
A50	IREF	VREF Input Current ⁽²⁾		_	5 150	μΑ μΑ		During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

5.0 PACKAGING INFORMATION

For packaging information, see the *"PIC18F2455/2550/4455/4550 Data Sheet"* (DS39632).

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2007)

Original data sheet for the PIC18F2458/2553/4458/ 4553 devices.

Revision B (June 2007)

Changes to Figure 4-2: PIC18LF2458/2553/4458/4553 Voltage-Frequency Graph (Industrial).

Revision C (October 2009)

Removed "Preliminary" marking.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

Features	PIC18F2458	PIC18F2553	PIC18F4458	PIC18F4553	
Program Memory (Bytes)	24576	32768	24576	32768	
Program Memory (Instructions)	12288	16384	12288	16384	
Interrupt Sources	19	19	20	20	
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E	
Capture/Compare/PWM Modules	2	2	1	1	
Enhanced Capture/Compare/ PWM Modules	0	0	1	1	
Parallel Communications (SPP)	No	No	Yes	Yes	
12-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels	
Packages	28-Pin SPDIP 28-Pin SOIC	28-Pin SPDIP 28-Pin SOIC	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	40-Pin PDIP 44-Pin TQFP 44-Pin QFN	

TABLE B-1:DEVICE DIFFERENCES