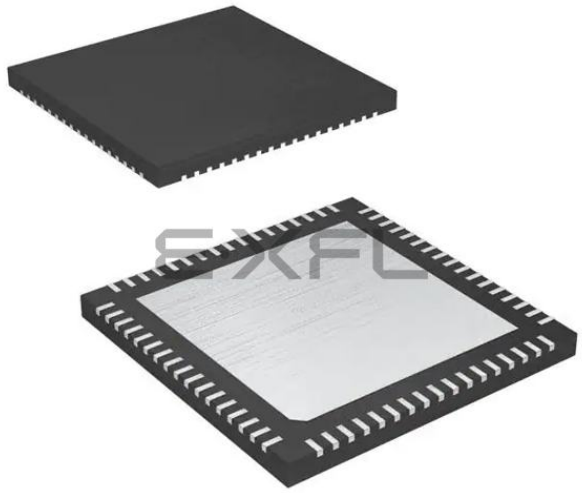

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1217f-68im-f

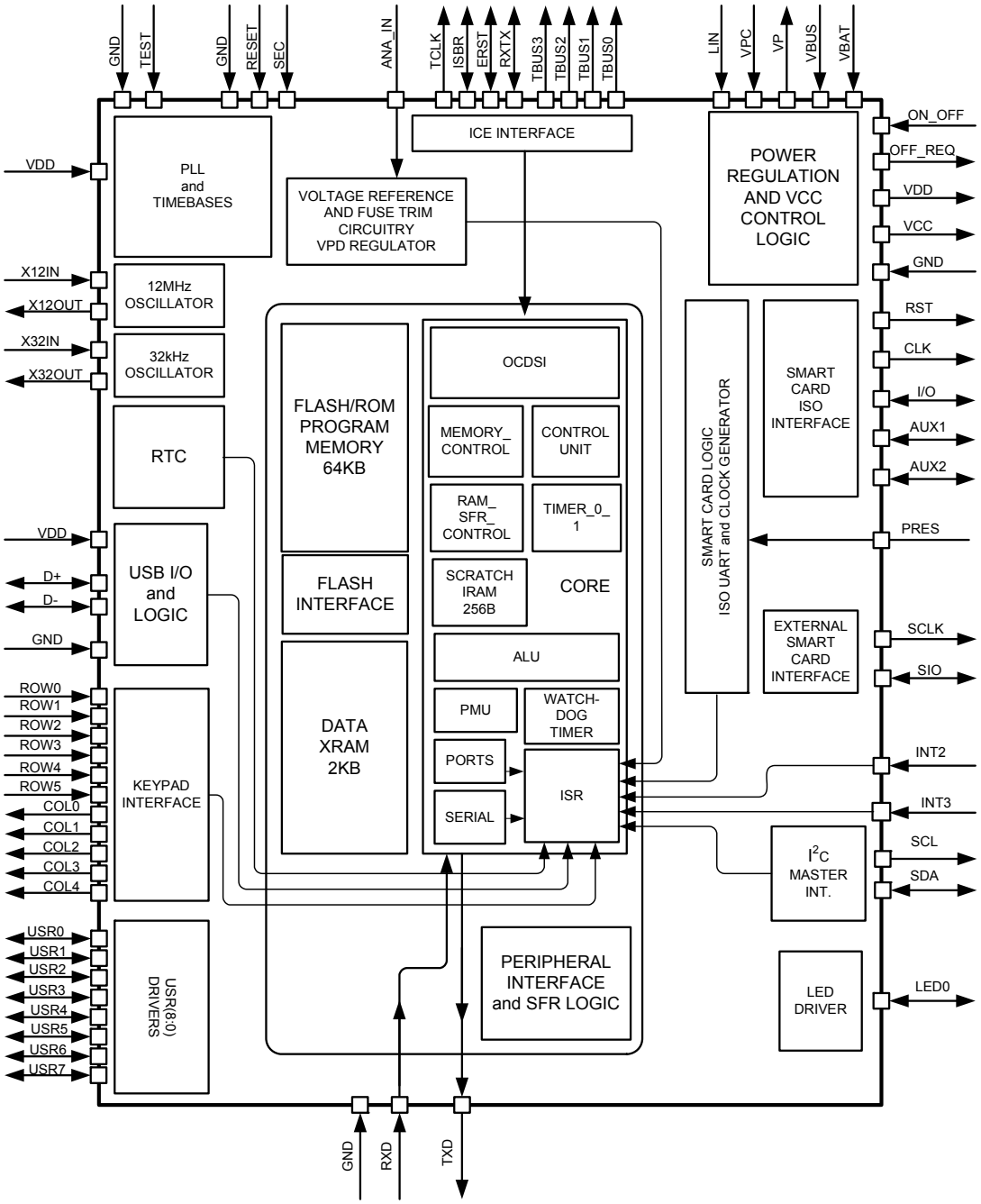

Figure 1: IC Functional Block Diagram

1 Hardware Description

1.1 Pin Description

Table 1: 73S1217 Pinout Description

Pin Name	Pin (68 QFN)	Type	Equivalent Circuit*	Description
X12IN	10	I	Figure 29	MPU/USB clock crystal oscillator input pin. A 12MHz crystal is required for USB operation. A 1MΩ resistor is required between pins X12IN and X12OUT.
X12OUT	11	O	Figure 29	MPU/USB clock crystal oscillator output pin.
X32IN	8	I	Figure 30	RTC clock crystal oscillator input pin. A 32768Hz crystal is required for low-power RTC operation.
X32OUT	7	O	Figure 30	RTC clock crystal oscillator output pin.
DP	26	IO	Figure 45	USB D+ IO pin, requires series 24Ω resistor.
DM	27	IO	Figure 45	USB D- IO pin, requires series 24Ω resistor.
ROW(5:0) 0 1 2 3 4 5	21 22 24 33 36 37	I	Figure 37	Keypad row input sense.
COL(4:0) 0 1 2 3 4	12 13 14 16 19	O	Figure 38	Keypad column output scan pins.
USR(7:0) 0 1 2 3 4 5 6 7	35 34 32 31 30 29 23 20	IO	Figure 33	General-purpose user pins, individually configurable as inputs or outputs or as external input interrupt ports.
SCL	5	O	Figure 32	I^2C (master mode) compatible Clock signal. Note: the pin is configured as an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
SDA	6	IO	Figure 31	I^2C (master mode) compatible data I/O. Note: this pin is bi-directional. When the pin is configured as output, it is an open drain output. When the I2C interface is being used, an external pull up resistor is required. A value of 3K is recommended.
RXD	17	I	Figure 35	Serial UART Receive data pin.
TXD	18	O	Figure 32	Serial UART Transmit data pin.

Table 5: Program Security Registers

Register	SFR Address	R/W	Description
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
TRIMPCtl	0xFFD1	W	0xA6 value will cause the selected fuse to be blown. All other values will stop the burning process.
FUSECtl	0xFFD2	W	0x54 value will set up for security fuse control. All other values are reserved and should not be used.
SECReg	0xFFD7	W	Bit 7 (PARAMSEC): 0 – Normal operation. 1 – Enable permanent programming of the security fuses.
		R	Bit 5 (SECPIN): Indicates the state of the SEC pin. The SEC pin is held low by a pull-down resistor. The user can force this pin high during boot sequence time to indicate to firmware that sec mode 1 is desired.
		R/W	Bit 1 (SECSET1): See the Program Security section.
		R/W	Bit 0 (SECSET0): See the Program Security section.

C4/C8 Data Direction Register (SCDIR): 0xFE0C – 0x00

This register determines the direction of the internal interface C4/C8 lines. After reset, all signals are tri-stated.

Table 91: The SCDIR Register

MSB							LSB
–	–	–	–	C8D	C4D	–	–

Bit	Symbol	Function
SCDIR.7	–	
SCDIR.6	–	
SCDIR.5	–	
SCDIR.4	–	
SCDIR.3	C8D	1 = input, 0 = output. Smart Card C8 direction.
SCDIR.2	C4D	1 = input, 0 = output. Smart Card C4 direction.
SCDIR.1	–	
SCDIR.0	–	

Parity Control Register (SParCtl): 0xFE11 ¯ 0x00

This register provides the ability to configure the parity circuitry on the smart card interface. The settings apply to both integrated smart card interfaces.

Table 95: The SParCtl Register

MSB							LSB
–	DISPAR	BRKGEN	BRKDET	RETRAN	DISCRX	INSPE	FORCPE

Bit	Symbol	Function
SParCtl.7	–	
SParCtl.6	DISPAR	Disable Parity Check – 1 = disabled, 0 = enabled. If enabled, the UART will check for even parity (the number of 1's including the parity bit is even) on every character. This also applies to the TS during ATR.
SParCtl.5	BRKGEN	Break Generation Disable – 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will generate a Break to the smart card if a parity error is detected on a receive character. No Break will be generated if parity checking is disabled. This also applies to TS during ATR.
SParCtl.4	BRKDET	Break Detection Disable – 1 = disabled, 0 = enabled. If enabled, and T=0 protocol, the UART will detect the generation of a Break by the smart card.
SParCtl.3	RETRAN	Retransmit Byte – 1 = enabled, 0 = disabled. If enabled and a Break is detected from the smart card (Break Detection must be enabled), the last character will be transmitted again. This bit applies to T=0 protocol.
SParCtl.2	DISCRX	Discard Received Byte – 1 = enabled, 0 = disabled. If enabled and a parity error is detected (Parity checking must be enabled), the last character received will be discarded. This bit applies to T=0 protocol.
SParCtl.1	INSPE	Insert Parity Error – 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will insert a parity error in every character transmitted by generating odd parity instead of even parity for the character.
SParCtl.0	FORCPE	Force Parity Error – 1 = enabled, 0 = disabled. Used for test purposes. If enabled, the UART will generate a parity error on a character received from the smart card.

FD Control Register (FDReg): 0xFE13 – 0x11

Table 97: The FDReg Register

MSB							LSB
FVAL.3	FVAL.2	FVAL.1	FVAL.0	DVAL.3	DVAL.2	DVAL.1	DVAL.0

Bit	Symbol	Function
FDReg.7	FVAL.3	Refer to Table 99. This value is converted per the table to set the divide ratio used to generate the baud rate (ETU). Default, also used for ATR, is 0001 (Fi = 372). This value is used by the selected interface.
FDReg.6	FVAL.2	
FDReg.5	FVAL.1	
FDReg.4	FVAL.0	
FDReg.3	DVAL.3	Refer to Table 99. This value is used to set the divide ratio used to generate the smart card CLK. Default, also used for ATR, is 0001 (Di = 1).
FDReg.2	DVAL.2	
FDReg.1	DVAL.1	
FDReg.0	DVAL.0	

This register uses the transmission factors F and D to set the ETU (baud) rate. The values in this register are mapped to the ISO 7816 conversion factors as described below. The CLK signal for each interface is created by dividing a high-frequency, intermediate signal (MSCLK) by 2. The ETU baud rate is created by dividing MSCLK by 2 times the Fi/Di ratio specified by the codes below. For example, if FI = 0001 and DI = 0001, the ratio of Fi/Di is 372/1. Thus, the ETU divider is configured to divide by 2 * 372 = 744. The maximum supported F/D ratio is 4096.

Table 98: Divider Ratios Provided by the ETU Counter

FI (code)	0000	0001	0010	0011	0100	0101	0110	0111
Fi (ratio)	372	372	558	744	1116	1488	1860	1860⊕
FCLK max	4	5	6	8	12	16	20	20⊕

FI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Fi(ratio)	512⊕	512	768	1024	1536	2048	2048⊕	2048⊕
FCLK max	5⊕	5	7.5	10	15	20	20⊕	20⊕

DI(code)	0000	0001	0010	0011	0100	0101	0110	0111
Di(ratio)	1⊕	1	2	4	8	16	32	32⊕

DI(code)	1000	1001	1010	1011	1100	1101	1110	1111
Di(ratio)	12	20	16⊕	16⊕	16⊕	16⊕	16⊕	16⊕

Note: values marked with ⊕ are not included in the ISO definition and arbitrary values have been assigned.

The values given below are used by the ETU divider to create the ETU clock. The entries that are not shaded will result in precise CLK/ETU per ISO requirements. Shaded areas are not precise but are within 1% of the target value.

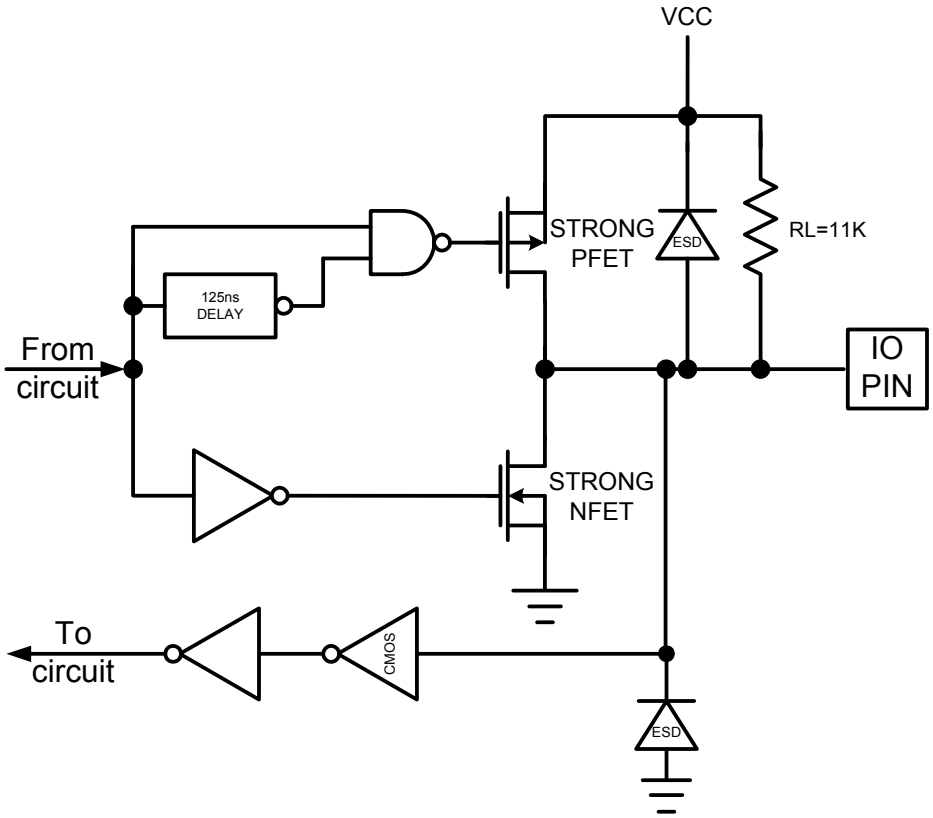

Figure 43: Smart Card I/O Circuit

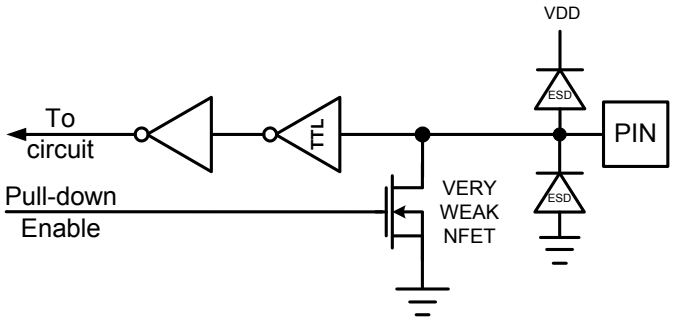

Figure 44: PRES Input Circuit

4.2 Packaging Information

68-Pin QFN Package Outline

Notes: 6.3mm x 6.3mm exposed pad area must remain UNCONNECTED (clear of PCB traces or vias). Controlling dimensions are in mm.

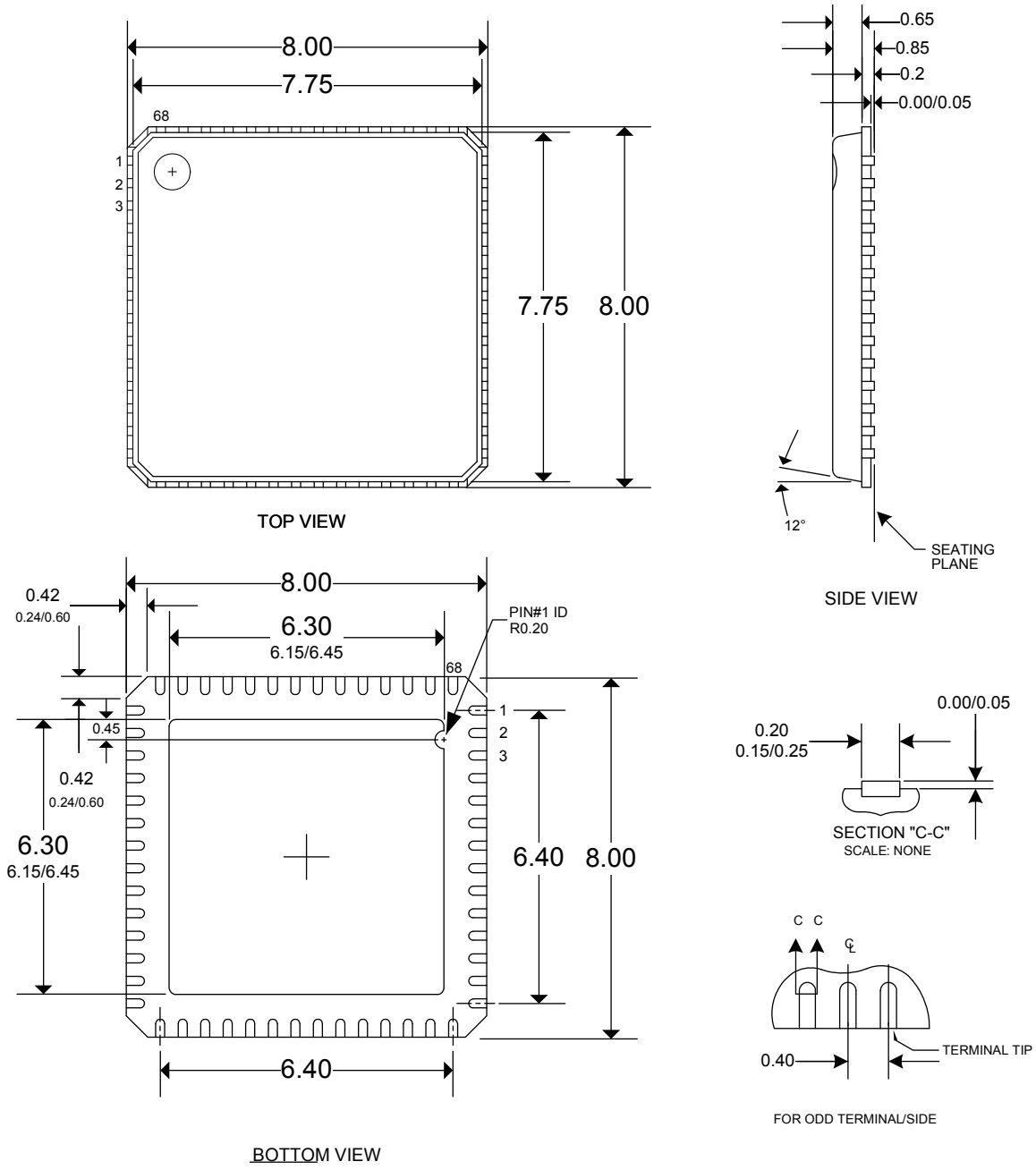

Figure 48: 73S1217F 68 QFN Mechanical Drawing