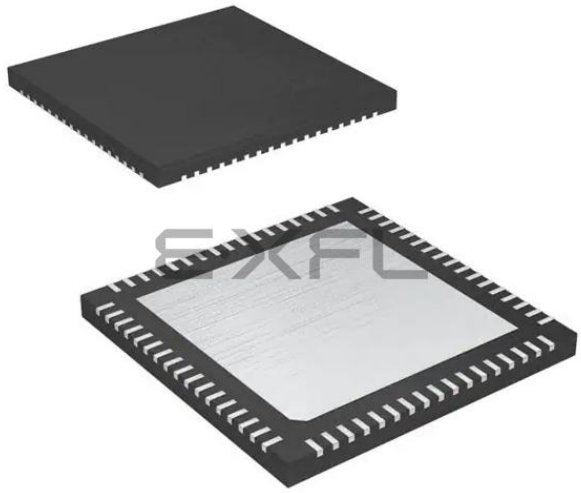
Analog Devices Inc./Maxim Integrated - 73S1217F-68IMR/F/P Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1217f-68imr-f-p

Table 5: Program Security Registers

Register	SFR Address	R/W	Description
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.
TRIMPCtl	0xFFD1	W	0xA6 value will cause the selected fuse to be blown. All other values will stop the burning process.
FUSECtl	0xFFD2	W	0x54 value will set up for security fuse control. All other values are reserved and should not be used.
SECReg	0xFFD7	W	Bit 7 (PARAMSEC): 0 – Normal operation. 1 – Enable permanent programming of the security fuses.
		R	Bit 5 (SECPIN): Indicates the state of the SEC pin. The SEC pin is held low by a pull-down resistor. The user can force this pin high during boot sequence time to indicate to firmware that sec mode 1 is desired.
		R/W	Bit 1 (SECSET1): See the Program Security section.
		R/W	Bit 0 (SECSET0): See the Program Security section.

1.5 Special Function Registers (SFRs)

The 1217 utilizes numerous SFRs to communicate with the many 1217 peripherals. This results in the need for more SFR locations outside the direct address IRAM space (0x80 to 0xFF). While some peripherals are mapped to unused IRAM SFR locations, additional SFRs for the USB, smart card and other peripheral functions are mapped to the top of the XRAM data space (0xFC00 to 0xFFFF).

1.5.1 Internal Data Special Function Registers (SFRs)

The Special Function Registers map is shown in Table 6.

Table 6: IRAM Special Function Registers Locations

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/ Hex
F8									FF
F0	B								F7
E8									EF
E0	A								E7
D8	BRCON								DF
D0	PSW	**KCOL**	**KROW**	**KSCAN**	**KSTAT**	**KSIZE**	**KORDERL**	**KORDERH**	D7
C8	T2CON								CF
C0	IRCON								C7
B8	IEN1	IP1	S0RELH	S1RELH					BF
B0			**FLSHCTL**					**PGADDR**	B7
A8	IEN0	IP0	S0RELL						AF
A0									A7
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL			9F
90	**USR70**	**UDIR70**	DPS		**ERASE**				97
88	TCON	TMOD	TL0	TL1	TH0	TH1		**MCLKCtl**	8F
80		SP	DPL	DPH	DPL1	DPH1	WDTREL	PCON	87

Only a few addresses are used, the others are not implemented. SFRs specific to the 73S1217F are shown in **bold** print (gray background). Any read access to unimplemented addresses will return undefined data, while most write access will have no effect. However, a few locations are reserved and not user configurable in the 73S1217F. **Writes to the unused SFR locations can affect the operation of the core and therefore must not be written to. This applies to all the SFR areas in both the IRAM and XRAM spaces. In addition, all unused bit locations within valid SFR registers must be left in their default (power on default) states.**

Program Status Word (PSW):

Table 9: PSW Register Flags

MSB							LSB
CV	AC	F0	RS1	RS	OV	–	P

Bit	Symbol	Function
PSW.7	CV	Carry flag.
PSW.6	AC	Auxiliary Carry flag for BCD operations.
PSW.5	F0	General purpose Flag 0 available for user.
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag.
PSW.1	F1	General purpose Flag 1 available for user.
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank Selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Register USR70. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 10) causes the corresponding pin to be at high level (3.3V), and writing a 0 causes the corresponding pin to be held at low level (GND). The data direction register UDIR70 define individual pins as input or output pins (see the User (USR) Ports section for details).

Table 10: Port Registers

Register	SFR Address	R/W	Description
USR70	0x90	R/W	Register for User port bits 7:0 read and write operations (pins USR0… USR7).
UDIR70	0x91	R/W	Data direction register for User port bits 0:7. Setting a bit to 0 means that the corresponding pin is an output.

All ports on the chip are bi-directional. Each consists of a Latch (SFR USR70), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

Table 17: The MCLKCtl Register

MSB							LSB
HSOEN	KBEN	SCEN	USBEN	32KEN	MCT.2	MCT.1	MCT.0

Bit	Symbol	Function
MCLKCtl.7	HSOEN	High-speed oscillator enable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. This bit is not changed when the PWRDN bit is set but the oscillator/VCO/PLL is disabled. The HSOEN bit should never be set under normal circumstances. Power down control should only be initiated via use of the PWRDN bit in MISCtl0.
MCLKCtl.6	KBEN	1 = Disable the keypad logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.5	SCEN	1 = Disable the smart card logic clock. This bit is not changed in PWRDN mode but the function is disabled. Interrupt logic for card insertion/removal remains operable even with smart card clock disabled.
MCLKCtl.4	USBEN	1 = Disable the USB logic clock. This bit is not changed in PWRDN mode but the function is disabled.
MCLKCtl.3	32KEN	1 = Disable the 32Khz oscillator. This function is not affected by PWRDN mode. **Note: This bit must be set if there is no 32KHz crystal. Some internal clocks and circuits will not run if the oscillator is enabled and no crystal is connected.**
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK = (MCount*2 + 4)*Fxtal. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

1.7.6 UART

The 80515 core of the 73S1217F includes two separate UARTs that can be programmed to communicate with a host. The 73S1217F can only connect one UART at a time since there is only one set of TX and Rx pins. The MISCtl0 register is used to select which UART is connected to the TX and RX pins. Each UART has a different set of operating modes that the user can select according to their needs. The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 115,200 bits/s. The TX and RX pins operate at the V_{DD} supply voltage levels and should never exceed 3.6V. The operation of each pin is as follows:

RX: Serial input data is applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first. The voltage applied at RX must not exceed 3.6V.

TX: This pin is used to output the serial data. The bytes are output LSB first.

The 73S1217F has several UART-related read/write registers. All UART transfers are programmable for parity enable, parity select, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 115200 bps. Table 47 shows the selectable UART operation modes and Table 48 shows how the baud rates are calculated.

Table 33: UART Modes

	UART 0	UART 1
Mode 0	N/A	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator)
Mode 1	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1)	Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator)
Mode 2	Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of f_{CKMPU}	N/A
Mode 3	Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1)	N/A

Note: Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1.8-bit serial modes with parity can be simulated by setting and reading the 9th bit, using the control bits S0CON3 and S1CON3 in the S0CON and S1CON SFRs.

Table 34: Baud Rate Generation

	Using Timer 1	Using Internal Baud Rate Generator
Serial Interface 0	$2^{smod} * f_{CKMPU}/ (384 * (256-TH1))$	$2^{smod} * f_{CKMPU}/(64 * (2^{10}-S0REL))$
Serial Interface 1	N/A	$f_{CKMPU}/(32 * (2^{10}-S1REL))$

Note: S0REL (9:0) and S1REL (9:0) are 10-bit values derived by combining bits from the respective timer reload registers SxRELH (bits 1:0) and SxRELL (bits 7:0). TH1 is the high byte of timer 1. The SMOD bit is located in the PCON SFR.

External Interrupt Control Register (INT6Ctl): 0xFF95 ← 0x00

Table 68: The INT6Ctl Register

MSB LSB

–	–	VFTIEN	VFTINT	I2CIEN	I2CINT	ANIEN	ANINT

Bit	Symbol	Function
INT6Ctl.7	–	
INT6Ctl.6	–	
INT6Ctl.5	VFTIEN	VDD fault interrupt enable.
INT6Ctl.4	VFTINT	VDD fault interrupt flag.
INT6Ctl.3	I2CIEN	When set = 1, the I^2C interrupt is enabled.
INT6Ctl.2	I2CINT	When set =1, the I^2C transaction has completed. Cleared upon the start of a subsequent I^2C transaction.
INT6Ctl.1	ANIEN	Analog compare interrupt enable.
INT6Ctl.0	ANINT	Analog compare interrupt flag.

1.7.14 Keypad Interface

The 73S1217F supports a 30-button (6 row x 5 column) keypad (SPST Mechanical Contact Switches) interface using 11 dedicated I/O pins. Figure 13 shows a simplified block diagram of the keypad interface.

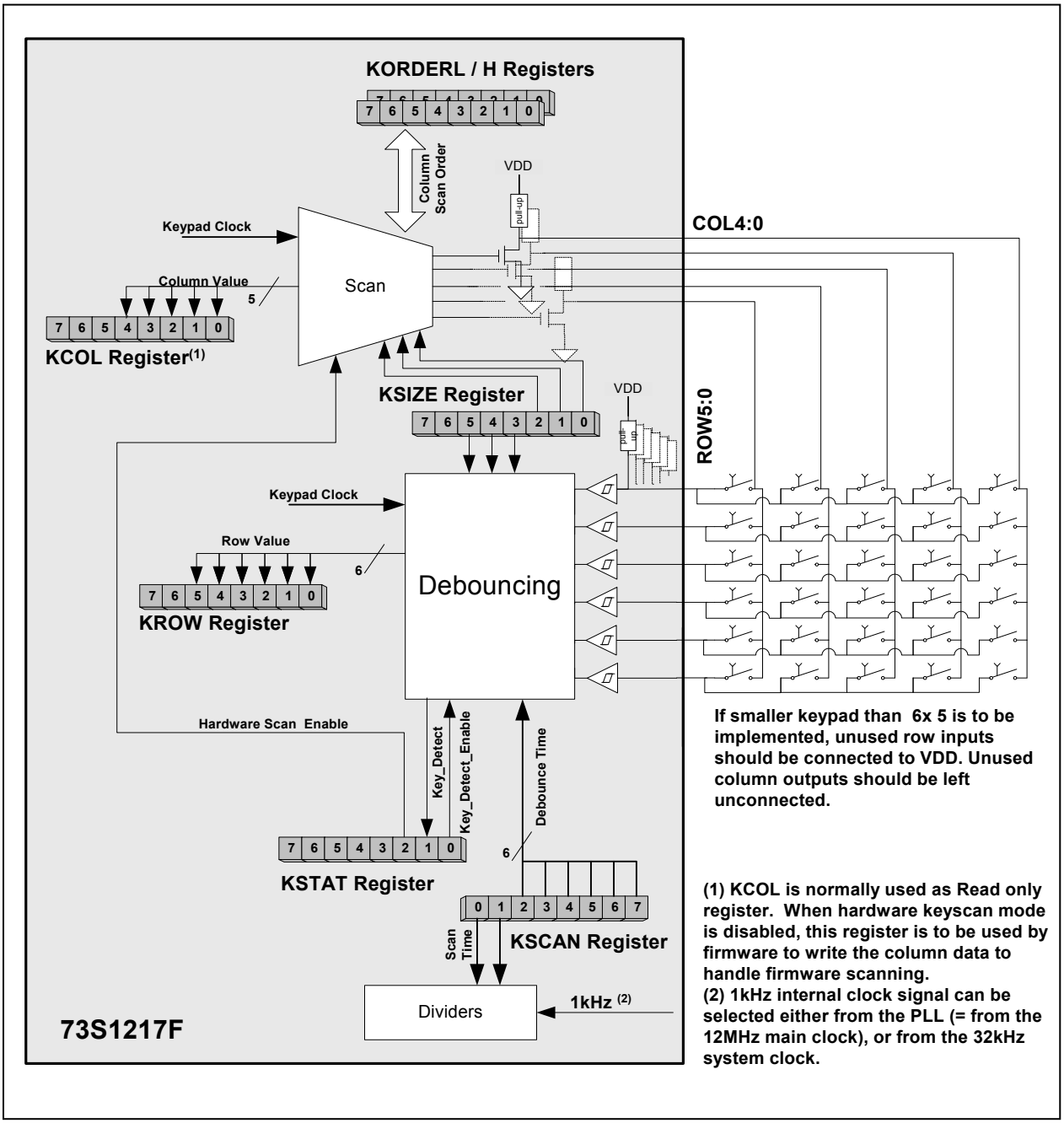


Figure 13: Simplified Keypad Block Diagram

There are five drive lines (outputs) corresponding to columns and six sense lines (inputs) corresponding to rows. Hysteresis and pull-ups are provided on all inputs (rows), which eliminate the need for external resistors in the keypad. Key scanning happens by asserting one of the 5 column lines low and looking for a low on a sense line indicating that a key is pressed (switch closed) at the intersection of the drive/sense (column/row) line in the keypad. Key detection is performed by hardware with an incorporated debounce timer. Debouncing time is adjustable through the KSCAN register. Internal hardware circuitry performs

decoding, handshake packet generation, Data0/Data1 toggle synchronization, bit stuffing, bus idle detection and other protocol generation/checking required in Chapter 8 of the USB specification.

The firmware is responsible for servicing and building the messages required under Chapter 9 of the USB specification. Device configuration is stored in the firmware. Data received from the USB port is stored in the appropriate IN FIFO that is read by the firmware and processed. The messages to be sent back to the USB host are generated by firmware and placed back into the appropriate OUT FIFO. Stall/NAK handshakes are generated as appropriate if the RAM is not available for another message from the USB host. Suspend and resume modes are supported. All register/FIFO spaces are located in Data Memory space. The FIFOs are dedicated for USB storage and are unused in a configuration that is not using USB. All registers in the USB interface are located in external data memory address (XRAM) space starting at address FC00'h.

1.7.16.1 USB Interface Implementation

The 73S1217F Application Programming Interface includes some dedicated software commands to configure the USB interface, to get a status of each USB Endpoint, to stall / unstall portions of the USB, and to send / receive data to / from each endpoint.

USB API entirely manages the USB circuitry, the USB registers and the FIFOs. Use of those commands facilitates USB implementation, without dealing with low-level programming.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 77: The MISCtl1 Register

MSB LSB

–	–	FRPEN	FLSH66	–	ANAPEN	USBPEN	USBCON

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable.
MISCtl1.4	FLSH66	Flash Read Pulse.
MISCtl1.3	–	
MISCtl1.2	ANAPEN	Analog power enable.
MISCtl1.1	USBPEN	0 = Enable the USB differential transceiver.
MISCtl1.0	USBCON	1 = Connect pull-up resistor from VDD to D+. If connected, the USB host will recognize the attachment of a USB device and begin enumeration.

Note: When using the USB on the 73S1217F, external 24Ω series resistors must be added to the D+ and D- signals to provide the proper impedance matching on these pins.

The USB peripheral block is not able to support read or write operations to the USB SFR registers when the MPU clock is running at MPU clock rates of 12MHz or greater. In order to properly communicate with the USB SFR registers when running at these speeds, wait states must be inserted when addressing the USB SFRs. The CKCON register allows wait states to be inserted when accessing these registers. The proper settings for the number of wait states are shown in **Error! Reference source not found.**.

When changing the MPU clock rate or the number of wait states, the USB connection must be inactive. If the USB is active, then it must be inactivated before changing the MPU clock or number of wait states. It can then be reconnected and re-enumerated. Changing these parameters while the USB interface is active may cause communication errors on the USB interface.

Clock Control Register (CKCON): 0x8E ← 0x01

Table 78: The CKCON Register

MSB LSB

–	–	–	–	–	CKWT.2	CKWT.1	CKWT.0

Bit	Symbol	Function
CKCON.7	–	
CKCON.6	–	
CKCON.5	–	
CKCON.4	–	
CKCON.3	–	
CKCON.2	CKWT.2	These three bits determine the number of wait states (machine cycles) to insert when accessing the USB SFRs: 000 = 0 (not to be used). 001 = 1 wait state. Use when MPU clock is <12MHz. 010 = 2 wait states. Use when MPU clock is between 12 and 16MHz. 011 = 3 wait states. Use when MPU clock is 24MHz. 100 = 4 wait states. 101 = 5 wait states. 110 = 6 wait states. 111 = 7 wait states.
CKCON.1	CKWT.1	
CKCON.0	CKWT.0	

The built-in ICC Interface has a linear regulator (V_{CC} generator) capable of driving 1.8, 3.0 and 5.0V smart cards in accordance with the ISO 7816-3 and EMV4.0 standards. This converter uses the V_P (5.5V nominal) input supply source. See the power supply management section above for more detail. Auxiliary I/O lines C4 and C8 are only provided for the built-in interface. If support for the auxiliary lines is necessary for the external smart card interface, they need to be handled manually through the USR GPIO pins. The external 73S8010x devices directly connect the I/O (SIO) and clock (SCLK) signals and control is handled via the I^2C interface.

Figure 17 shows how multiple 73S8010x devices can be connected to the 73S1217F.

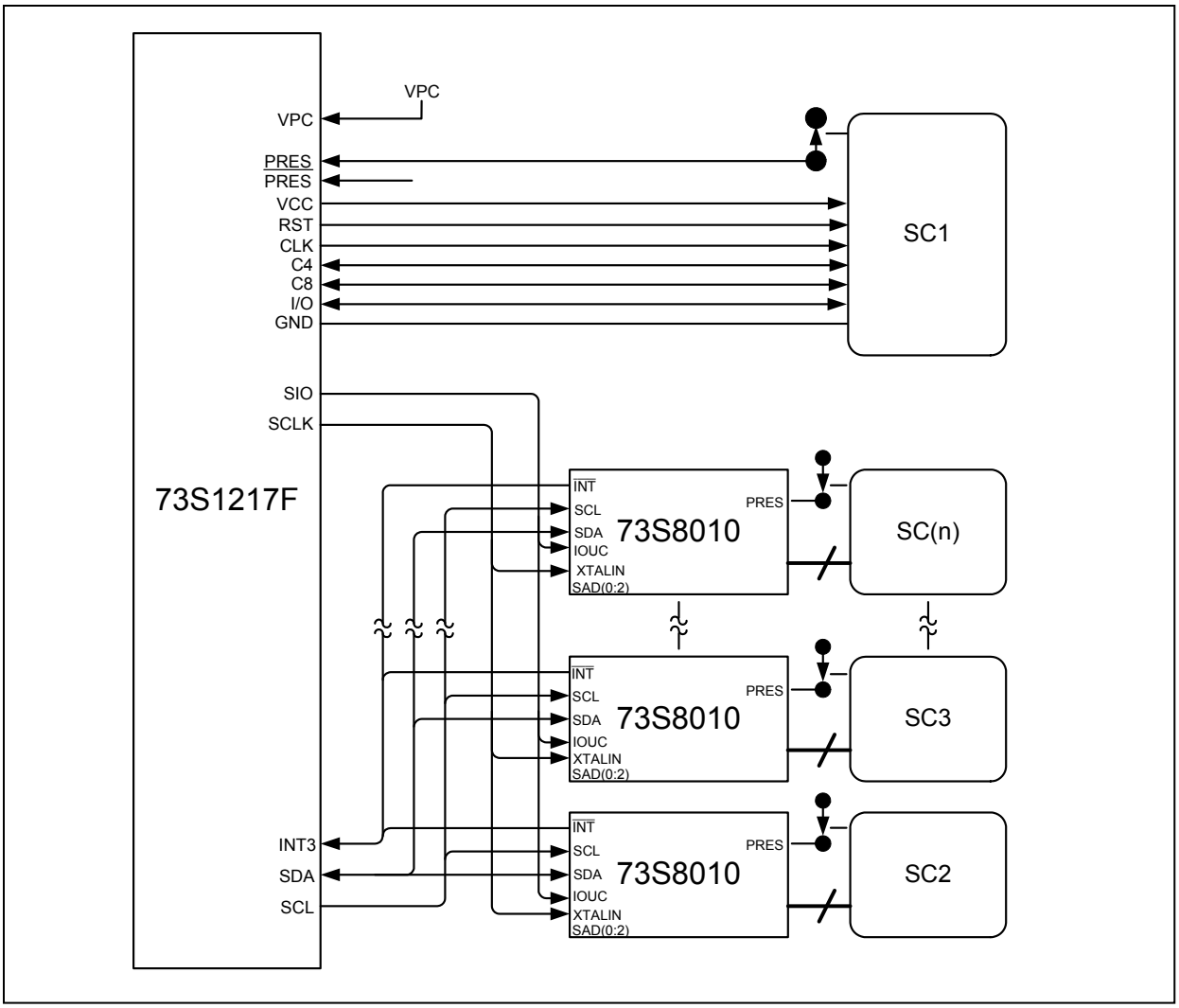
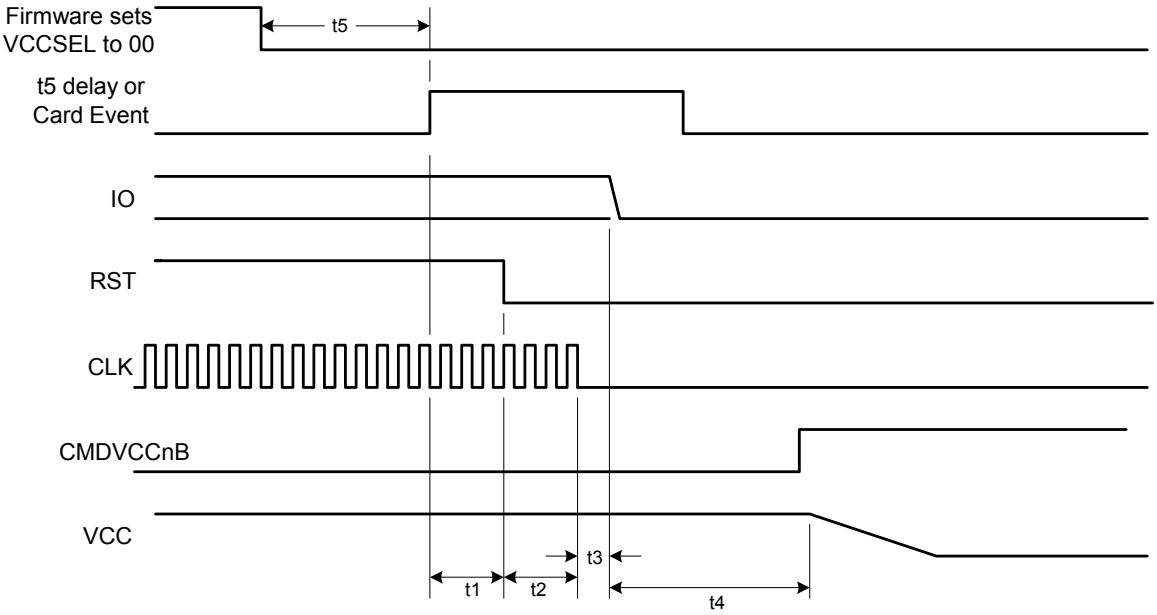


Figure 17: Smart Card Interface Block Diagram



t1: Time after either a “card event” occurs or firmware sets the VCCSela and VCCSelb bits to 0 (see t5, VCCOff_tmr) occurs until RST is asserted low.

t2: Time after RST goes low until CLK stops.

t3: Time after CLK stops until IO goes low.

t4: Time after IO goes low until VCC is powered down.

t5: Delayed VCC off time (in ETUs per VCCOff_tmr bits). Only in effect due to firmware deactivation.

Figure 19: Deactivation Sequence

1.7.17.3 Data Reception/Transmission

When a 12Mhz crystal is used, the smart card UART will generate a 3.69Mhz (default) clock to both smart card interfaces. This will allow approximately 9600bps (1/ETU) communication during ATR (ISO 7816 default). As part of the PPS negotiation between the smart card and the reader, the firmware may determine that the smart card parameters F and D may be changed. After this negotiation, the firmware may change the ETU by writing to the SFR FDReg to adjust the ETU and CLK. The firmware may also change the smart card clock frequency by writing to the SFR SCCLK (SCECLK for external interface). Independent clock frequency control is provided to each smart card interface. Clock stop high or Clock stop low is supported in asynchronous mode. Figure 20 shows the ETU and CLK control circuits. The firmware determines when clock stop is supported by the smart card and when it is appropriate to go into that mode (and when to come out of it). The smart card UART is clocked by the same clock is provided to the selected smart card. The transition between smart card clocks is handled in hardware to eliminate any glitches for the UART during switchover. The external smart card clock is not affected when switching the UART to communicate with the internal smart card.

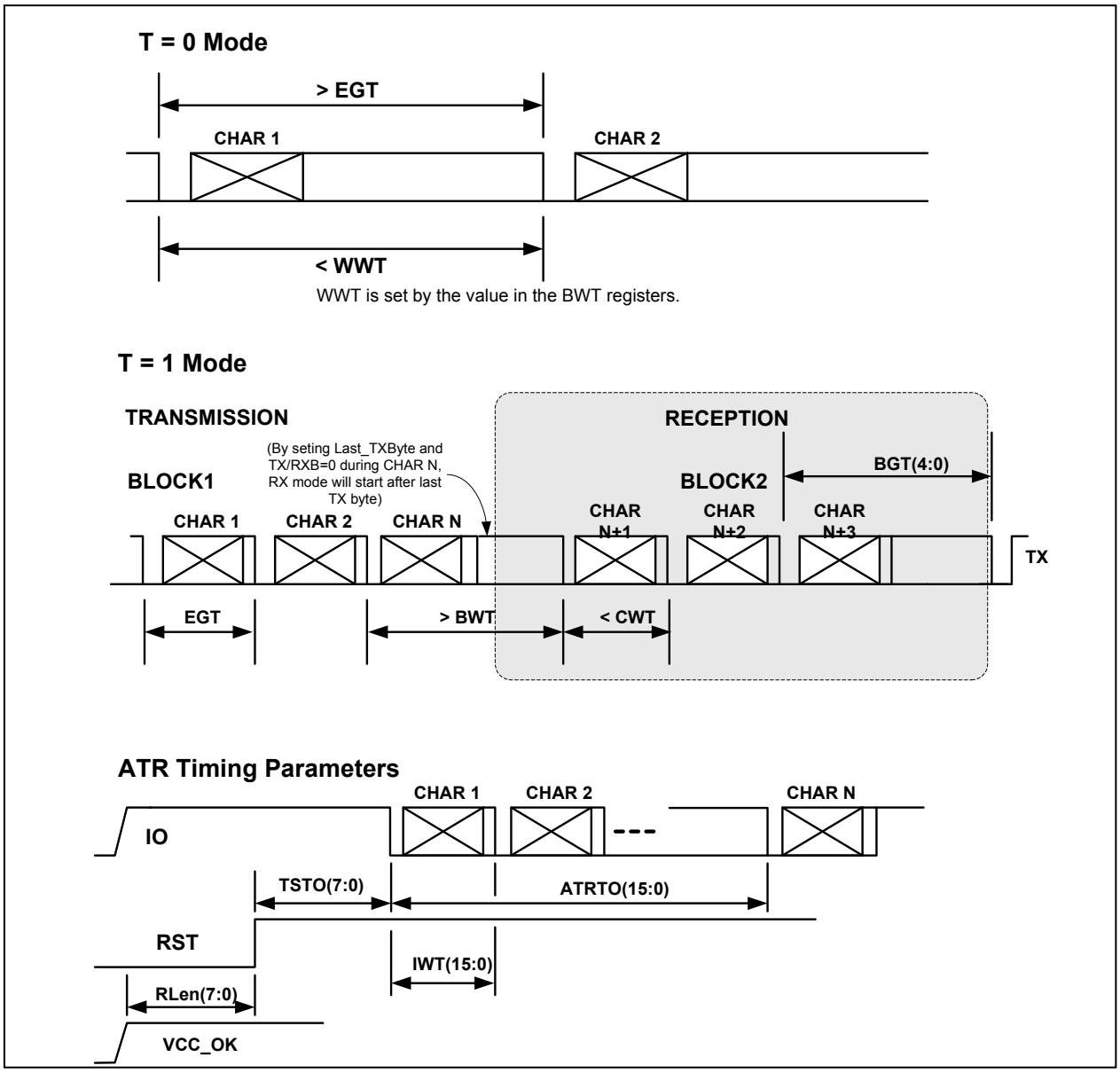


Figure 21: Guard, Block, Wait and ATR Time Definitions

1.7.17.4 Bypass Mode

It is possible to bypass the smart card UART in order for the firmware to support non-T=0/T=1 smart cards. This is called Bypass mode. In this mode the embedded firmware will communicate directly with the selected smart card and drive I/O during transmit and read I/O during receive in order to communicate with the smart card. In this mode, ATR processing is under firmware control. The firmware must sequence the interface signals as required. Firmware must perform TS processing, parity checking, break generation and CRC/LRC calculation (if required).

1.7.17.5 Synchronous Operation Mode

The 73S1217F supports synchronous operation. When sync mode is selected for either interface, the CLK signal is generated by the ETU counter. The values in FDReg, SCCLK, and SCECLK must be set to obtain the desired sync CLK rate. There is only one ETU counter and therefore, in sync mode, the interface must be selected to obtain a smart card clock signal. In sync mode, input data is sampled on the rise of CLK, and output data is changed on the fall of CLK.
Special Notes Regarding Synchronous Mode Operation

Smart Card Control Register (SCCtl): 0xFE0A ← 0x21

This register is used to monitor reception of data from the smart card.

Table 89: The SCCtl Register

MSB LSB

RSTCRD	–	IO	IOD	C8	C4	CLKLVL	CLKOFF

Bit	Symbol	Function
SCCtl.7	RSTCRD	1 = Asserts the RST (set RST = 0) to the smart card interface, 0 = De-assert the RST (set RST = 1) to the smart card interface. Can be used to extend RST to the smart card. Refer to the RLength register description. This bit is operational in all modes and can be used to extend RST during activation or perform a "Warm Reset" as required. In auto-sequence mode, this bit should be set = 0 to allow the sequencer to de-assert RST per the RLength parameters. In sync mode (see the SPrtcol register) the sense of this bit is non-inverted, if set =1 , RST = 1, if set = 0, RST = 0. Rlen has no effect on Reset in sync mode.
SCCtl.6	–	
SCCtl.5	IO	Smart Card I/O. Read is state of I/O signal (Caution, this signal is not synchronized to the MPU clock). In Bypass mode, write value is state of signal on I/O. In sync mode, this bit will contain the value of I/O pin on the latest rising edge of CLK.
SCCtl.4	IOD	Smart Card I/O Direction control Bypass mode or sync mode. 1 = input (default), 0 = output.
SCCtl.3	C8	Smart Card C8. When C8 is an output, the value written to this bit will appear on the C8 line. The value read when C8 is an output is the value stored in the register. When C8 is an input, the value read is the value on the C8 pin (Caution, this signal is not synchronized to the MPU clock). When C8 is an input, the value written will be stored in the register but not presented to the C8 pin.
SCCtl.2	C4	Smart Card C4. When C4 is an output, the value written to this bit will appear on the C4 line. The value read when C4 is an output is the value stored in the register. When C4 is an input, the value read is the value on the C4 pin (Caution, this signal is not synchronized to the MPU clock). When C4 is an input, the value written will be stored in the register but not presented to the C4 pin.
SCCtl.1	CLKLVL	1 = High, 0 = Low. If CLKOFF is set = 1, the CLK to smart card will be at the logic level indicated by this bit. If in bypass mode, this bit directly controls the state of CLK.
SCCtl.0	CLKOFF	0 = CLK is enabled. 1 = CLK is not enabled. When asserted, the CLK will stop at the level selected by CLKLVL. This bit has no effect if in bypass mode.

External Smart Card Control Register (SCECtl): 0xFE0B ← 0x00

This register is used to directly set and sample signals of External Smart Card interface. There are three modes of asynchronous operation, an "automatic sequence" mode, and bypass mode. Clock stop per the ISO 7816-3 interface is also supported but firmware must handle the protocol for SIO and SCLK for I^2C clock stop and start. Control for Reset (to make RST signal), activation control, voltage select, etc. should be handled via the I^2C interface when using external 73S73S8010x devices. USR(n) pins shall be used for C4, C8 functions if necessary.

Table 90: The SCECtl Register

MSB LSB

–	–	SIO	SIOD	–	–	SCLKLVL	SCLKOFF

Bit	Symbol	Function
SCECtl.7	–	
SCECtl.6	–	
SCECtl.5	SIO	External Smart Card I/O. Bit when read indicates state of pin SIO for SIOD = 1 (Caution, this signal is not synchronized to the MPU clock), when written, sets the state of pin SIO for SIOD = 0. Ignored if not in bypass or sync modes. In sync mode, this bit will contain the value of IO pin on the latest rising edge of SCLK.
SCECtl.4	SIOD	1 = input, 0 = output. External Smart Card I/O Direction control. Ignored if not in bypass or sync modes.
SCECtl.3	–	
SCECtl.2	–	
SCECtl.1	SCLKLVL	Sets the state of SCLK when disabled by SCLKOFF bit. If in bypass mode, this bit directly controls the state of SCLK.
SCECtl.0	SCLKOFF	0 = SCLK enabled, 1 = SCLK disabled. When disabled, SCLK level is determined by SCLKLVL. This bit has no effect if in bypass mode.

Table 99: Divider Values for the ETU Clock

	Fi code	0000	0001	0010	0011	0100	0101
Di code	F→ D↓	372	372	558	744	1116	1488
0001	1	744	744	1116	1488	2232	2976
0010	2	372	372	558	744	1116	1488
0011	4	186	186	279	372	558	744
0100	8	93	93	138	186	279	372
1000	12	62	62	93	124	186	248
0101	16	47	47	70	93	140	186
1001	20	37	37	56	74	112	149
0110	32	23	23	35	47	70	93

	Fi code	0110	1001	1010	1011	1100	1101
Di code	F→ D↓	1860	512	768	1024	1536	2048
0001	1	3720	1024	1536	2048	3072	4096
0010	2	1860	512	768	1024	1536	2048
0011	4	930	256	384	512	768	1024
0100	8	465	128	192	256	384	512
1000	12	310	85	128	171	256	341
0101	16	233	64	96	128	192	256
1001	20	186	51	77	102	154	205
0110	32	116	32	48	64	96	128

Block Wait Time Registers (BWTB0): 0xFE1B ← 0x00, (BWTB1): 0xFE1A ← 0x00, (BWTB2): 0xFE19 ← 0x00, (BWTB3): 0xFE18 ← 0x00

Table 104: The BWTB0 Register

MSB							LSB
BWT.7	BWT.6	BWT.5	BWT.4	BWT.3	BWT.1	BWT.2	BWT.0

Table 105: The BWTB1 Register

MSB							LSB
BWT.15	BWT.14	BWT.13	BWT.12	BWT.11	BWT.10	BWT.9	BWT.8

Table 106: The BWTB2 Register

MSB							LSB
BWT.23	BWT.22	BWT.21	BWT.20	BWT.19	BWT.18	BWT.17	BWT.16

Table 107: The BWTB3 Register

MSB							LSB
–	–	–	–	BWT.27	BWT.26	BWT.25	BWT.24

These registers (BWTB0, BWTB1, BWTB2, BWTB3) are used to set the Block Waiting Time(27:0) (BWT). All of these parameters define the maximum time the 73S1217F will have to wait for a character from the smart card. These registers serve a dual purpose. When T=1, these registers are used to set up the block wait time. The block wait time defines the time in ETUs between the beginning of the last character sent to smart card and the start bit of the first character received from smart card. It can be used to detect an unresponsive card and should be loaded by firmware prior to writing the last TX byte. When T = 0, these registers are used to set up the work wait time. The work wait time is defined as the time between the leading edge of two consecutive characters being sent to or from the card. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action. A Wait Time Extension (WTX) is supported with the 28-bit BWT.

Character Wait Time Registers (CWTB0): 0xFE1D ← 0x00, (CWTB1): 0xFE1C ← 0x00

Table 108: The CWTB0 Register

MSB							LSB
CWT.7	CWT.6	CWT.5	CWT.4	CWT.3	CWT.1	CWT.2	CWT.0

Table 109: The CWTB1 Register

MSB							LSB
CWT.15	CWT.14	CWT.13	CWT.12	CWT.11	CWT.10	CWT.9	CWT.8

These registers (CWTB0, CWTB1) are used to hold the Character Wait Time(15:0) (CWT) or Initial Waiting Time(15:0) (IWT) depending on the situation. Both the IWT and the CWT measure the time in ETUs between the leading edge of the start of the current character received from the smart card and the leading edge of the start of the next character received from the smart card. The only difference is the mode in which the card is operating. When T=1 these registers are used to configure the CWT and these registers configure the IWT when the ATR is being received. These registers should be loaded prior to receiving characters from the smart card. Firmware must manage which time is stored in the register. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action.

2 Application Schematics

2.1 Typical Application Schematic 1

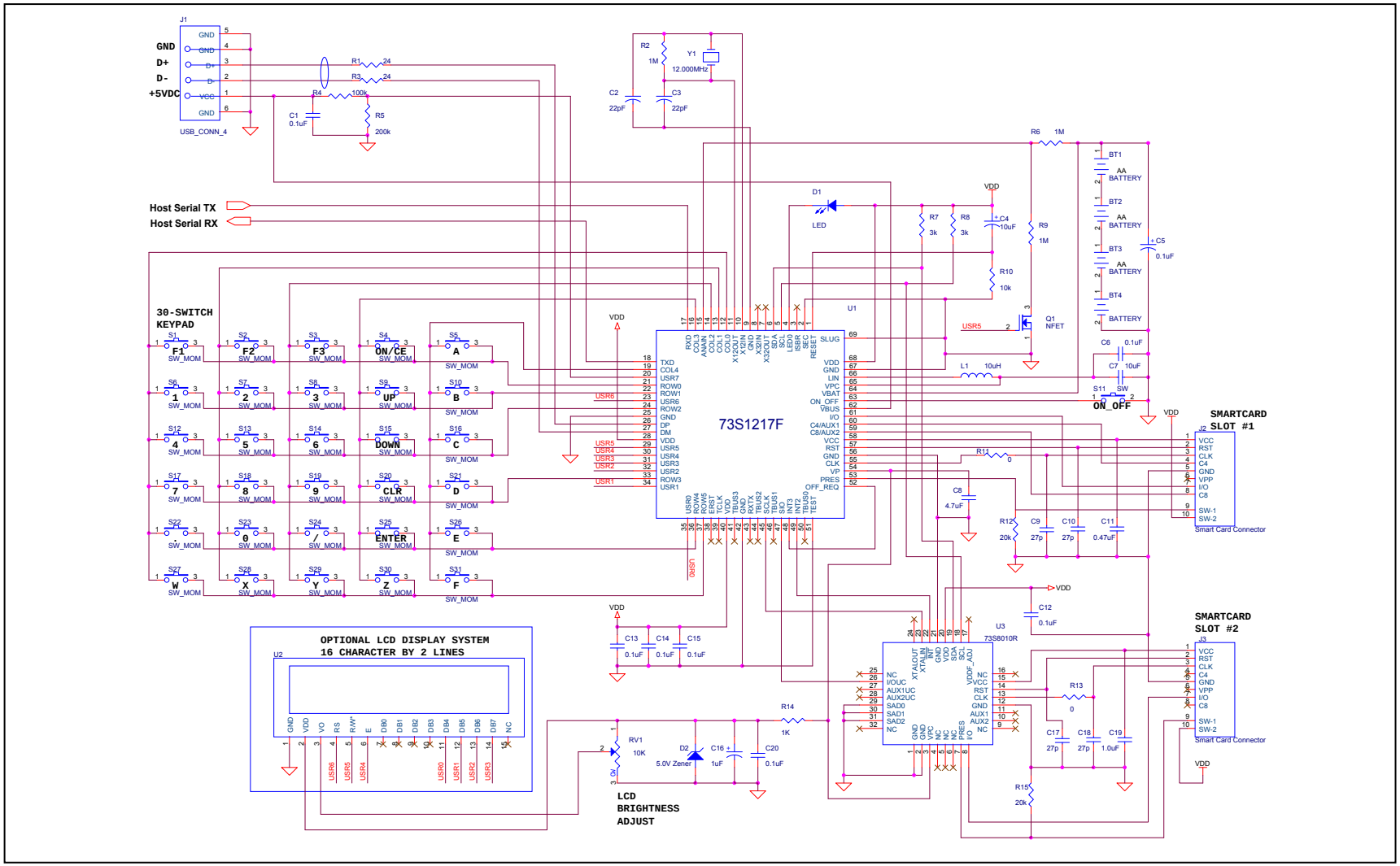


Figure 27: 73S1217F Typical Application Schematic (Handheld USB PINpad, with Combo USB-Bus and Self-powered Configuration)

2.2 Typical Application Schematic 2

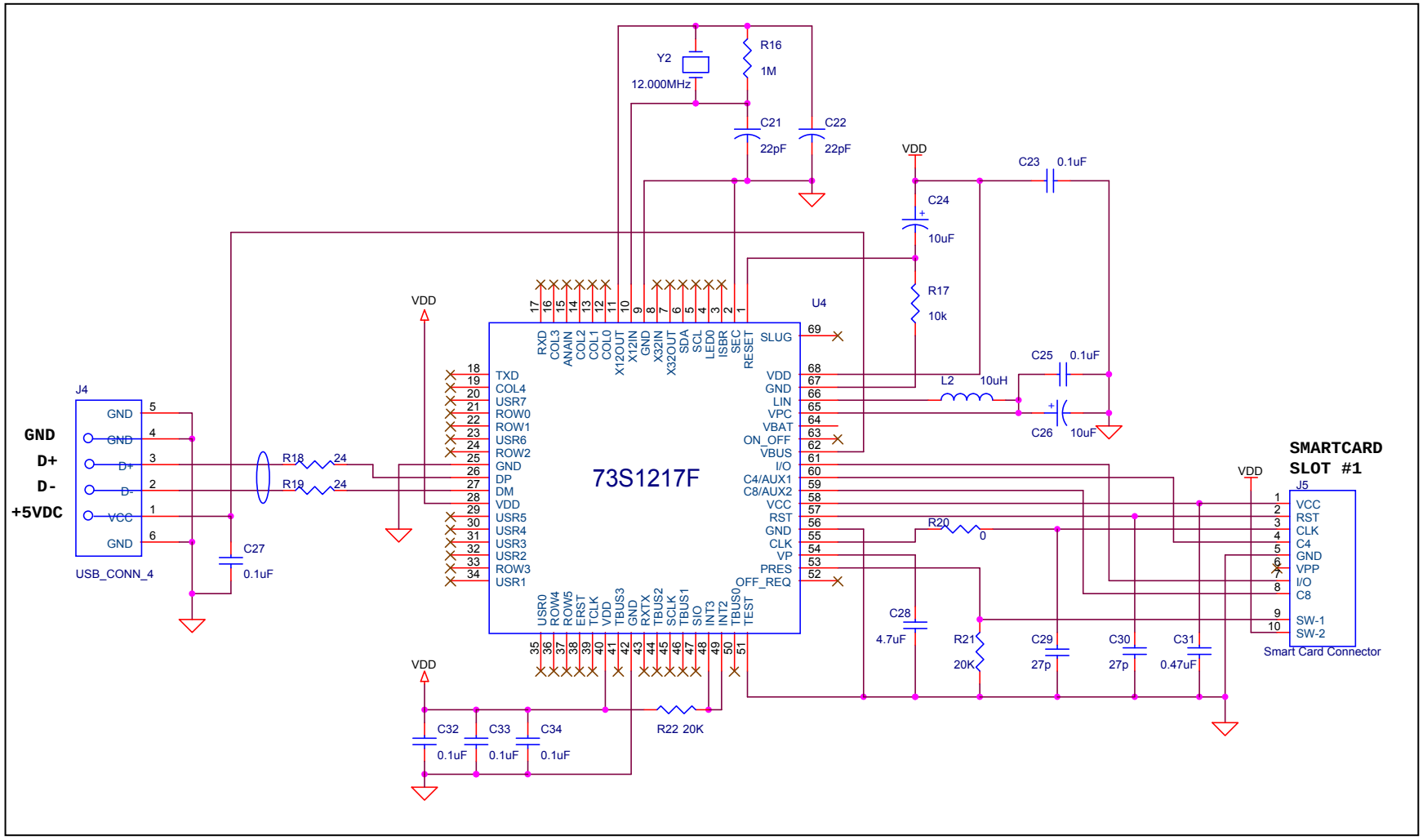


Figure 28: 73S1217F Typical Application Schematic (USB Transparent Reader and USB Key Configuration)

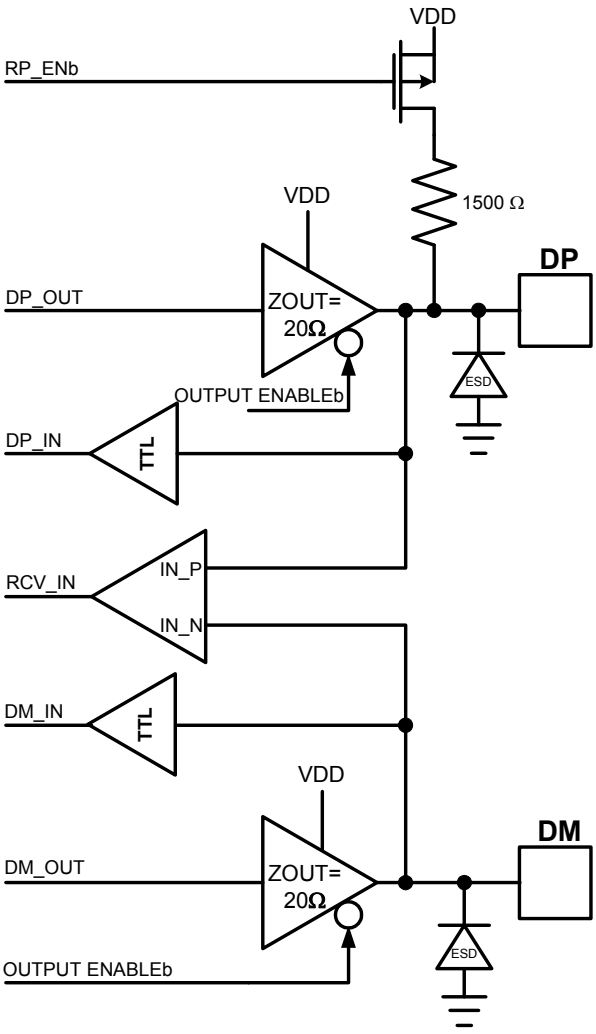


Figure 45: USB Circuit

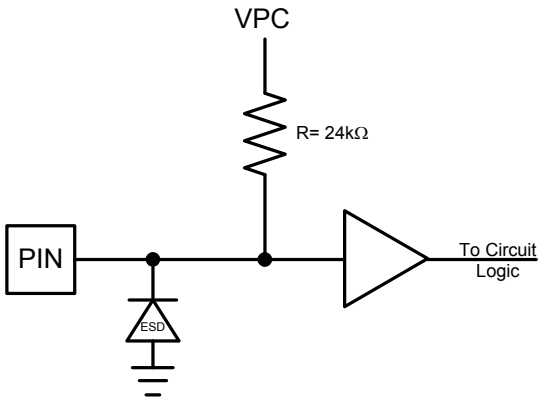


Figure 46: ON_OFF Input Circuit

5 Ordering Information

Table 116 lists the order numbers and packaging marks used to identify 73S1217F products.

Table 116: Order Numbers and Packaging Marks

Part Description	Order Number	Packaging Mark
73S1217F 68-Pin QFN, Lead Free	73S1217F-68IM/F	73S1217F68IM
73S1217F 68-Pin QFN, Lead Free, Tape and Reel	73S1217F-IMR/F	73S1217F68IM

6 Related Documentation

The following 73S1217F documents are available from Teridian Semiconductor Corporation:

73S1217F Data Sheet (this document)
73S1217F Development Board Quick Start Guide
73S1217F Software Development Kit Quick Start Guide
73S1217F Evaluation Board User's Guide
73S12xxF Software User's Guide
73S12xxF Synchronous Card Design Application Note

7 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S1217F, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.