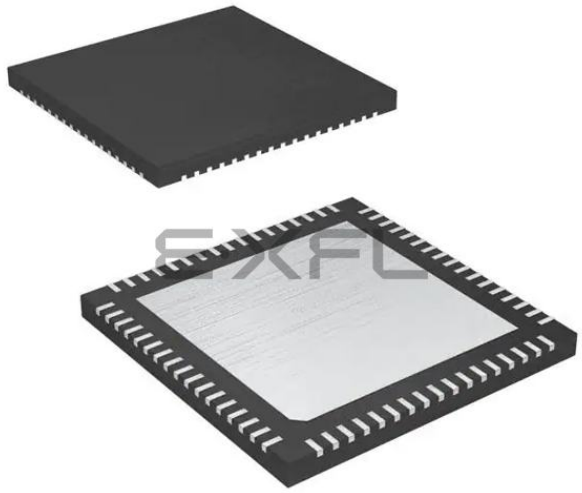
Analog Devices Inc./Maxim Integrated - 73S1217F-68MR/F/PE Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80515
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SmartCard, UART/USART, USB
Peripherals	LED, POR, WDT
Number of I/O	8
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/73s1217f-68mr-f-pe

Table of Contents

Figures

Table 3: Flash Special Function Registers

Register	SFR Address	R/W	Description
ERASE	0x94	W	This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for ERASE in order to initiate the appropriate Erase cycle (default = 0x00). 0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to PGADDR @ SFR 0xB7. 0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN @ SFR 0xB2 and the debug port must be enabled. Any other pattern written to ERASE will have no effect.
PGADDR	0xB7	R/W	Flash Page Erase Address register containing the flash memory page address (page 0 through 127) that will be erased during the Page Erase cycle (default = 0x00). Note: the page address is shifted left by one bit (see detailed description above). Must be re-written for each new Page Erase cycle.
FLSHCTL	0xB2	R/W	Bit 0 (FLSH_PWE): Program Write Enable: 0 – MOVX commands refer to XRAM Space, normal operation (default). 1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR. This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled.
		W	Bit 1 (FLSH_MEEN): Mass Erase Enable: 0 – Mass Erase disabled (default). 1 – Mass Erase enabled. Must be re-written for each new Mass Erase cycle.
		R/W	Bit 6 (SECURE): Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored.

Internal Data Memory: The internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always one byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addresses 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 4 shows the internal data memory map.

Program Status Word (PSW):

Table 9: PSW Register Flags

MSB							LSB
CV	AC	F0	RS1	RS	OV	–	P

Bit	Symbol	Function
PSW.7	CV	Carry flag.
PSW.6	AC	Auxiliary Carry flag for BCD operations.
PSW.5	F0	General purpose Flag 0 available for user.
PSW.4	RS1	Register bank select control bits. The contents of RS1 and RS0 select the working register bank:
PSW.3	RS0	
PSW.2	OV	Overflow flag.
PSW.1	F1	General purpose Flag 1 available for user.
PSW.0	P	Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity.

RS1/RS0	Bank Selected	Location
00	Bank 0	(0x00 – 0x07)
01	Bank 1	(0x08 – 0x0F)
10	Bank 2	(0x10 – 0x17)
11	Bank 3	(0x18 – 0x1F)

Stack Pointer (SP): The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

Data Pointer: The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

Program Counter: The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory. Note: The program counter is not mapped to the SFR area.

Port Registers: The I/O ports are controlled by Special Function Register USR70. The contents of the SFR can be observed on corresponding pins on the chip. Writing a 1 to any of the ports (see Table 10) causes the corresponding pin to be at high level (3.3V), and writing a 0 causes the corresponding pin to be held at low level (GND). The data direction register UDIR70 define individual pins as input or output pins (see the User (USR) Ports section for details).

Table 10: Port Registers

Register	SFR Address	R/W	Description
USR70	0x90	R/W	Register for User port bits 7:0 read and write operations (pins USR0… USR7).
UDIR70	0x91	R/W	Data direction register for User port bits 0:7. Setting a bit to 0 means that the corresponding pin is an output.

All ports on the chip are bi-directional. Each consists of a Latch (SFR USR70), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports if they are not used for alternate purposes.

The master clock control register enables different sections of the clock circuitry and specifies the value of the VCO Mcount divider. The MCLK must be configured to operate at 96MHz to ensure proper operation of some of the peripheral blocks according to the following formula:

$$MCLK = (Mcount * 2 + 4) * F_{XTAL} = 96MHz$$

Mcount is configured in the MCLKCtl register must be bound between a value of 1 to 7. The possible crystal or external clock frequencies for getting MCLK = 96MHz are shown in Table 11.

Table 11: Frequencies and Mcount Values for MCLK = 96MHz

F_{XTAL} (MHz)	Mcount (N)
12.00	2
9.60	3
8.00	4
6.86	5
6.00	6

Master Clock Control Register (MCLKCtl): 0x8F ← 0x0A

Table 12: The MCLKCtl Register

MSB							LSB
HSOEN	KBEN	SCEN	USBEN	32KEN	MCT.2	MCT.1	MCT.0

Bit	Symbol	Function
MCLKCtl.7	HSOEN	High-speed oscillator disable. When set = 1, disables the high-speed crystal oscillator and VCO/PLL system. Do not set this bit = 1.
MCLKCtl.6	KBEN	1 = Disable the keypad logic clock.
MCLKCtl.5	SCEN	1 = Disable the smart card logic clock.
MCLKCtl.4	USBEN	1 = Disable the USB logic clock.
MCLKCtl.3	32KEN	1 = Disable the 32Khz oscillator. When the 32kHz oscillator is enabled, the RTC and other circuits such as debounce clocks are clocked using the 32kHz oscillator output. When disabled, the main oscillator provides the 32kHz clock for the RTC and other circuits. **Note: This bit must be set if there is no 32KHz crystal. Some internal clocks and circuits will not run if the oscillator is enabled and no crystal is connected.**
MCLKCtl.2	MCT.2	This value determines the ratio of the VCO frequency (MCLK) to the high-speed crystal oscillator frequency such that: MCLK = (MCount*2 + 4)* F_{XTAL}. The default value is MCount = 2h such that MCLK = (2*2 + 4)*12.00MHz = 96MHz.
MCLKCtl.1	MCT.1	
MCLKCtl.0	MCT.0	

The MPU clock that drives the CPU core defaults to 3.6923MHz after reset. The MPU clock is scalable by configuring the MPU Clock Control register (MPUCKCtl).

1.7.2 Power Supply Management

The detailed power supply management logic block diagram is shown in Figure 5.

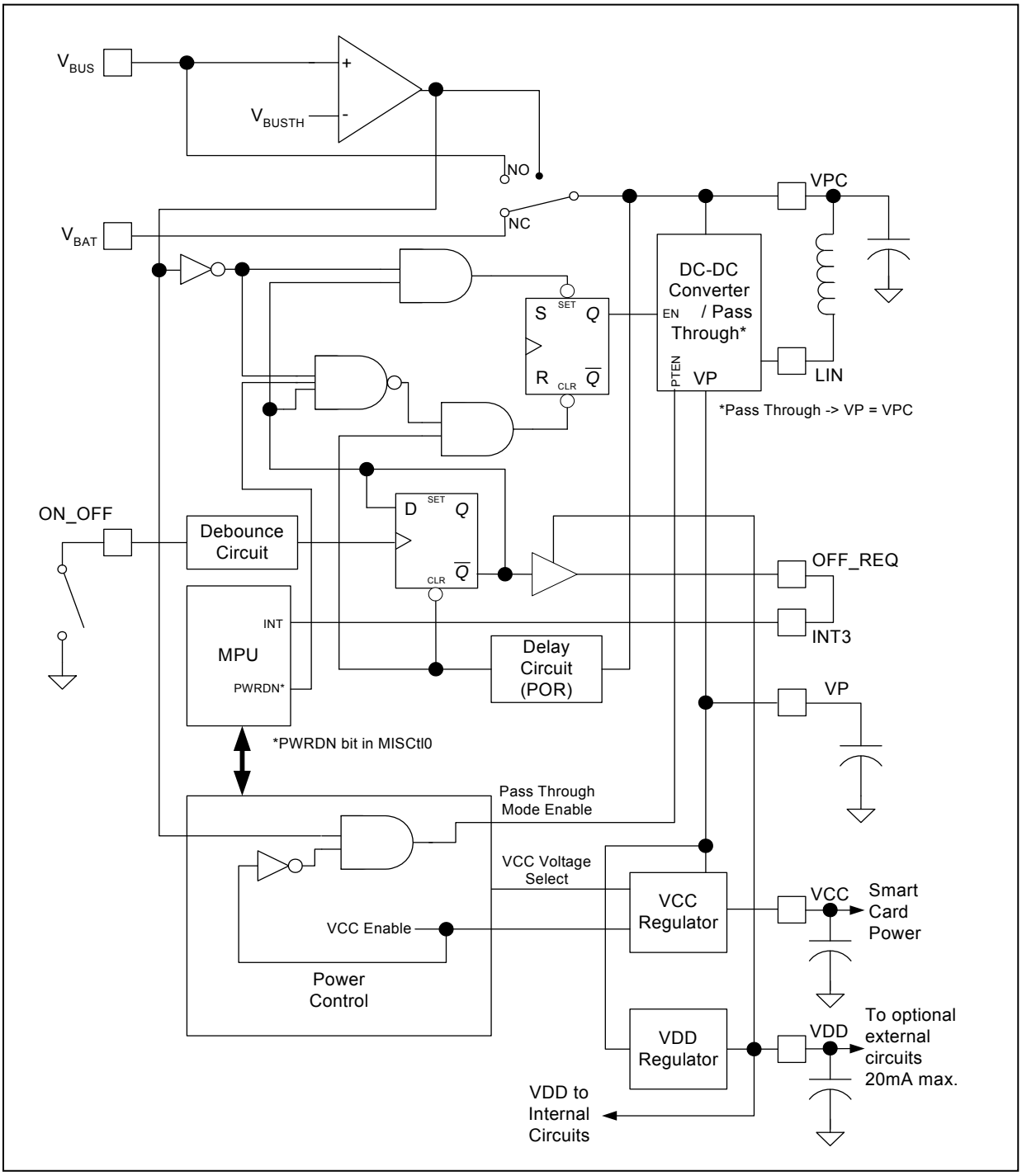


Figure 5: Detailed Power Management Logic Block Diagram

The 73S1217F contains a power supply and converter circuit that takes power from any one of three sources; V_{PC}, V_{BUS}, or V_{BAT}.

V_{PC} is specified to range from 2.7 to 6.5 volts. It can typically be supplied by a single cell battery with a voltage range of 2.7 to approximately 3.1 volts or by a standard supply of 3.3 or 5 volts.

External Interrupt Control Register (INT5Ctl): 0xFF94 ← 0x00

Table 14: The INT5Ctl Register

MSB LSB

PDMUX	–	RTCIEN	RTCINT	USBIEN	USBINT	KPIEN	KPINT

Bit	Symbol	Function
INT5Ctl.7	PDMUX	When set = 1, enables interrupts from USB, RTC, Keypad (normally going to int5), Smart Card interrupts (normally going to int4), or USR(7:0) pins (int0) to cause interrupt on int0. The assertion of the interrupt to int0 is delayed by 512 MPU clocks to allow the analog circuits, including the clock system, to stabilize. This bit must be set prior to asserting the PWRDN bit in order to properly configure the interrupts that will wake up the circuit. This bit is reset = 0 when this register is read.
INT5Ctl.6	–	
INT5Ctl.5	RTCIEN	RTC interrupt enable.
INT5Ctl.4	RTCINT	RTC interrupt flag.
INT5Ctl.3	USBIEN	USB interrupt enable.
INT5Ctl.2	USBINT	USB interrupt flag.
INT5Ctl.1	KPIEN	Keypad interrupt enable.
INT5Ctl.0	KPINT	Keypad interrupt flag.

Miscellaneous Control Register 0 (MISCtl0): 0xFFF1 ← 0x00

Table 15: The MISCtl0 Register

MSB LSB

PWRDN	–	–	–	–	–	SLPBK	SSEL

Bit	Symbol	Function
MISCtl0.7	PWRDN	This bit sets the circuit into a low-power condition. All analog (high speed oscillator and VCO/PLL) functions are disabled 32 MPU clock cycles after this bit is set = 1. This allows time for the next instruction to set the STOP bit in the PCON register to stop the CPU core. The RTC will stay active if it is set to operate from the 32kHz oscillator. The MPU is not operative in this mode. When set, this bit overrides the individual control bits that otherwise control power consumption.
MISCtl0.6	–	
MISCtl0.5	–	
MISCtl0.4	–	
MISCtl0.3	–	
MISCtl0.2	–	
MISCtl0.1	SLPBK	UART loop back testing mode.
MISCtl0.0	SSEL	Serial port pins select.

Interrupt Request Register (IRCON): 0xC0 ← 0x00

Table 24: The IRCON Register

MSB							LSB
–	–	EX6	IEX5	IEX4	IEX3	IEX2	–

Bit	Symbol	Function
IRCON.7	–	
IRCON.6	–	
IRCON.5	IEX6	External interrupt 6 flag.
IRCON.4	IEX5	External interrupt 5 flag.
IRCON.3	IEX4	External interrupt 4 flag.
IRCON.2	IEX3	External interrupt 3 flag.
IRCON.1	IEX2	External interrupt 2 flag.
IRCON.0	–	

1.7.5.3 External Interrupts

The external interrupts (external to the CPU core) are connected as shown in Table 25. Interrupts with multiple sources are OR'ed together and individual interrupt source control is provided in XRAM SFRs to mask the individual interrupt sources and provide the corresponding interrupt flags. Multifunction USR [7:0] pins control Interrupts 0 and 1. Dedicated external interrupt pins INT2 and INT3 control interrupts 2 and 3. The polarity of interrupts 2 and 3 is programmable in the MPU. Interrupts 4, 5 and 6 have multiple peripheral sources and are multiplexed to one of these three interrupts. The peripheral functions will be described in subsequent sections. Generic 80515 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 4, 5 and 6 are converted to rising edge level by the hardware.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler.

Table 25: External MPU Interrupts

External Interrupt	Connection	Polarity	Flag Reset
0	USR I/O High Priority	see USRIntCtlx	Automatic
1	USR I/O Low Priority	see USRIntCtlx	Automatic
2	External Interrupt Pin INT2	Edge selectable	Automatic
3	External Interrupt Pin INT3	Edge selectable	Automatic
4	Smart Card Interrupts	N/A	Automatic
5	USB, RTC and Keypad	N/A	Automatic
6	I^2C, V_{DD}_Fault, Analog Comp	N/A	Automatic

Note: Interrupts 4, 5 and 6 have multiple interrupt sources and the flag bits are cleared upon reading of the corresponding register. To prevent any interrupts from being ignored, the register containing multiple interrupt flags should be stored temporary to allow each interrupt flag to be tested separately to see which interrupt(s) is/are pending.

External Interrupt Control Register (USRIntCtl1) : 0xFF90 ← 0x00

Table 50: The USRIntCtl1 Register

MSB							LSB
–	U1IS.6	U1IS.5	U1IS.4	–	U0IS.2	U0IS.1	U0IS.0

External Interrupt Control Register (USRIntCtl2) : 0xFF91 ← 0x00

Table 51: The USRIntCtl2 Register

MSB							LSB
–	U3IS.6	U3IS.5	U3IS.4	–	U2IS.2	U2IS.1	U2IS.0

External Interrupt Control Register (USRIntCtl3) : 0xFF92 ← 0x00

Table 52: The USRIntCtl3 Register

MSB							LSB
–	U5IS.6	U5IS.5	U5IS.4	–	U4IS.2	U4IS.1	U4IS.0

External Interrupt Control Register (USRIntCtl4) : 0xFF93 ← 0x00

Table 53: The USRIntCtl4 Register

MSB							LSB
–	U7IS.6	U7IS.5	U7IS.4	–	U6IS.2	U6IS.1	U6IS.0

1.7.11 Analog Voltage Comparator

The 73S1217F includes a programmable comparator that is connected to the ANA_IN pin. The comparator can be configured to trigger an interrupt if the input voltage rises above or falls below a selectable threshold voltage. The comparator control register should not be modified when the analog interrupt (ANAIEN bit in the INT6Ctl register) is enabled to guard against any false interrupt that might be generated when modifying the threshold. The comparator has a built-in hysteresis to prevent the comparator from repeatedly responding to low-amplitude noise. This hysteresis is approximately 20mV. The maximum voltage on the ANA_IN pad should be less than 3 volts. An external resistor divider is required for detecting voltages greater than 3.0 volts. Interrupt control is handled in the INT6Ctl register.

Analog Compare Control Register (ACOMP): 0xFFD0 ← 0x00

Table 59: The ACOMP Register

MSB LSB

ANALVL	–	ONCHG	CPOL	CMPEN	0	TSEL.1	TSEL.0

Bit	Symbol	Function
ACOMP.7	ANALVL	When read, indicates whether the input level is above or below the threshold. This is a real time value and is not latched, so it may change from the time of the interrupt trigger until read.
ACOMP.6	–	
ACOMP.5	ONCHG	If set, the Ana_interrupt is invoked on any change above or below the threshold, bit 4 is ignored.
ACOMP.4	CPOL	If set = 1, Ana_interrupt is invoked when signal rises above selected threshold. If set = 0, Ana_interrupt is invoked when signal goes below selected threshold (default).
ACOMP.3	CMPEN	Enables power to the analog comparator. 1= Enabled. 0 = Disabled (default).
ACOMP.2	0	This value must be fixed at 0.
ACOMP.1	TSEL.1	Sets the voltage threshold for comparison to the voltage on pin ANA_IN. Thresholds are as follows: 00 = 1.00V 01 = 1.24V 10 = 1.40V 11 = 1.50V
ACOMP.0	TSEL.0	

1.7.13 I²C Master Interface

The 73S1217F includes a dedicated fast mode, 400kHz I²C Master interface. The I²C interface can read or write 1 or 2 bytes of data per data transfer frame. The MPU communicates with the interface through six dedicated SFR registers:

- Device Address (DAR)
- Write Data (WDR)
- Secondary Write Data (SWDR)
- Read Data (RDR)
- Secondary Read Data (SRDR)
- Control and Status (CSR)

The DAR register is used to set up the slave address and specify if the transaction is a read or write operation. The CSR register sets up, starts the transaction and reports any errors that may occur. When the I²C transaction is complete, the I²C interrupt is reported via external interrupt 6. The I²C interrupt is automatically de-asserted when a subsequent I²C transaction is started. The I²C interface uses a 400kHz clock from the time-base circuits.

1.7.13.1 I²C Write Sequence

To write data on the I²C Master Bus, the 80515 has to program the following registers according to the following sequence:

1. Write slave device address to Device Address register (DAR). The data contains 7 bits for the slave device address and 1 bit of op-code. The op-code bit should be written with a '0' to indicate a write operation.
2. Write data to Write Data register (WDR). This data will be transferred to the slave device.
3. If writing 2 bytes, set bit 0 of the Control and Status register (CSR) and load the second data byte to Secondary Write Data register (SWDR).
4. Set bit 1 of the CSR register to start I²C Master Bus.
5. Wait for I²C interrupt to be asserted. It indicates that the write on I²C Master Bus is done. Refer to information about the INT6Ctl, IEN1 and IRCON register for masking and flag operation.

The following diagram shows the timing of the I^2C read mode.

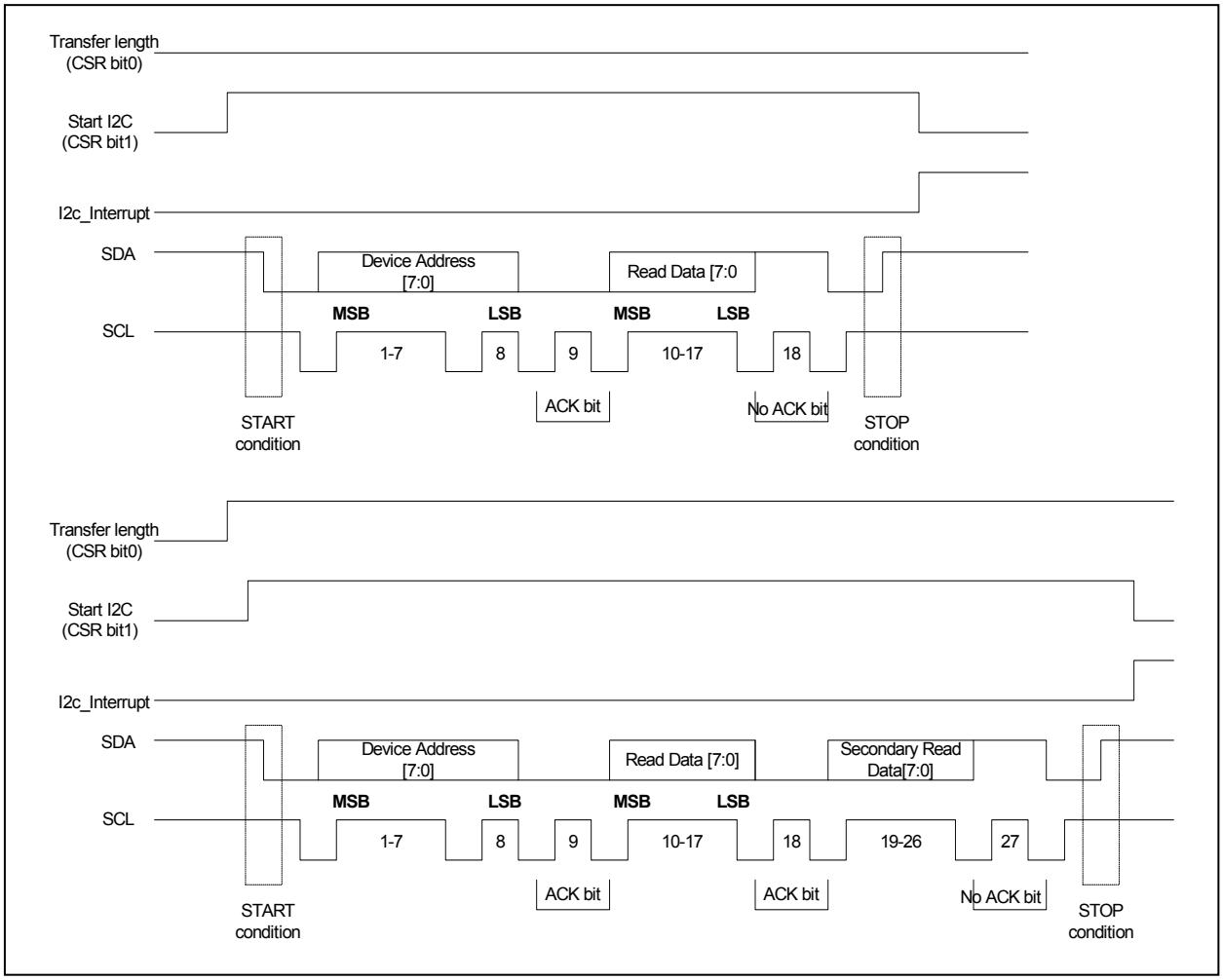


Figure 12: I^2C Read Operation

I2C Secondary Write Data Register (SWDR): 0XFF82 ← 0x00

Table 64: The SWDR Register

MSB LSB

SWDR.7	SWDR.6	SWDR.5	SWDR.4	SWDR.3	SWDR.2	SWDR.1	SWDR.0

Bit	Function
SWDR.7	Second Data byte to be written to the I^2C slave device if bit 0 (I2CLEN) of the Control and Status register (CSR) is set = 1.
SWDR.6	
SWDR.5	
SWDR.4	
SWDR.3	
SWDR.2	
SWDR.1	
SWDR.0	

I2C Read Data Register (RDR): 0XFF83 ← 0x00

Table 65: The RDR Register

MSB LSB

RDR.7	RDR.6	RDR.5	RDR.4	RDR.3	RDR.2	RDR.1	RDR.0

Bit	Function
RDR.7	Data read from the I^2C slave device.
RDR.6	
RDR.5	
RDR.4	
RDR.3	
RDR.2	
RDR.1	
RDR.0	

decoding, handshake packet generation, Data0/Data1 toggle synchronization, bit stuffing, bus idle detection and other protocol generation/checking required in Chapter 8 of the USB specification.

The firmware is responsible for servicing and building the messages required under Chapter 9 of the USB specification. Device configuration is stored in the firmware. Data received from the USB port is stored in the appropriate IN FIFO that is read by the firmware and processed. The messages to be sent back to the USB host are generated by firmware and placed back into the appropriate OUT FIFO. Stall/NAK handshakes are generated as appropriate if the RAM is not available for another message from the USB host. Suspend and resume modes are supported. All register/FIFO spaces are located in Data Memory space. The FIFOs are dedicated for USB storage and are unused in a configuration that is not using USB. All registers in the USB interface are located in external data memory address (XRAM) space starting at address FC00'h.

1.7.16.1 USB Interface Implementation

The 73S1217F Application Programming Interface includes some dedicated software commands to configure the USB interface, to get a status of each USB Endpoint, to stall / unstall portions of the USB, and to send / receive data to / from each endpoint.

USB API entirely manages the USB circuitry, the USB registers and the FIFOs. Use of those commands facilitates USB implementation, without dealing with low-level programming.

Miscellaneous Control Register 1 (MISCtl1): 0xFFF2 ← 0x10

Table 77: The MISCtl1 Register

MSB LSB

–	–	FRPEN	FLSH66	–	ANAPEN	USBPEN	USBCON

Bit	Symbol	Function
MISCtl1.7	–	
MISCtl1.6	–	
MISCtl1.5	FRPEN	Flash Read Pulse enable.
MISCtl1.4	FLSH66	Flash Read Pulse.
MISCtl1.3	–	
MISCtl1.2	ANAPEN	Analog power enable.
MISCtl1.1	USBPEN	0 = Enable the USB differential transceiver.
MISCtl1.0	USBCON	1 = Connect pull-up resistor from VDD to D+. If connected, the USB host will recognize the attachment of a USB device and begin enumeration.

Note: When using the USB on the 73S1217F, external 24Ω series resistors must be added to the D+ and D- signals to provide the proper impedance matching on these pins.

The USB peripheral block is not able to support read or write operations to the USB SFR registers when the MPU clock is running at MPU clock rates of 12MHz or greater. In order to properly communicate with the USB SFR registers when running at these speeds, wait states must be inserted when addressing the USB SFRs. The CKCON register allows wait states to be inserted when accessing these registers. The proper settings for the number of wait states are shown in **Error! Reference source not found.**.

When changing the MPU clock rate or the number of wait states, the USB connection must be inactive. If the USB is active, then it must be inactivated before changing the MPU clock or number of wait states. It can then be reconnected and re-enumerated. Changing these parameters while the USB interface is active may cause communication errors on the USB interface.

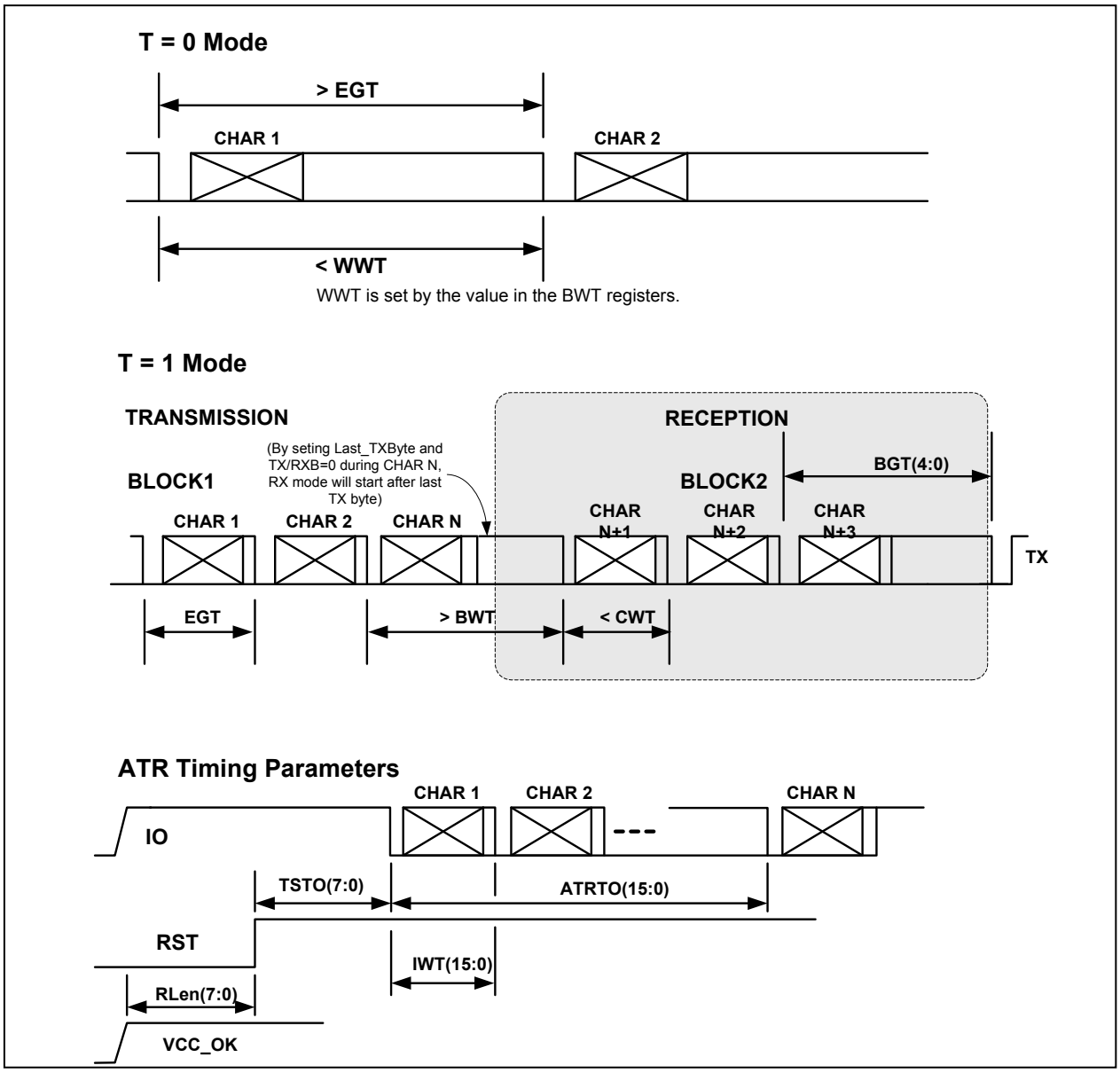


Figure 21: Guard, Block, Wait and ATR Time Definitions

1.7.17.4 Bypass Mode

It is possible to bypass the smart card UART in order for the firmware to support non-T=0/T=1 smart cards. This is called Bypass mode. In this mode the embedded firmware will communicate directly with the selected smart card and drive I/O during transmit and read I/O during receive in order to communicate with the smart card. In this mode, ATR processing is under firmware control. The firmware must sequence the interface signals as required. Firmware must perform TS processing, parity checking, break generation and CRC/LRC calculation (if required).

1.7.17.5 Synchronous Operation Mode

The 73S1217F supports synchronous operation. When sync mode is selected for either interface, the CLK signal is generated by the ETU counter. The values in FDReg, SCCLK, and SCECLK must be set to obtain the desired sync CLK rate. There is only one ETU counter and therefore, in sync mode, the interface must be selected to obtain a smart card clock signal. In sync mode, input data is sampled on the rise of CLK, and output data is changed on the fall of CLK.
Special Notes Regarding Synchronous Mode Operation

SRX Data Register (SRXData): 0xFE09 ← 0x00

Table 88: The SRXData Register

MSB LSB

SRXDAT.7	SRXDAT.6	SRXDAT.5	SRXDAT.4	SRXDAT.3	SRXDAT.2	SRXDAT.1	SRXDAT.0

Bit	Function
SRXData.7	(Read only) Data received from the smart card. Data received from the smart card gets stored in a FIFO that is read by the firmware.
SRXData.6	
SRXData.5	
SRXData.4	
SRXData.3	
SRXData.2	
SRXData.1	
SRXData.0	

Block Wait Time Registers (BWTB0): 0xFE1B ← 0x00, (BWTB1): 0xFE1A ← 0x00, (BWTB2): 0xFE19 ← 0x00, (BWTB3): 0xFE18 ← 0x00

Table 104: The BWTB0 Register

MSB							LSB
BWT.7	BWT.6	BWT.5	BWT.4	BWT.3	BWT.1	BWT.2	BWT.0

Table 105: The BWTB1 Register

MSB							LSB
BWT.15	BWT.14	BWT.13	BWT.12	BWT.11	BWT.10	BWT.9	BWT.8

Table 106: The BWTB2 Register

MSB							LSB
BWT.23	BWT.22	BWT.21	BWT.20	BWT.19	BWT.18	BWT.17	BWT.16

Table 107: The BWTB3 Register

MSB							LSB
–	–	–	–	BWT.27	BWT.26	BWT.25	BWT.24

These registers (BWTB0, BWTB1, BWTB2, BWTB3) are used to set the Block Waiting Time(27:0) (BWT). All of these parameters define the maximum time the 73S1217F will have to wait for a character from the smart card. These registers serve a dual purpose. When T=1, these registers are used to set up the block wait time. The block wait time defines the time in ETUs between the beginning of the last character sent to smart card and the start bit of the first character received from smart card. It can be used to detect an unresponsive card and should be loaded by firmware prior to writing the last TX byte. When T = 0, these registers are used to set up the work wait time. The work wait time is defined as the time between the leading edge of two consecutive characters being sent to or from the card. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action. A Wait Time Extension (WTX) is supported with the 28-bit BWT.

Character Wait Time Registers (CWTB0): 0xFE1D ← 0x00, (CWTB1): 0xFE1C ← 0x00

Table 108: The CWTB0 Register

MSB							LSB
CWT.7	CWT.6	CWT.5	CWT.4	CWT.3	CWT.1	CWT.2	CWT.0

Table 109: The CWTB1 Register

MSB							LSB
CWT.15	CWT.14	CWT.13	CWT.12	CWT.11	CWT.10	CWT.9	CWT.8

These registers (CWTB0, CWTB1) are used to hold the Character Wait Time(15:0) (CWT) or Initial Waiting Time(15:0) (IWT) depending on the situation. Both the IWT and the CWT measure the time in ETUs between the leading edge of the start of the current character received from the smart card and the leading edge of the start of the next character received from the smart card. The only difference is the mode in which the card is operating. When T=1 these registers are used to configure the CWT and these registers configure the IWT when the ATR is being received. These registers should be loaded prior to receiving characters from the smart card. Firmware must manage which time is stored in the register. If a timeout occurs, an interrupt is generated to the firmware. The firmware can then take appropriate action.

ATR Timeout Registers (ATRLsB): 0xFE20 ← 0x00, (ATRMsB): 0xFE1F ← 0x00

Table 110: The ATRLsB Register

MSB							LSB
ATRTO.7	ATRTO.6	ATRTO.5	ATRTO.4	ATRTO.3	ATRTO.1	ATRTO.2	ATRTO.0

Table 111: The ATRMsB Register

MSB							LSB
ATRTO.15	ATRTO.14	ATRTO.13	ATRTO.12	ATRTO.11	ATRTO.10	ATRTO.9	ATRTO.8

These registers (ATRLsB and ATRLsB) form the ATR timeout (ATRTO [15:0]) parameter. Time in ETU between the leading edge of the first character and leading edge of the last character of the ATR response. Timer is enabled when the RCVATR is set and starts when leading edge of the first start bit is received and disabled when the RCVATR is cleared. An ATR timeout is generated if this time is exceeded.

TS Timeout Register (STSTO): 0xFE21 ← 0x00

Table 112: The STSTO Register

MSB							LSB
TST0.7	TST0.6	TST0.5	TST0.4	TST0.3	TST0.1	TST0.2	TST0.0

The TS timeout is the time in ETU between the de-assertion of smart card reset and the leading edge of the TS character in the ATR (when DETTS is set). The timer is started when smart card reset is de-asserted. An ATR timeout is generated if this time is exceeded (MUTE card).

Reset Time Register (RLength): 0xFE22 ← 0x70

Table 113: The RLength Register

MSB							LSB
RLen.7	RLen.6	RLen.5	RLen.4	RLen.3	RLen.1	RLen.2	RLen.0

Time in ETUs that the hardware delays the de-assertion of RST. If set to 0 and RSTCRD = 0, the hardware adds no extra delay and the hardware will release RST after VCCOK is asserted during power-up. If set to 1, it will delay the release of RST by the time in this register. When the firmware sets the RSTCRD bit, the hardware will assert reset (RST = 0 on pin). When firmware clears the bit, the hardware will release RST after the delay specified in Rlen. If firmware sets the RSTCRD bit prior to instructing the power to be applied to the smart card, the hardware will not release RST after power-up until RLen after the firmware clears the RSTCRD bit. This provides a means to power up the smart card and hold it in reset until the firmware wants to release the RST to the selected smart card. Works with the selected smart card interface.

2.2 Typical Application Schematic 2

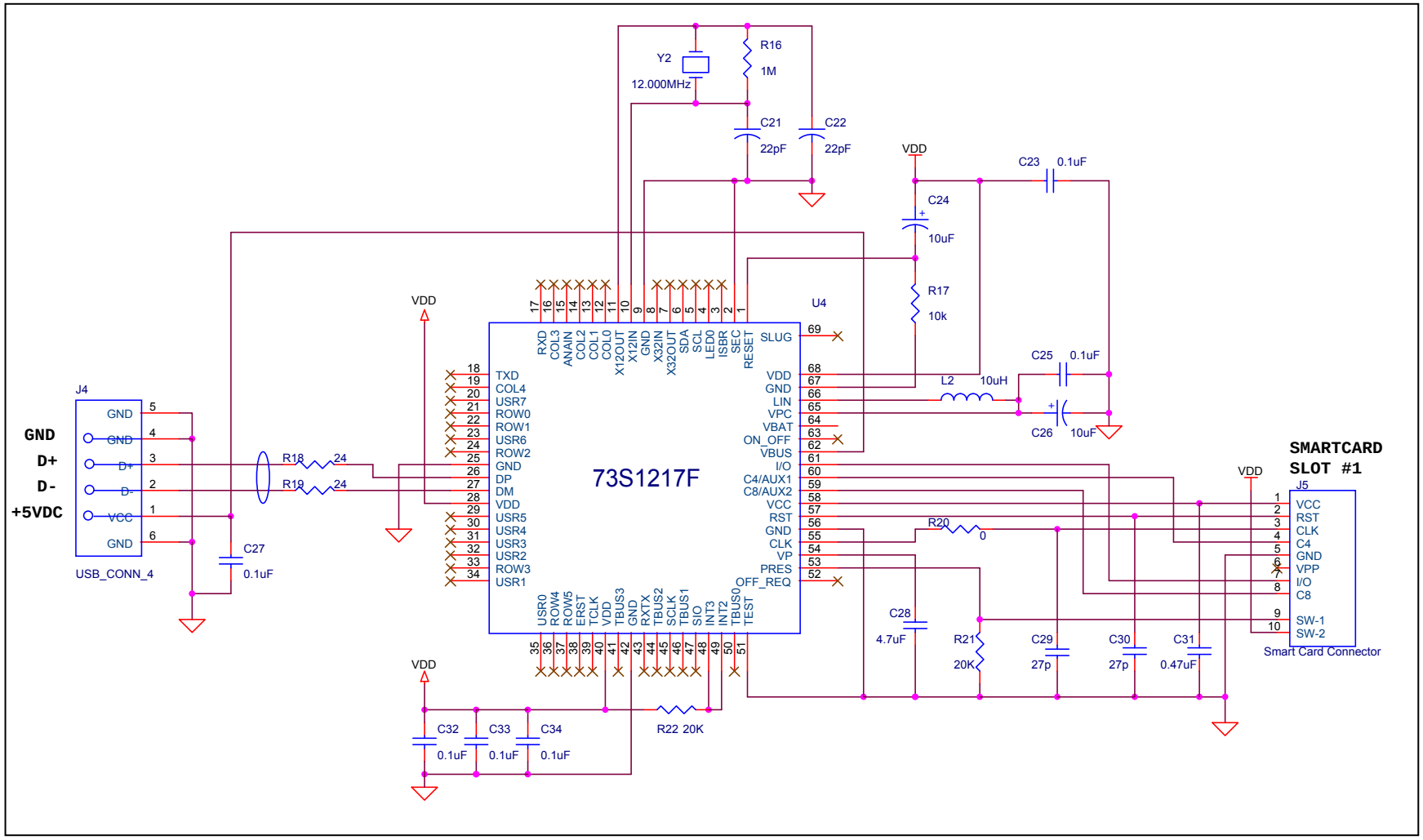


Figure 28: 73S1217F Typical Application Schematic (USB Transparent Reader and USB Key Configuration)

4.1 Package Pin Designation (68-Pin QFN)

CAUTION: Use handling procedures necessary for a static sensitive component

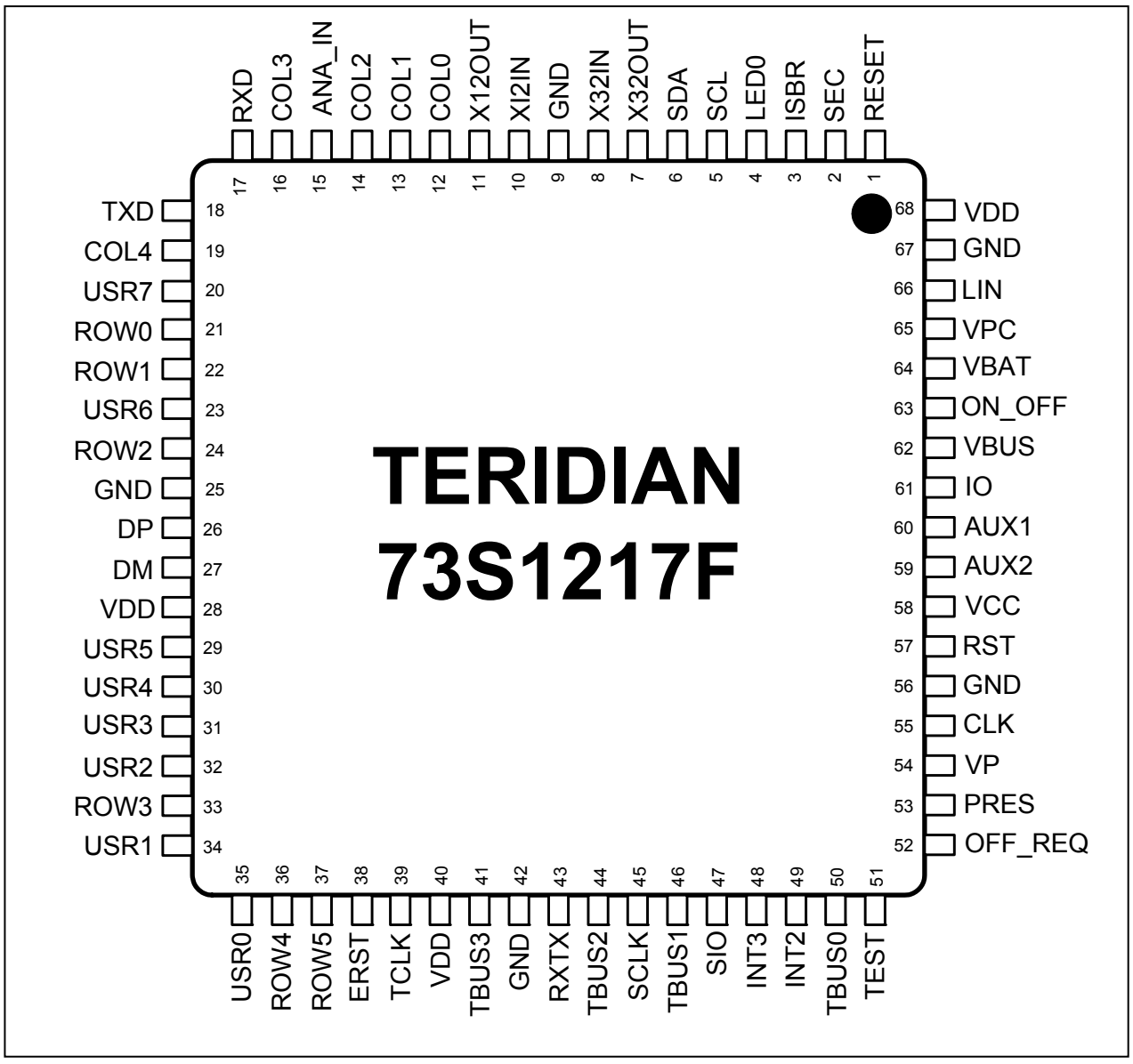


Figure 47: 73S1217F Pinout