Renesas Electronics America Inc - R5F5634BCDFB#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5634bcdfb-30

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Power supply voltage		• 3-V package VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V • 5-V package VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V
Operating temperature		–40 to +85°C (products with wide-temperature-range spec.)
Packages		144-pin LQFP (PLQP0144KA-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1 / 4)

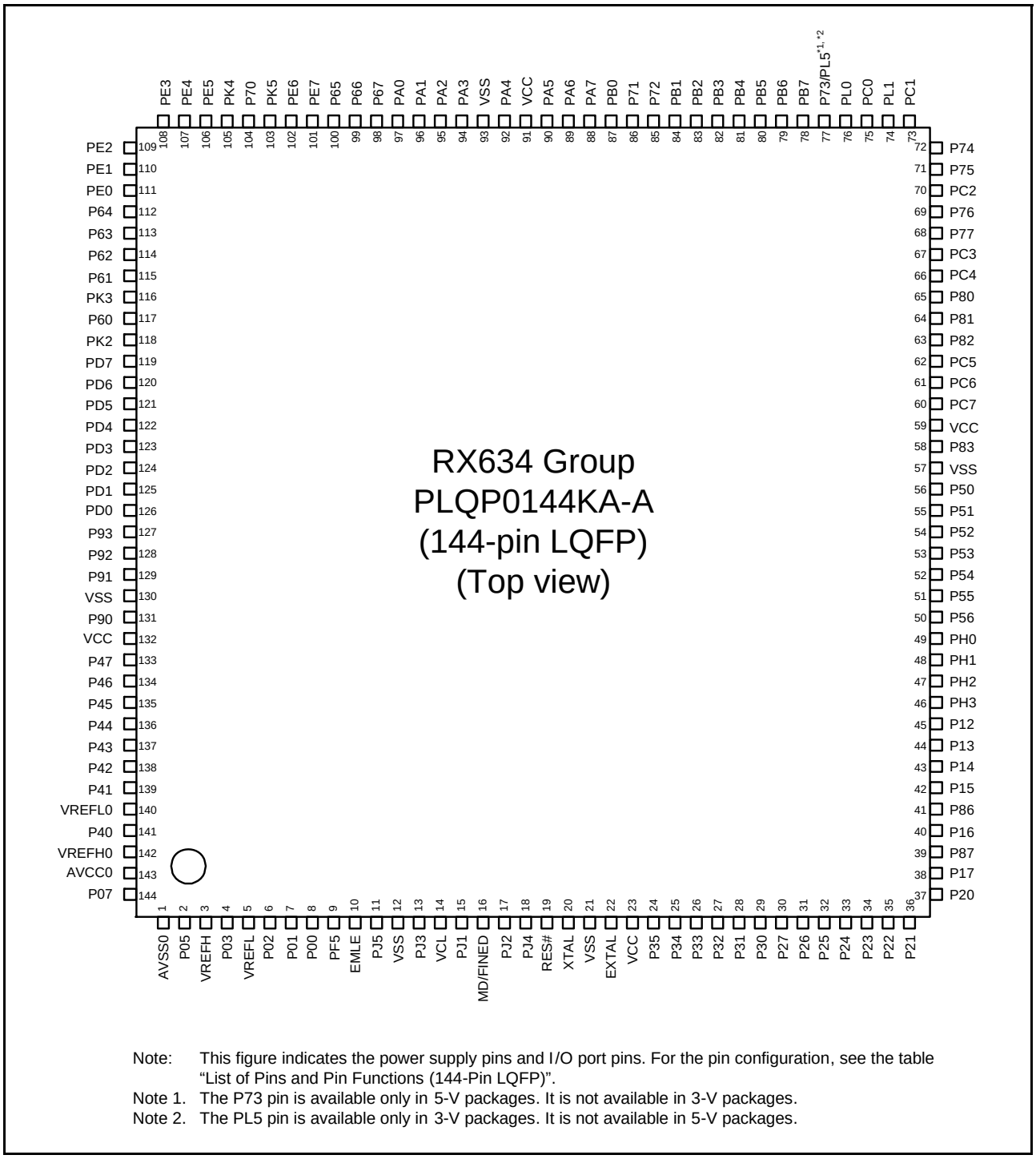
Classifications	Pin Name	I/O	Description
Power supply	VCC	—	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	—	Connect this pin to the VSS pin via the 0.1 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	—	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
Clock frequency accuracy measurement	CACREF	Input	Input for the trigger signal in measuring accuracy of the clock frequency
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the onchip emulator is used, this pin should be driven high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC#	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in single-write strobe mode.
	WR0# to WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in single-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT#	Input	Input pin for wait request signals in access to the external space.
	CS0# to CS3#	Output	Select signals for areas 0 to 3.

Table 1.4 Pin Functions (3 / 4)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIe)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	RXD0 to RXD11	Input	Input pins for received data
	TXD0 to TXD11	Output	Output pins for transmitted data
	CTS0# to CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmission of data
	SS0# to SS11#	Input	Chip-select input pins
Serial communications interface (SCIf)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmit data
	SMOSI12	I/O	Input/output pin for master transmit data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCId
	TXDX12	Output	Output pin for data transmission by SCId
	SIOX12	I/O	Input/output pin for data reception or transmission by SCId
I^2C bus interface	SCL0, SCL1, SCL3	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open-drain output.
	SDA0, SDA1, SDA3	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open-drain output.
Serial peripheral interface	RSPCKA, RSPCKB	I/O	Clock input/output pin for the RSPI.
	MOSIA, MOSIB	I/O	Input or output data output from the master for the RSPI.
	MISOA, MISOB	I/O	Input or output data output from the slave for the RSPI.
	SSLA0, SSLB0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3 SSLB1 to SSLB3	Output	Output pins to select the slave for the RSPI.
CEC transmission/ reception circuit (CEC)	CECIO	I/O	Input/output pin for CEC communication data
Remote control signal receiver (RCR)	PMC0	Input	Input pin for external pulse signal
	PMC1	Input	Input pin for external pulse signal

1.5 Pin Assignments

Figure 1.3 shows the pin assignments. Table 1.5 shows the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see the table "List of Pins and Pin Functions (144-Pin LQFP)".
Note 1. The P73 pin is available only in 5-V packages. It is not available in 3-V packages.
Note 2. The PL5 pin is available only in 3-V packages. It is not available in 5-V packages.

Figure 1.3 Pin Assignments of the 144-Pin LQFP

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).
The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.
When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

Table 4.1 List of I/O Registers (Address Order) (2 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACA	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 to 2BCLK		Buses	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 to 2BCLK			
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 to 2BCLK			
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 to 2BCLK			
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 to 2BCLK			
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 to 2BCLK			

Table 4.1 List of I/O Registers (Address Order) (13 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 750Eh	CEC	CEC Interrupt Control Register 2	CECINTCR2	8	8	2 ICLK		CEC	Not available in 5-V packages.
0008 750Fh	CEC	CEC Interrupt Control Register 3	CECINTCR3	8	8	2 ICLK			Not available in 5-V packages.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUb	
0008 7511h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 to 3PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 to 3PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 to 3PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 to 3PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 to 3PCLKB	2 ICLK	DAa	
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2 to 3PCLKB	2 ICLK		
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 to 3PCLKB	2 ICLK		
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 to 3PCLKB	2 ICLK	TPUa	
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 to 3PCLKB	2 ICLK		
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (16 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8310h	RIIC0	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8311h	RIIC0	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8312h	RIIC0	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8313h	RIIC0	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8320h	RIIC1	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8321h	RIIC1	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8322h	RIIC1	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8323h	RIIC1	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8324h	RIIC1	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8325h	RIIC1	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8326h	RIIC1	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8327h	RIIC1	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8328h	RIIC1	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8329h	RIIC1	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8330h	RIIC1	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8331h	RIIC1	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8332h	RIIC1	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8333h	RIIC1	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8360h	RIIC3	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8361h	RIIC3	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8362h	RIIC3	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8363h	RIIC3	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8364h	RIIC3	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8365h	RIIC3	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8366h	RIIC3	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8367h	RIIC3	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8368h	RIIC3	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8369h	RIIC3	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 836Ch	RIIC3	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Dh	RIIC3	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Eh	RIIC3	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (23 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A0E8h	SCI7	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A0E9h	SCI7	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EAh	SCI7	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EBh	SCI7	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A0ECh	SCI7	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A0EDh	SCI7	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A100h	SCI8	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A101h	SCI8	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A102h	SCI8	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A103h	SCI8	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A104h	SCI8	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A105h	SCI8	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A106h	SCI8	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A107h	SCI8	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A108h	SCI8	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A109h	SCI8	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Ah	SCI8	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Bh	SCI8	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Ch	SCI8	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A10Dh	SCI8	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A120h	SCI9	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A121h	SCI9	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A122h	SCI9	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A123h	SCI9	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A124h	SCI9	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A125h	SCI9	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A126h	SCI9	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A127h	SCI9	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A128h	SCI9	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A129h	SCI9	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Ah	SCI9	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Bh	SCI9	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Ch	SCI9	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A12Dh	SCI9	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A140h	SCI10	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A141h	SCI10	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A142h	SCI10	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 A143h	SCI10	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A144h	SCI10	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A145h	SCI10	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A146h	SCI10	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A147h	SCI10	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A148h	SCI10	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A149h	SCI10	I²C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Ah	SCI10	I²C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Bh	SCI10	I²C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Ch	SCI10	I²C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A14Dh	SCI10	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A160h	SCI11	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A161h	SCI11	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 A162h	SCI11	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (27 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C066h	PORT6	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C073h	PORTK	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C074h	PORTL	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ch	PORT6	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A6h	PORTK	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A7h	PORTK	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (29 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C158h	MPC	P30 Pin Function Control Registers	P30PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C159h	MPC	P31 Pin Function Control Registers	P31PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ah	MPC	P32 Pin Function Control Registers	P32PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Bh	MPC	P33 Pin Function Control Registers	P33PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ch	MPC	P34 Pin Function Control Registers	P34PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C160h	MPC	P40 Pin Function Control Registers	P40PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C161h	MPC	P41 Pin Function Control Registers	P41PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C162h	MPC	P42 Pin Function Control Registers	P42PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C163h	MPC	P43 Pin Function Control Registers	P43PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C164h	MPC	P44 Pin Function Control Registers	P44PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C165h	MPC	P45 Pin Function Control Registers	P45PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C166h	MPC	P46 Pin Function Control Registers	P46PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C167h	MPC	P47 Pin Function Control Registers	P47PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C168h	MPC	P50 Pin Function Control Registers	P50PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C169h	MPC	P51 Pin Function Control Registers	P51PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ah	MPC	P52 Pin Function Control Registers	P52PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ch	MPC	P54 Pin Function Control Registers	P54PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Dh	MPC	P55 Pin Function Control Registers	P55PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Eh	MPC	P56 Pin Function Control Registers	P56PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C170h	MPC	P60 Pin Function Control Registers	P60PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C171h	MPC	P61 Pin Function Control Registers	P61PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C178h	MPC	P70 Pin Function Control Registers	P70PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Registers	P73PFS	8	8	2 to 3PCLKB	2 ICLK		Not available in 3-V packages.
0008 C17Ch	MPC	P74 Pin Function Control Registers	P74PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Registers	P75PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Registers	P76PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Fh	MPC	P77 Pin Function Control Registers	P77PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Registers	P80PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C181h	MPC	P81 Pin Function Control Registers	P81PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C182h	MPC	P82 Pin Function Control Registers	P82PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C183h	MPC	P83 Pin Function Control Registers	P83PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C186h	MPC	P86 Pin Function Control Registers	P86PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C187h	MPC	P87 Pin Function Control Registers	P87PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C188h	MPC	P90 Pin Function Control Registers	P90PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C189h	MPC	P91 Pin Function Control Registers	P91PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Ah	MPC	P92 Pin Function Control Registers	P92PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Bh	MPC	P93 Pin Function Control Registers	P93PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C190h	MPC	PA0 Pin Function Control Registers	PA0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C191h	MPC	PA1 Pin Function Control Registers	PA1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C192h	MPC	PA2 Pin Function Control Registers	PA2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Registers	PA3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Registers	PA4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C195h	MPC	PA5 Pin Function Control Registers	PA5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C196h	MPC	PA6 Pin Function Control Registers	PA6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C197h	MPC	PA7 Pin Function Control Registers	PA7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C198h	MPC	PB0 Pin Function Control Registers	PB0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Registers	PB1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Registers	PB2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Registers	PB3PFS	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (31 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 to 5PCLKB	2 to 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash Write Erase Protection Register	FWEPROR	8	8	4 to 5PCLKB	2 to 3 ICLK	Flash Memory	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 to 5PCLKB	2 to 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4 to 5PCLKB	2 to 3 ICLK	Low Power Consumption	
000A 0A00h	CEC	CEC Local Address Setting Register	CADR	16	16	1 to 2PCLK	1 ICLK	CEC	Not available in 5-V packages.
000A 0A02h	CEC	CEC Control Register 1	CECCTL1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A04h	CEC	CEC Transmission Start Bit Width Setting Register	STATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A06h	CEC	CEC Transmission Start Bit Low Width Setting Register	STATL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A08h	CEC	CEC Transmission Logical 0 Low Width Setting Register	LGC0L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ah	CEC	CEC Transmission Logical 1 Low Width Setting Register	LGC1L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ch	CEC	CEC Transmission Data Bit Width Setting Register	DATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Eh	CEC	CEC Reception Data Sampling Time Setting Register	NOMT	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A10h	CEC	CEC Reception Start Bit Minimum Low Width Setting Register	STATLL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A12h	CEC	CEC Reception Start Bit Maximum Low Width Setting Register	STATLH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A14h	CEC	CEC Reception Start Bit Minimum Bit Width Setting Register	STATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A16h	CEC	CEC Reception Start Bit Maximum Bit Width Setting Register	STATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A18h	CEC	CEC Reception Logical 0 Minimum Low Width Setting Register	LGC0LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ah	CEC	CEC Reception Logical 0 Maximum Low Width Setting Register	LGC0LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ch	CEC	CEC Reception Logical 1 Minimum Low Width Setting Register	LGC1LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Eh	CEC	CEC Reception Logical 1 Maximum Low Width Setting Register	LGC1LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A20h	CEC	CEC Reception Data Bit Minimum Bit Width Setting Register	DATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A22h	CEC	CEC Reception Data Bit Maximum Bit Width Setting Register	DATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A24h	CEC	CEC Data Bit Reference Width Setting Register	NOMP	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

Table 4.1 List of I/O Registers (Address Order) (34 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
000A 0B95h	RCR1	Receive Bit Count Register	RBIT	8	8	1 to 2PCLK	1 ICLK	RCR	Not available in 5-V packages.
000A 0B96h	RCR1	Receive Data 0 Register	DAT0	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B97h	RCR1	Receive Data 1 Register	DAT1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B98h	RCR1	Receive Data 2 Register	DAT2	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B99h	RCR1	Receive Data 3 Register	DAT3	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Ah	RCR1	Receive Data 4 Register	DAT4	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Bh	RCR1	Receive Data 5 Register	DAT5	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Ch	RCR1	Receive Data 6 Register	DAT6	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Dh	RCR1	Receive Data 7 Register	DAT7	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0B9Eh	RCR1	Measurement Result Register	TIM	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0C00h	SYSTEM	Main Clock Supply Control Register	MOSCR	8	8	1 to 2PCLK	1 ICLK	Clock Generation Circuit	Not available in 5-V packages.
000A 0C02h	SYSTEM	Main Clock Noise Filter Control Register	MONFCR	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
007F C402h	FLASH	Flash Mode Register	FMODR	8	8	2 to 3 FCLK	2 to 3 ICLK	Flash Memory	
007F C410h	FLASH	Flash Access Status Register	FASTAT	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C411h	FLASH	Flash Access Error Interrupt Enable Register	FAEINT	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C412h	FLASH	Flash Ready Interrupt Enable Register	FRDYIE	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F C440h	FLASH	E2 DataFlash Read Enable Register 0	DFLRE0	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C442h	FLASH	E2 DataFlash Read Enable Register 1	DFLRE1	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C450h	FLASH	E2 DataFlash P/E Enable Register 0	DFLWE0	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F C452h	FLASH	E2 DataFlash P/E Enable Register 1	DFLWE1	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB0h	FLASH	Flash Status Register 0	FSTATR0	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F FFB1h	FLASH	Flash Status Register 1	FSTATR1	8	8	2 to 3 FCLK	2 to 3 ICLK		
007F FFB2h	FLASH	Flash P/E Mode Entry Register	FENTRYR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB4h	FLASH	Flash Protection Register	FPROTR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFB6h	FLASH	Flash Reset Register	FRESETR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFBAh	FLASH	FCU Command Register	FCMDR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFC8h	FLASH	FCU Processing Switching Register	FCPSR	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCAh	FLASH	E2 DataFlash Blank Check Control Register	DFLBCCNT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCCh	FLASH	Flash P/E Status Register	FPESTAT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFCEh	FLASH	E2 DataFlash Blank Check Status Register	DFLBCSTAT	16	16	2 to 3 FCLK	2 to 3 ICLK		
007F FFE8h	FLASH	Peripheral Clock Notification Register	PCKAR	16	16	2 to 3 FCLK	2 to 3 ICLK		

Note: This table lists the I/O registers in both 5-V and 3-V package specifications. The I/O registers of each product correspond to the functions listed in Table 1.2. For details, see Table 1.2, Comparison of Functions of Different RX634 Group Products.
Note: The CEC, RCR0, and RCR1 are not available in 5-V packages.
Note 1. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register.
Note 2. Odd addresses cannot be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMOCNTL register.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings
Conditions: VSS = AVSS0 = VREFL = VREFL0 = 0 V

Item	Symbol	Value	Unit
Power supply voltage	VCC	–0.3 to +6.5	V
Analog power supply voltage	AVCC0*1	–0.3 to +6.5	V
Reference power supply voltage	VREFH0*1	–0.3 to AVCC0 + 0.3	V
	VREFH*1	–0.3 to +6.5	V
Input voltage (except for port 4, ports 03, 05, and 07)	V_{in}	–0.3 to VCC + 0.3	V
Input voltage (port 4, port 07)	V_{in}	–0.3 to AVCC0 + 0.3	V
Input voltage (ports 03, 05)	V_{in}	–0.3 to VREFH + 0.3	V
Analog input voltage (ports 4, E)	V_{AN}	–0.3 to AVCC0 + 0.3	V
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interferences, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, and between the VREFH0 and VREFL0 pins. Place capacitors of 0.1 µF or so as close to every power pin and use the shortest and heaviest possible traces.

Note 1. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

Table 5.3 DC Characteristics (2)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Test Conditions
Input leakage current	RES#, MD input pin, P35/NMI, EXTAL, port 4	$\lvert I_{in} \rvert$	—	—	1.0	μA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports 12, 13, 16, 17, 20, 21, C0, C1	$\lvert I_{TSI} \rvert$	—	—	5.0	μA	V_{in} = 0 V, VCC
	Except for ports 12, 13, 16, 17, 20, 21, C0, C1		—	—	1.0		
	Port L5		—	—	1.8		VCC = 0 V, V_{in} = 3.9 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, C0, C1)	C_{in}	—	—	15	pF	V_{in} = 0 V, f = 1 MHz, T_a = 25°C
	Ports 12, 13, 16, 17, 20, 21, C0, C1		—	—	30		

Table 5.4 DC Characteristics (3)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	VCC				Unit	Test Conditions
			2.7 to 3.6V		4.0 to 5.5V			
			Min.	Max.	Min.	Max.		
Input pull-up MOS current	All ports (except for ports 03, 05, ports 35 to P37, port 4, port L5)	I_p	–200	–10	–400	–50	μA	V_{in} = 0 V

Table 5.5 DC Characteristics (4)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I_{CC}	20	—	mA	ICLK = 54 MHz PCLKB = 27 MHz PCLKD = 54 MHz FCLK = 27 MHz BCLK = 54 MHz
			All peripheral operation: Normal*3	ICLK = 54 MHz		24	—		
			All peripheral operation: Max.*3	ICLK = 54 MHz		—	55		
		Sleep mode	No peripheral operation	ICLK = 54 MHz		15.5	—		
			All peripheral operation: Normal	ICLK = 54 MHz		19.5	—		
		All-module clock stop mode				14	—		
		Increase during BGO operation*4				12	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation.

Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation.

Note 4. This is the increase if data is programmed to or erasing from the ROM or E2 DataFlash during program execution.

5.3.4 Control Signal Timing

Table 5.21 Control Signal Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.11
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.12
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.12

Note: 200 ns minimum in deep software standby and software standby modes.

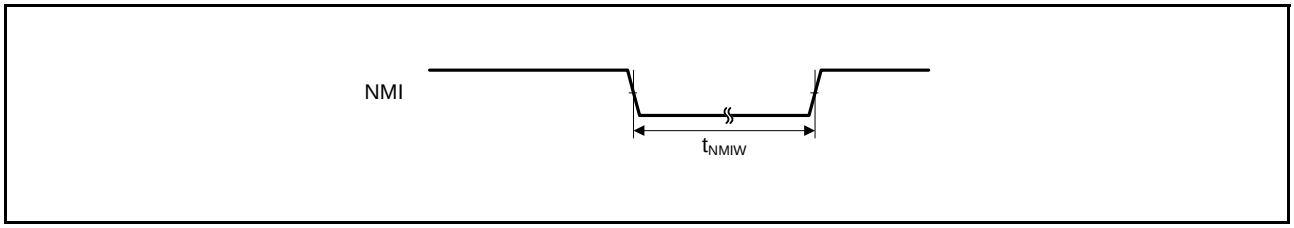


Figure 5.11 NMI Interrupt Input Timing

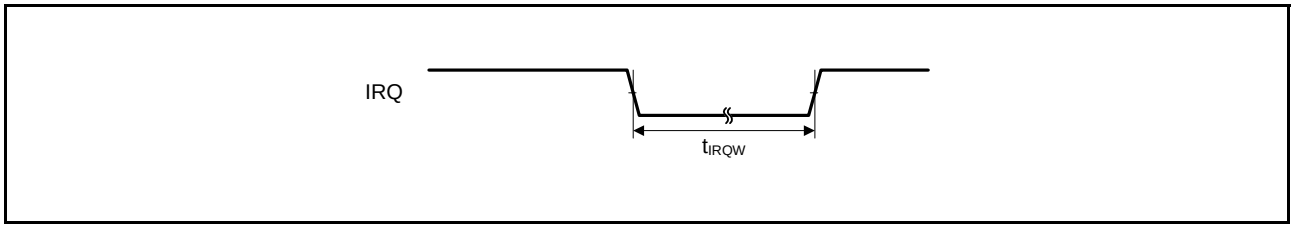


Figure 5.12 IRQ Interrupt Input Timing

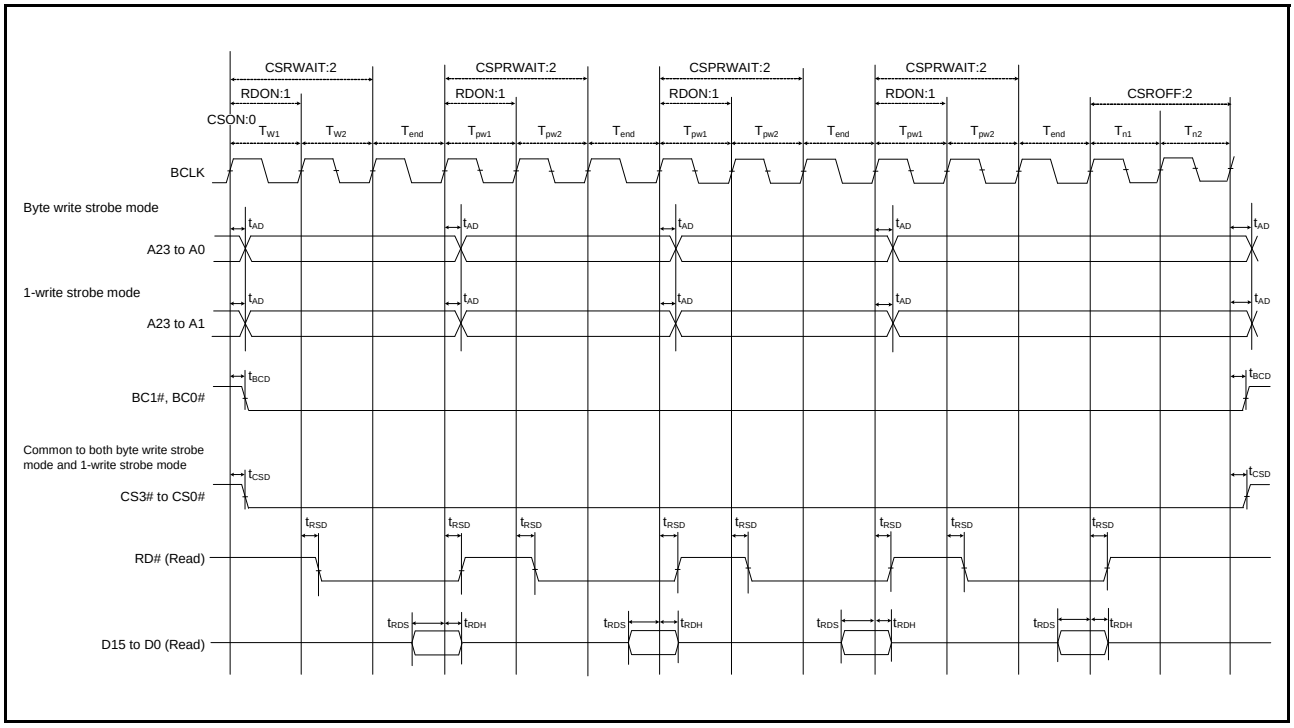
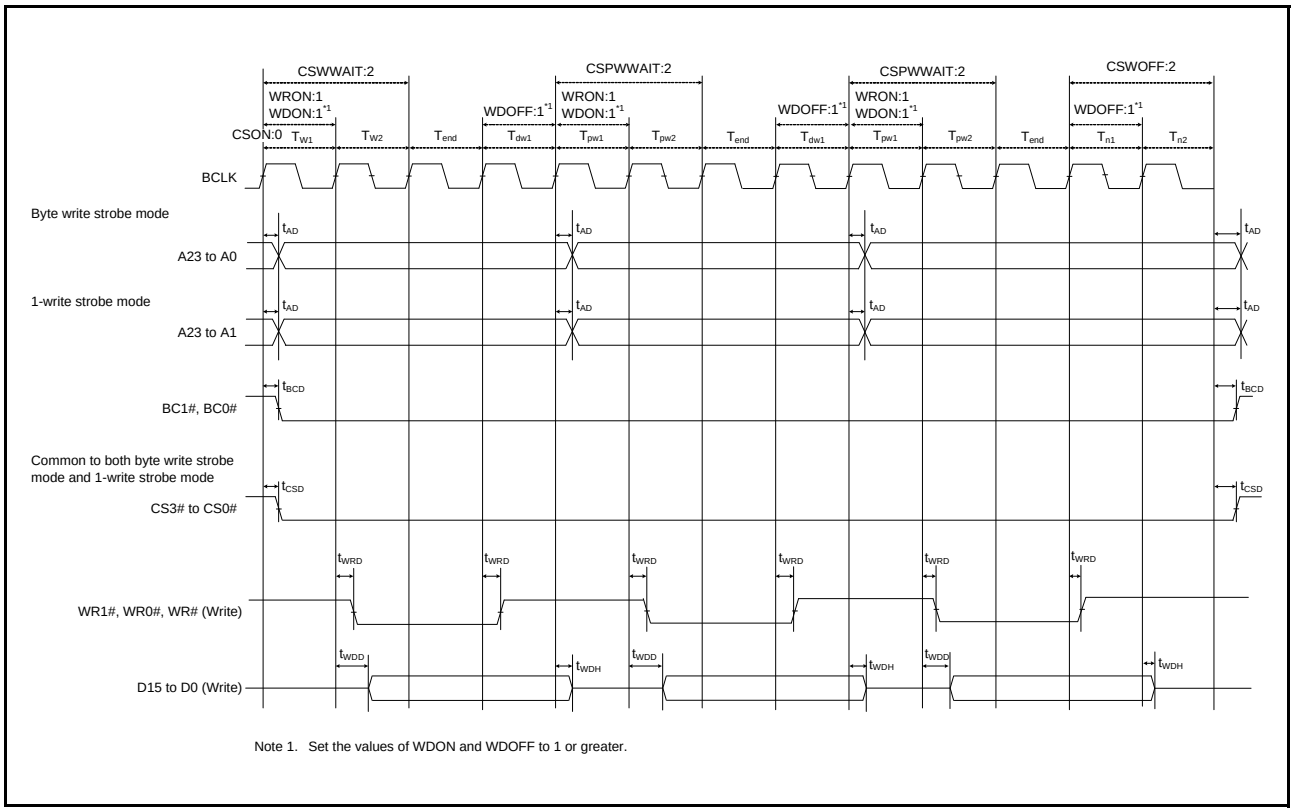


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

Table 5.26 Timing of On-Chip Peripheral Modules (3)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.28
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 5.29 to Figure 5.34
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 5.33, Figure 5.34
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

Table 5.27 Timing of On-Chip Peripheral Modules (4)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.(*1, *2)	Max.	Unit	Test Conditions
RIIC (Standard-mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 5.35
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	1000	—	ns	
	Stop condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast-mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 + 0.1C_b	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 + 0.1C_b	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	Start condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Restart condition input setup time	t_{STAS}	300	—	ns	
	Stop condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference count clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bits = 1.

Note 2. C_b indicates the total capacity of the bus line.

5.5 D/A Conversion Characteristics

Table 5.33 D/A Conversion Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	10	Bit	
Conversion time	—	—	±3.0	µs	20-pF capacitive load
Absolute accuracy	—	±3.0	±5.0	LSB	4-MΩ resistive load
	—	—	±4.0	LSB	8-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	