Renesas Electronics America Inc - R5F5634BYDFB#30 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5634bydfb-30

1.Overview

1.1 Outline of Specifications

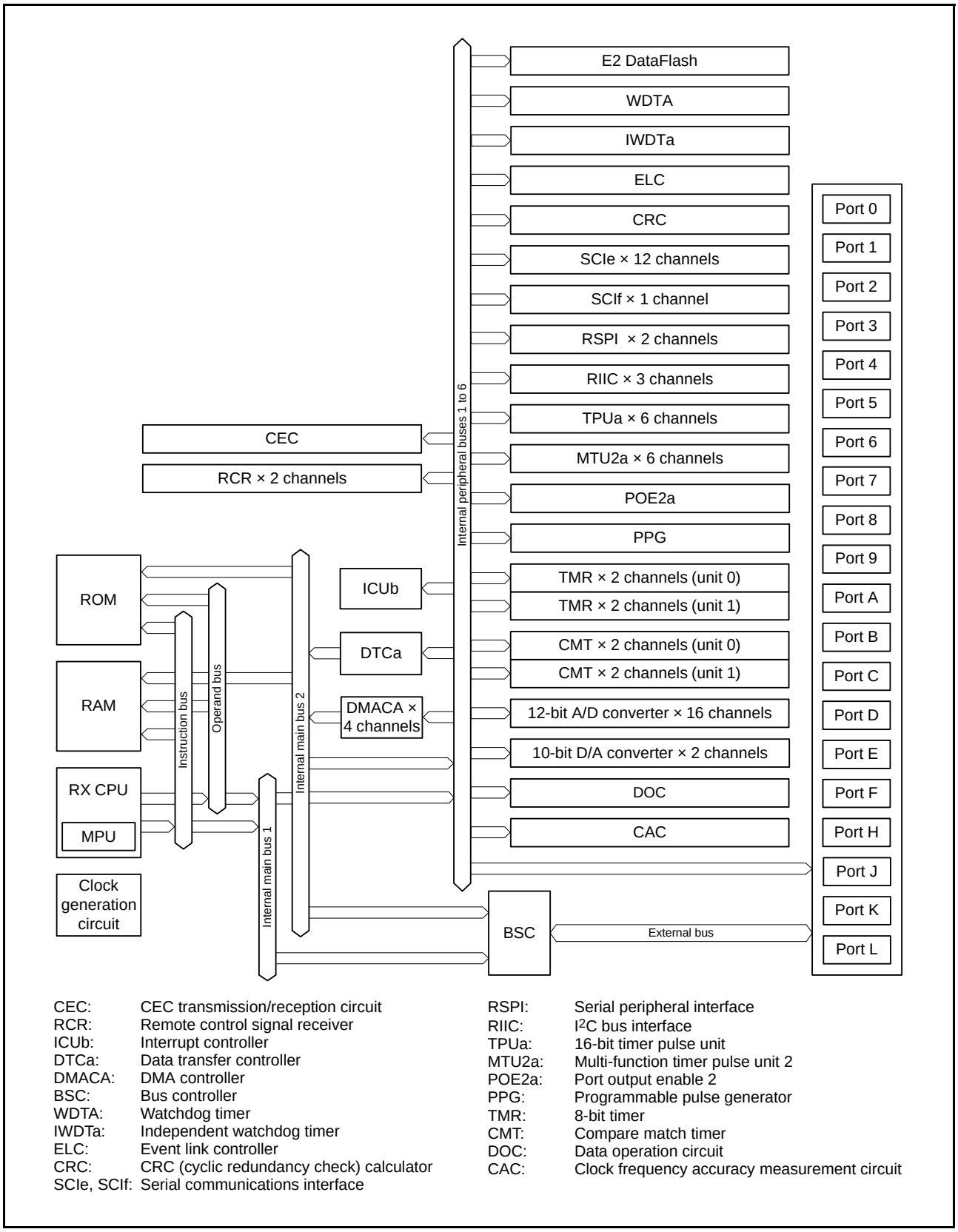
Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1 / 4)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 1 M/1.5 M/2 Mbytes • 54 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 128 Kbytes • 54 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 32 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLKB): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 27 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. The detection voltage level of voltage detection circuit 0 is fixed Voltage detection circuit 1 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 3 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 178 • External interrupts: 14 (NMI, IRQ0 to IRQ12 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

1.3 Block Diagram

Figure 1.2 shows a block diagram.



CEC: CEC transmission/reception circuit
RCR: Remote control signal receiver
ICUb: Interrupt controller
DTCa: Data transfer controller
DMACA: DMA controller
BSC: Bus controller
WDTA: Watchdog timer
IWDTa: Independent watchdog timer
ELC: Event link controller
CRC: CRC (cyclic redundancy check) calculator
SCIe, SCIf: Serial communications interface
RSPI: Serial peripheral interface
RIIC: I^2C bus interface
TPUa: 16-bit timer pulse unit
MTU2a: Multi-function timer pulse unit 2
POE2a: Port output enable 2
PPG: Programmable pulse generator
TMR: 8-bit timer
CMT: Compare match timer
DOC: Data operation circuit
CAC: Clock frequency accuracy measurement circuit

Figure 1.2 Block Diagram

Table 1.4 Pin Functions (2 / 4)

Classifications	Pin Name	I/O	Description
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ12	Input	Interrupt request pins.
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/ PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/ PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/ PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/ PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/ PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/ PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/ PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Programmable pulse generator	PO0 to PO15	Output	Output pins for the pulse signals.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter.
	TMRI0 to TMRI3	Input	Input pins for the counter reset.

Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1 / 4)

Pin No.	Power Supply, Clock, System Control	I/O Port	External Bus	Timers (MTU, TPU, TMR, POE, PPG, CAC)	Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR)	Interrupt	AD, DA
1	AVSS0						
2		P05					DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	
7		P01		TMCI0	RXD6/SMISO6/SSCL6/PMC1	IRQ9	
8		P00		TMRI0	TXD6/SMOSI6/SSDA6/PMC0	IRQ8	
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS0#/RTS0#/SS0#/CTS6#/ RTS6#/SS6#		
14	VCL						
15		PJ1		MTIOC3A			
16	MD/FINED						
17		PJ2					
18		PJ4					
19	RES#						
20	XTAL						
21	VSS						
22	EXTAL						
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMCI3/POE2#/ PO12	SCK0/SCK6	IRQ4	
26		P33		MTIOC0D/TIOCD0/TMRI3/ POE3#/PO11	RXD0/SMISO0/SSCL0/RXD6/ SMISO6/SSCL6	IRQ3_DS	
27		P32		MTIOC0C/TIOCC0/TMO3/ PO10	TXD0/SMOSI0/SSDA0/TXD6/ SMOSI6/SSDA6	IRQ2_DS	
28	TMS	P31		MTIOC4D/TMCI2/PO9	CTS1#/RTS1#/SS1#/SSLB0	IRQ1_DS	
29	TDI	P30		MTIOC4B/TMRI3/POE8#/ PO8	RXD1/SMISO1/SSCL1/MISOB	IRQ0_DS	
30	FINEC/TCK	P27	CS3#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
31	TDO	P26	CS2#	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/CTS3#/ RTS3#/SS3#/MOSIB		
32		P25	CS1#	MTIOC4C/MTCLKB/TIOCA4/ PO5	RXD3/SMISO3/SSCL3		ADTRG0#
33		P24	CS0#	MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4	SCK3		
34		P23		MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/SMOSI3/SSDA3/CTS0#/ RTS0#/SS0#		
35		P22		MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2	SCK0		
36		P21		MTIOC1B/TIOCA3/TMCI0/ PO1	RXD0/SMISO0/SSCL0/SCL1	IRQ9	
37		P20		MTIOC1A/TIOCB3/TMRI0/ PO0	TXD0/SMOSI0/SSDA0/SDA1	IRQ8	
38		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#/PO15	SCK1/TXD3/SMOSI3/SSDA3/ MISOA/SDA0_DS	IRQ7	

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK		Operating Modes	
0008 0002h	SYSTEM	Mode Status Register	MDSR	16	16	3 ICLK			
0008 0006h	SYSTEM	System Control Register 0	SYSCR0	16	16	3 ICLK			
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK			
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK		Low Power Consumption	
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK			
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK			
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK			
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK		Clock Generation Circuit	
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK			
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK			
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK			
0008 0030h	SYSTEM	External Bus Clock Control Register	BCKCR	8	8	3 ICLK			
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK			
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK			
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK			
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK			
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK			
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK		Low Power Consumption	
0008 00A1h	SYSTEM	Sleep Mode Return Clock Source Switching Register	RSTCKCR	8	8	3 ICLK			
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK			
0008 00A6h	SYSTEM	PLL Wait Control Register	PLLWTCR	8	8	3 ICLK			
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK		Resets	
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK			
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK		LVDA	
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK			
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK			
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK			
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK		Register Write Protection Function	
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK		Buses	
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK			
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK			
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK			
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK			
0008 2000h	DMAC0	DMA Source Address Register	DMSAR	32	32	2 ICLK		DMACA	
0008 2004h	DMAC0	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2008h	DMAC0	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 200Ch	DMAC0	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2010h	DMAC0	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2013h	DMAC0	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2014h	DMAC0	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 2018h	DMAC0	DMA Offset Register	DMOFR	32	32	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (7 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK		ICUb	
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK			
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK			
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK			
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK			
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK			
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK			
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK			
0008 70E6h	ICU	Interrupt Request Register 230	IR230	8	8	2 ICLK			
0008 70E7h	ICU	Interrupt Request Register 231	IR231	8	8	2 ICLK			
0008 70E8h	ICU	Interrupt Request Register 232	IR232	8	8	2 ICLK			
0008 70E9h	ICU	Interrupt Request Register 233	IR233	8	8	2 ICLK			
0008 70EAh	ICU	Interrupt Request Register 234	IR234	8	8	2 ICLK			
0008 70EBh	ICU	Interrupt Request Register 235	IR235	8	8	2 ICLK			
0008 70ECh	ICU	Interrupt Request Register 236	IR236	8	8	2 ICLK			
0008 70EDh	ICU	Interrupt Request Register 237	IR237	8	8	2 ICLK			
0008 70EEh	ICU	Interrupt Request Register 238	IR238	8	8	2 ICLK			
0008 70EFh	ICU	Interrupt Request Register 239	IR239	8	8	2 ICLK			
0008 70F0h	ICU	Interrupt Request Register 240	IR240	8	8	2 ICLK			
0008 70F1h	ICU	Interrupt Request Register 241	IR241	8	8	2 ICLK			
0008 70F2h	ICU	Interrupt Request Register 242	IR242	8	8	2 ICLK			
0008 70F3h	ICU	Interrupt Request Register 243	IR243	8	8	2 ICLK			
0008 70F4h	ICU	Interrupt Request Register 244	IR244	8	8	2 ICLK			
0008 70F5h	ICU	Interrupt Request Register 245	IR245	8	8	2 ICLK			
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK			
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK			
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK			
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK			
0008 70FAh	ICU	Interrupt Request Register 250	IR250	8	8	2 ICLK			
0008 70FBh	ICU	Interrupt Request Register 251	IR251	8	8	2 ICLK			
0008 70FCh	ICU	Interrupt Request Register 252	IR252	8	8	2 ICLK			
0008 70FDh	ICU	Interrupt Request Register 253	IR253	8	8	2 ICLK			
0008 711Bh	ICU	DTC Activation Enable Register 027	DTCER027	8	8	2 ICLK			
0008 711Ch	ICU	DTC Activation Enable Register 028	DTCER028	8	8	2 ICLK			
0008 711Dh	ICU	DTC Activation Enable Register 029	DTCER029	8	8	2 ICLK			
0008 711Eh	ICU	DTC Activation Enable Register 030	DTCER030	8	8	2 ICLK			
0008 711Fh	ICU	DTC Activation Enable Register 031	DTCER031	8	8	2 ICLK			
0008 712Dh	ICU	DTC Activation Enable Register 045	DTCER045	8	8	2 ICLK			
0008 712Eh	ICU	DTC Activation Enable Register 046	DTCER046	8	8	2 ICLK			
0008 7131h	ICU	DTC Activation Enable Register 049	DTCER049	8	8	2 ICLK			
0008 7132h	ICU	DTC Activation Enable Register 050	DTCER050	8	8	2 ICLK			
0008 7140h	ICU	DTC Activation Enable Register 064	DTCER064	8	8	2 ICLK			
0008 7141h	ICU	DTC Activation Enable Register 065	DTCER065	8	8	2 ICLK			
0008 7142h	ICU	DTC Activation Enable Register 066	DTCER066	8	8	2 ICLK			
0008 7143h	ICU	DTC Activation Enable Register 067	DTCER067	8	8	2 ICLK			
0008 7144h	ICU	DTC Activation Enable Register 068	DTCER068	8	8	2 ICLK			
0008 7145h	ICU	DTC Activation Enable Register 069	DTCER069	8	8	2 ICLK			
0008 7146h	ICU	DTC Activation Enable Register 070	DTCER070	8	8	2 ICLK			
0008 7147h	ICU	DTC Activation Enable Register 071	DTCER071	8	8	2 ICLK			
0008 7148h	ICU	DTC Activation Enable Register 072	DTCER072	8	8	2 ICLK			
0008 7149h	ICU	DTC Activation Enable Register 073	DTCER073	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (11 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 734Bh	ICU	Interrupt Source Priority Register 075	IPR075	8	8	2 ICLK		ICUb	
0008 734Ch	ICU	Interrupt Source Priority Register 076	IPR076	8	8	2 ICLK			
0008 734Dh	ICU	Interrupt Source Priority Register 077	IPR077	8	8	2 ICLK			Not available in 5-V packages.
0008 734Eh	ICU	Interrupt Source Priority Register 078	IPR078	8	8	2 ICLK			Not available in 5-V packages.
0008 734Fh	ICU	Interrupt Source Priority Register 079	IPR079	8	8	2 ICLK			Not available in 5-V packages.
0008 735Eh	ICU	Interrupt Source Priority Register 094	IPR094	8	8	2 ICLK			Not available in 5-V packages.
0008 735Fh	ICU	Interrupt Source Priority Register 095	IPR095	8	8	2 ICLK			Not available in 5-V packages.
0008 7362h	ICU	Interrupt Source Priority Register 098	IPR098	8	8	2 ICLK			
0008 7363h	ICU	Interrupt Source Priority Register 099	IPR099	8	8	2 ICLK			
0008 7364h	ICU	Interrupt Source Priority Register 100	IPR100	8	8	2 ICLK			
0008 7365h	ICU	Interrupt Source Priority Register 101	IPR101	8	8	2 ICLK			
0008 7366h	ICU	Interrupt Source Priority Register 102	IPR102	8	8	2 ICLK			
0008 7367h	ICU	Interrupt Source Priority Register 103	IPR103	8	8	2 ICLK			
0008 736Ah	ICU	Interrupt Source Priority Register 106	IPR106	8	8	2 ICLK			
0008 736Bh	ICU	Interrupt Source Priority Register 107	IPR107	8	8	2 ICLK			
0008 736Fh	ICU	Interrupt Source Priority Register 111	IPR111	8	8	2 ICLK			Not available in 5-V packages.
0008 7372h	ICU	Interrupt Source Priority Register 114	IPR114	8	8	2 ICLK			
0008 7376h	ICU	Interrupt Source Priority Register 118	IPR118	8	8	2 ICLK			
0008 7379h	ICU	Interrupt Source Priority Register 121	IPR121	8	8	2 ICLK			
0008 737Bh	ICU	Interrupt Source Priority Register 123	IPR123	8	8	2 ICLK			
0008 737Dh	ICU	Interrupt Source Priority Register 125	IPR125	8	8	2 ICLK			
0008 737Fh	ICU	Interrupt Source Priority Register 127	IPR127	8	8	2 ICLK			
0008 7381h	ICU	Interrupt Source Priority Register 129	IPR129	8	8	2 ICLK			
0008 7385h	ICU	Interrupt Source Priority Register 133	IPR133	8	8	2 ICLK			
0008 7386h	ICU	Interrupt Source Priority Register 134	IPR134	8	8	2 ICLK			
0008 738Ah	ICU	Interrupt Source Priority Register 138	IPR138	8	8	2 ICLK			
0008 738Bh	ICU	Interrupt Source Priority Register 139	IPR139	8	8	2 ICLK			
0008 738Eh	ICU	Interrupt Source Priority Register 142	IPR142	8	8	2 ICLK			
0008 7392h	ICU	Interrupt Source Priority Register 146	IPR146	8	8	2 ICLK			
0008 7393h	ICU	Interrupt Source Priority Register 147	IPR147	8	8	2 ICLK			
0008 7395h	ICU	Interrupt Source Priority Register 149	IPR149	8	8	2 ICLK			
0008 7397h	ICU	Interrupt Source Priority Register 151	IPR151	8	8	2 ICLK			
0008 7399h	ICU	Interrupt Source Priority Register 153	IPR153	8	8	2 ICLK			
0008 739Bh	ICU	Interrupt Source Priority Register 155	IPR155	8	8	2 ICLK			
0008 739Fh	ICU	Interrupt Source Priority Register 159	IPR159	8	8	2 ICLK			
0008 73A0h	ICU	Interrupt Source Priority Register 160	IPR160	8	8	2 ICLK			
0008 73A2h	ICU	Interrupt Source Priority Register 162	IPR162	8	8	2 ICLK			
0008 73A4h	ICU	Interrupt Source Priority Register 164	IPR164	8	8	2 ICLK			
0008 73A6h	ICU	Interrupt Source Priority Register 166	IPR166	8	8	2 ICLK			
0008 73AAh	ICU	Interrupt Source Priority Register 170	IPR170	8	8	2 ICLK			
0008 73ABh	ICU	Interrupt Source Priority Register 171	IPR171	8	8	2 ICLK			
0008 73AEh	ICU	Interrupt Source Priority Register 174	IPR174	8	8	2 ICLK			
0008 73B1h	ICU	Interrupt Source Priority Register 177	IPR177	8	8	2 ICLK			
0008 73B4h	ICU	Interrupt Source Priority Register 180	IPR180	8	8	2 ICLK			
0008 73B7h	ICU	Interrupt Source Priority Register 183	IPR183	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (13 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 750Eh	CEC	CEC Interrupt Control Register 2	CECINTCR2	8	8	2 ICLK		CEC	Not available in 5-V packages.
0008 750Fh	CEC	CEC Interrupt Control Register 3	CECINTCR3	8	8	2 ICLK			Not available in 5-V packages.
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK		ICUb	
0008 7511h	ICU	IRQ Pin Digital Filter Enable Register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ Pin Digital Filter Setting Register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK			
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 to 3PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 to 3PCLKB	2 ICLK		
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 to 3PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 to 3PCLKB	2 ICLK		
0008 8020h	WDT	WDT Refresh Register	WDTRR	8	8	2 to 3PCLKB	2 ICLK	WDTA	
0008 8022h	WDT	WDT Control Register	WDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8024h	WDT	WDT Status Register	WDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8026h	WDT	WDT Reset Control Register	WDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 to 3PCLKB	2 ICLK	IWDTa	
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 to 3PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 to 3PCLKB	2 ICLK		
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 to 3PCLKB	2 ICLK	DAa	
0008 80C2h	DA	D/A Data Register 1	DADR1	16	16	2 to 3PCLKB	2 ICLK		
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 to 3PCLKB	2 ICLK		
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 to 3PCLKB	2 ICLK		
0008 8100h	TPU	Timer Start Register	TSTR	8	8	2 to 3PCLKB	2 ICLK	TPUa	
0008 8101h	TPU	Timer Synchronous Register	TSYR	8	8	2 to 3PCLKB	2 ICLK		
0008 8108h	TPU0	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8109h	TPU1	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ah	TPU2	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Bh	TPU3	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Ch	TPU4	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 810Dh	TPU5	Noise Filter Control Register	NFCR	8	8	2 to 3PCLKB	2 ICLK		
0008 8110h	TPU0	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (16 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8310h	RIIC0	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8311h	RIIC0	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8312h	RIIC0	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8313h	RIIC0	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8320h	RIIC1	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8321h	RIIC1	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8322h	RIIC1	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8323h	RIIC1	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8324h	RIIC1	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8325h	RIIC1	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8326h	RIIC1	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8327h	RIIC1	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8328h	RIIC1	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8329h	RIIC1	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8330h	RIIC1	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8331h	RIIC1	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8332h	RIIC1	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8333h	RIIC1	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8360h	RIIC3	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8361h	RIIC3	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8362h	RIIC3	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8363h	RIIC3	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8364h	RIIC3	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8365h	RIIC3	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8366h	RIIC3	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8367h	RIIC3	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8368h	RIIC3	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8369h	RIIC3	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 836Ch	RIIC3	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Dh	RIIC3	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Eh	RIIC3	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (25 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 B126h	ELC	Port Group Control Register 2	PGC2	8	8	2 to 3PCLKB	2 ICLK	ELC	
0008 B127h	ELC	Port Buffer Register 1	PDBF1	8	8	2 to 3PCLKB	2 ICLK		
0008 B128h	ELC	Port Buffer Register 2	PDBF2	8	8	2 to 3PCLKB	2 ICLK		
0008 B129h	ELC	Event Link Port Setting Register 0	PEL0	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ah	ELC	Event Link Port Setting Register 1	PEL1	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Bh	ELC	Event Link Port Setting Register 2	PEL2	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Ch	ELC	Event Link Port Setting Register 3	PEL3	8	8	2 to 3PCLKB	2 ICLK		
0008 B12Dh	ELC	Event Link Software Event Generation Register	ELSEGR	8	8	2 to 3PCLKB	2 ICLK		
0008 B300h	SCI12	Serial Mode Register	SMR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 B301h	SCI12	Bit Rate Register	BRR	8	8	2 to 3PCLKB	2 ICLK		
0008 B302h	SCI12	Serial Control Register	SCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B303h	SCI12	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B304h	SCI12	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 B305h	SCI12	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 B306h	SCI12	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B307h	SCI12	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B308h	SCI12	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 B309h	SCI12	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ah	SCI12	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Bh	SCI12	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Ch	SCI12	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 B30Dh	SCI12	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B320h	SCI12	Extended Serial Module Enable Register	ESMER	8	8	2 to 3PCLKB	2 ICLK		
0008 B321h	SCI12	Control Register 0	CR0	8	8	2 to 3PCLKB	2 ICLK		
0008 B322h	SCI12	Control Register 1	CR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B323h	SCI12	Control Register 2	CR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B324h	SCI12	Control Register 3	CR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B325h	SCI12	Port Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B326h	SCI12	Interrupt Control Register	ICR	8	8	2 to 3PCLKB	2 ICLK		
0008 B327h	SCI12	Status Register	STR	8	8	2 to 3PCLKB	2 ICLK		
0008 B328h	SCI12	Status Clear Register	STCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B329h	SCI12	Control Field 0 Data Register	CF0DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ah	SCI12	Control Field 0 Compare Enable Register	CF0CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Bh	SCI12	Control Field 0 Receive Data Register	CF0RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Ch	SCI12	Primary Control Field 1 Data Register	PCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Dh	SCI12	Secondary Control Field 1 Data Register	SCF1DR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Eh	SCI12	Control Field 1 Compare Enable Register	CF1CR	8	8	2 to 3PCLKB	2 ICLK		
0008 B32Fh	SCI12	Control Field 1 Receive Data Register	CF1RR	8	8	2 to 3PCLKB	2 ICLK		
0008 B330h	SCI12	Timer Control Register	TCR	8	8	2 to 3PCLKB	2 ICLK		
0008 B331h	SCI12	Timer Mode Register	TMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B332h	SCI12	Timer Prescaler Register	TPRE	8	8	2 to 3PCLKB	2 ICLK		
0008 B333h	SCI12	Timer Count Register	TCNT	8	8	2 to 3PCLKB	2 ICLK		
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 to 3PCLKB	2 ICLK		

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	VCC + 0.3	V	
	Port 4, port 07		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05		VREFH × 0.8	—	VREFH + 0.3		
	Port L5		VCC × 0.8	—	3.9		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (except for SMBus)	V_{IL}	–0.3	—	VCC × 0.3		
	Port 4, port 07		–0.3	—	AVCC0 × 0.2		
	Port 03, 05		–0.3	—	VREFH × 0.2		
	Port L5		–0.3	—	VCC × 0.2		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		–0.3	—	VCC × 0.2		
	RIIC input pin (except for SMBus)	ΔV_T	VCC × 0.05	—	—		
	Port 4, port 07		AVCC0 × 0.06	—	—		
	Ports 03, 05		VREFH × 0.06	—	—		
	Port L5		VCC × 0.06	—	—		Conditions 1
	Except for RIIC input pin, port 4, ports 03, 05, 07, port L5		VCC × 0.06	—	—		
Input level voltage (except for schmitt trigger input pins)	MD, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, WAIT#, TCK, RSPI input pin		VCC × 0.8	—	VCC + 0.3		
	D0 to D15		VCC × 0.7	—	VCC + 0.3		
	RIIC input pin (SMBus)		2.1	—	VCC + 0.3		Conditions 1
	CEC input pin		2.0	—	3.9		Conditions 1
	MD, EMLE	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL, WAIT#, TCK, RSPI input pin		–0.3	—	VCC × 0.2		
	D0 to D15		–0.3	—	VCC × 0.3		
	RIIC input pin (SMBus)		–0.3	—	0.8		Conditions 1
	CEC input pin		–0.3	—	0.8		Conditions 1
	CEC input pin	ΔV_T	—	0.3	—		Conditions 1

Table 5.6 DC Characteristics (5)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*2	ICLK = 1 MHz	I_{CC}	4	—	mA	
			All peripheral operation: Normal*3	ICLK = 1 MHz		4.2	—		
			All peripheral operation: Max.*3	ICLK = 1 MHz		—	15		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		3.8	—		
			All peripheral operation: Normal	ICLK = 1 MHz		4.0	—		
		All-module clock stop mode				3.7	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*4	ICLK = 125 kHz		0.4	—		
			All peripheral operation: Normal*5	ICLK = 125 kHz		0.5	—		
			All peripheral operation: Max.*5	ICLK = 125 kHz		—	8*6		
		Sleep mode	No peripheral operation	ICLK = 125 kHz		0.3	—		
			All peripheral operation: Normal	ICLK = 125 kHz		0.4	—		
		All-module clock stop mode				0.28	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main clock.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main clock.
Note 4. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is LOCO.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is LOCO.
Note 6. Value when the main clock continues oscillating at 13.5 MHz.

Table 5.7 DC Characteristics (6)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply power*1	Software standby mode			I_{CC}	40	1000	µA	
	Deep software standby mode	RAM power supplied			22	200		
		RAM power not supplied	Power-on reset circuit low power consumption function disabled		21	60		
			Power-on reset circuit low power consumption function enabled		6.2	28		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Table 5.12 Output Values of Voltage (1)

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output	V_{OL}	—	0.5	V	I_{OL} = 1.0 mA
		High-drive output		—	0.5		I_{OL} = 2.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
	CEC pins			—	0.6		I_{OL} = 2.1 mA
Output high	All output pins	Normal output	V_{OH}	VCC – 0.5	—	V	I_{OH} = –1.0 mA
		High-drive output		VCC – 0.5	—		I_{OH} = –2.0 mA

Table 5.13 Output Values of Voltage (2)

Conditions: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output pins (other than RIIC)	Normal output	V_{OL}	—	0.8	V	I_{OL} = 2.0 mA
		High-drive output		—	0.8		I_{OL} = 4.0 mA
	RIIC pins			—	0.4		I_{OL} = 3.0 mA
				—	0.6		I_{OL} = 6.0 mA
Output high	All output pins	Normal output	V_{OH}	VCC – 0.8	—	V	I_{OH} = –2.0 mA
		High-drive output		VCC – 0.8	—		I_{OH} = –4.0 mA

5.3.4 Control Signal Timing

Table 5.21 Control Signal Timing

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.11
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.11
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_{c\ (PCLKB)}$× 2 ≤ 200ns, Figure 5.12
		$t_{c\ (PCLKB)}$ × 2	—	—	ns	$t_{c\ (PCLKB)}$× 2 > 200ns, Figure 5.12

Note: 200 ns minimum in deep software standby and software standby modes.

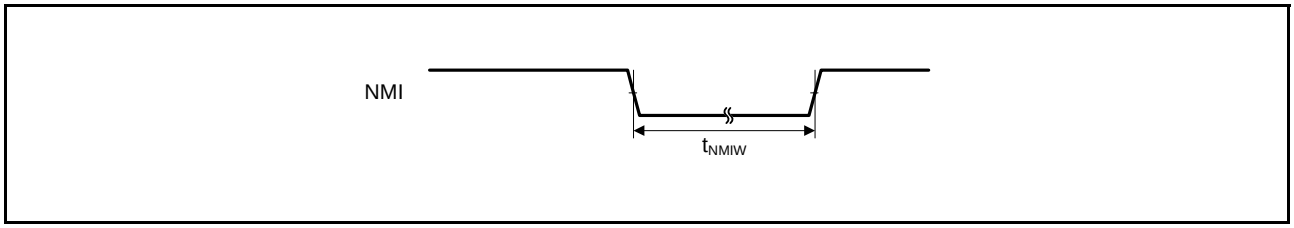


Figure 5.11 NMI Interrupt Input Timing

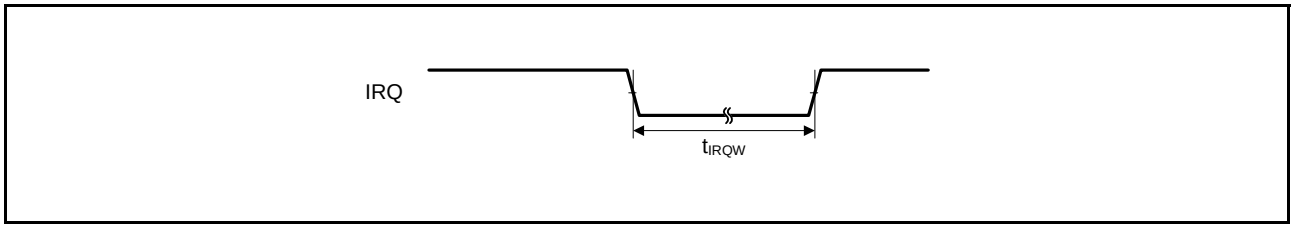


Figure 5.12 IRQ Interrupt Input Timing

Table 5.25 Timing of On-Chip Peripheral Modules (2)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.28
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/ fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	µs	
	Data input setup time	Master		t_{SU}	15	—	ns	Figure 5.29 to Figure 5.34
		Slave			$20 - t_{Pcyc}$	—		
	Data input hold time	Master	PCLKB set to a division ratio other than divided by 2	t_H	t_{Pcyc}	—	ns	
			PCLKB set to divided by 2		0	—		
		Slave			$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{Pcyc}	
	Data output delay time	Master		t_{OD}	—	18	ns	
		Slave			—	$3 \times t_{Pcyc} + 40$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/ fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	µs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	µs	
	Slave access time			t_{SA}	—	4	t_{Pcyc}	Figure 5.33, Figure 5.34
	Slave output release time			t_{REL}	—	3	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

Table 5.26 Timing of On-Chip Peripheral Modules (3)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	65536	t_{Pcyc}	Figure 5.28
	SCK clock cycle input (slave)		8	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	40	—	ns	Figure 5.29 to Figure 5.34
	Data input hold time	t_H	40	—	ns	
	SS input setup time	t_{LEAD}	6	—	t_{Pcyc}	
	SS input hold time	t_{LAG}	6	—	t_{Pcyc}	
	Data output delay time	t_{OD}	—	40	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	20	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 5.33, Figure 5.34
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLKB cycle

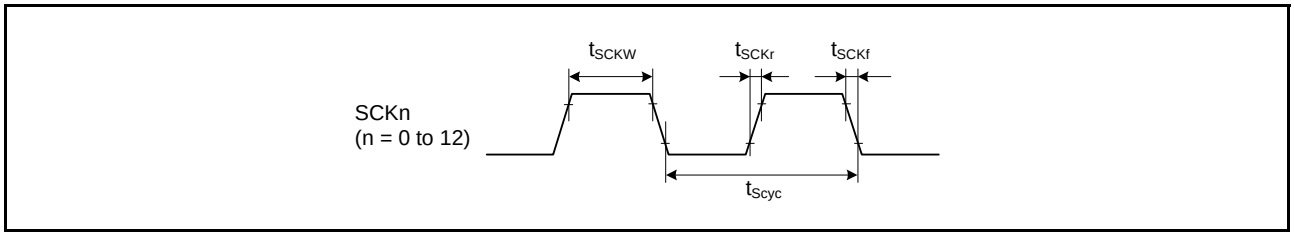


Figure 5.25 SCK Clock Input Timing

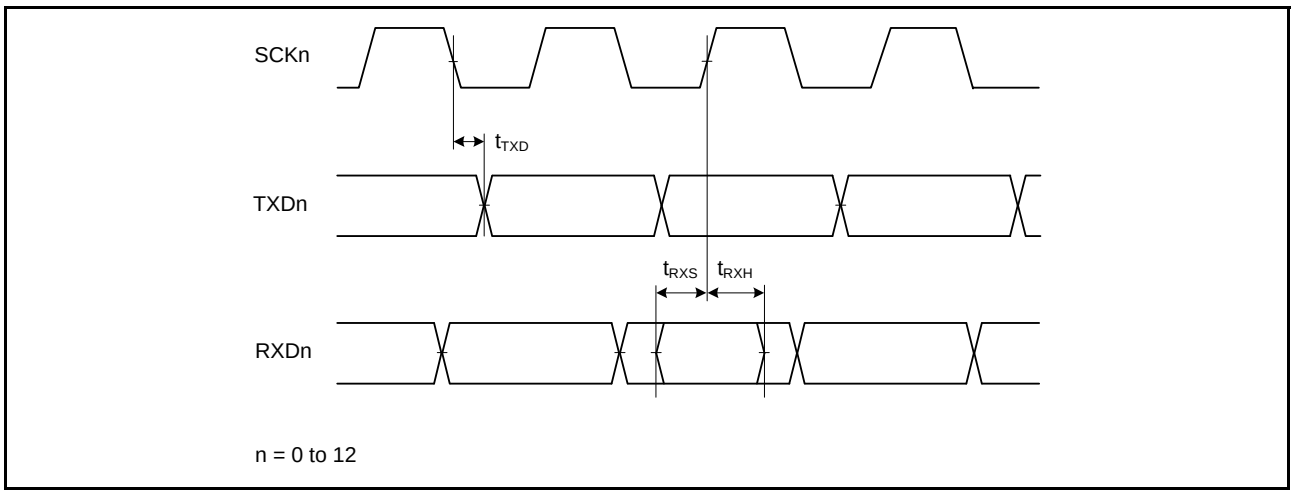


Figure 5.26 SCI Input/Output Timing: Clock Synchronous Mode

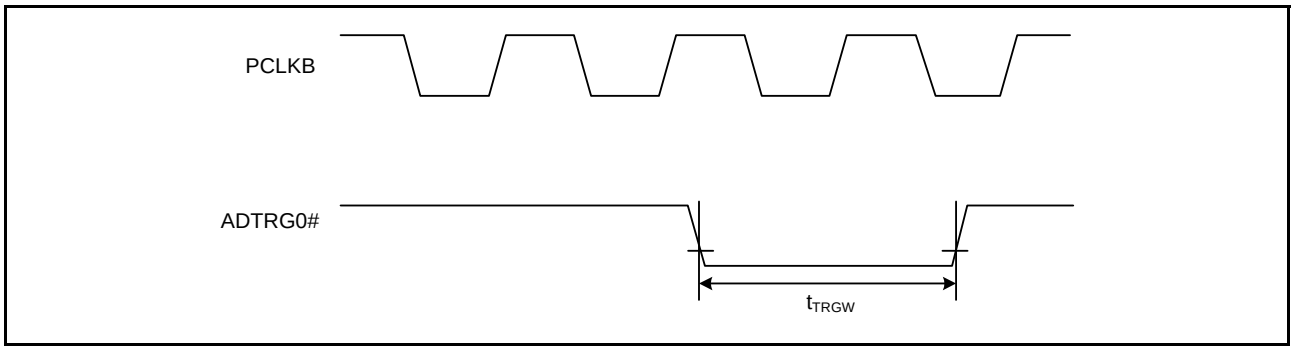


Figure 5.27 A/D Converter External Trigger Input Timing

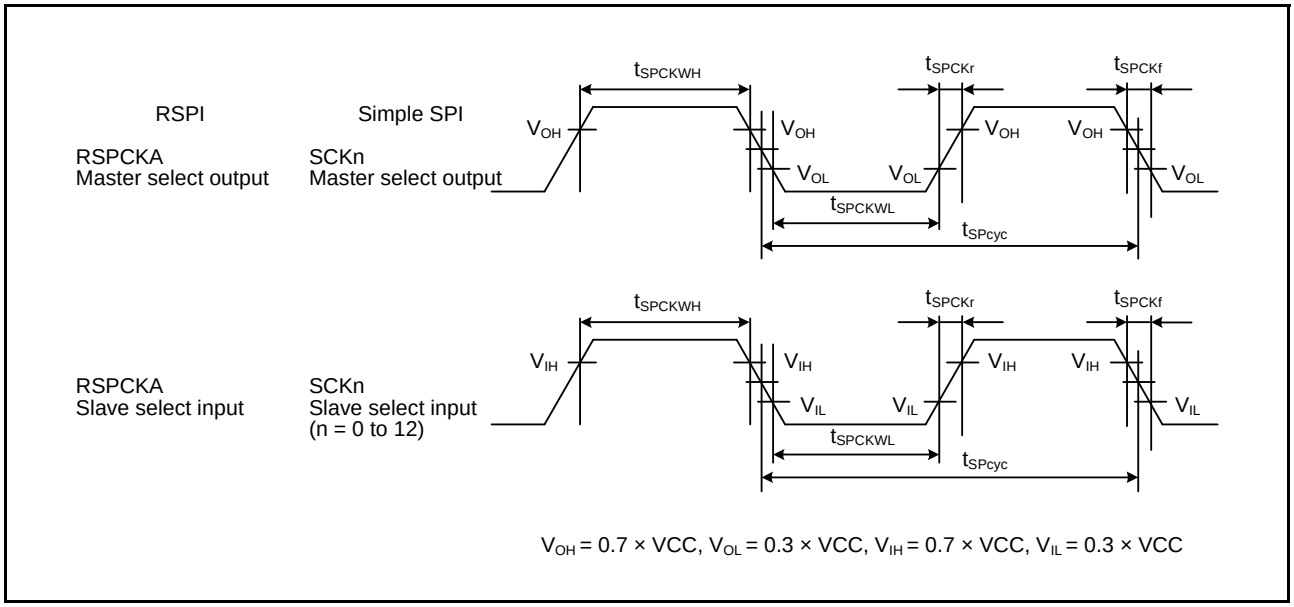


Figure 5.28 RSPI Clock Timing and Simple SPI Clock Timing

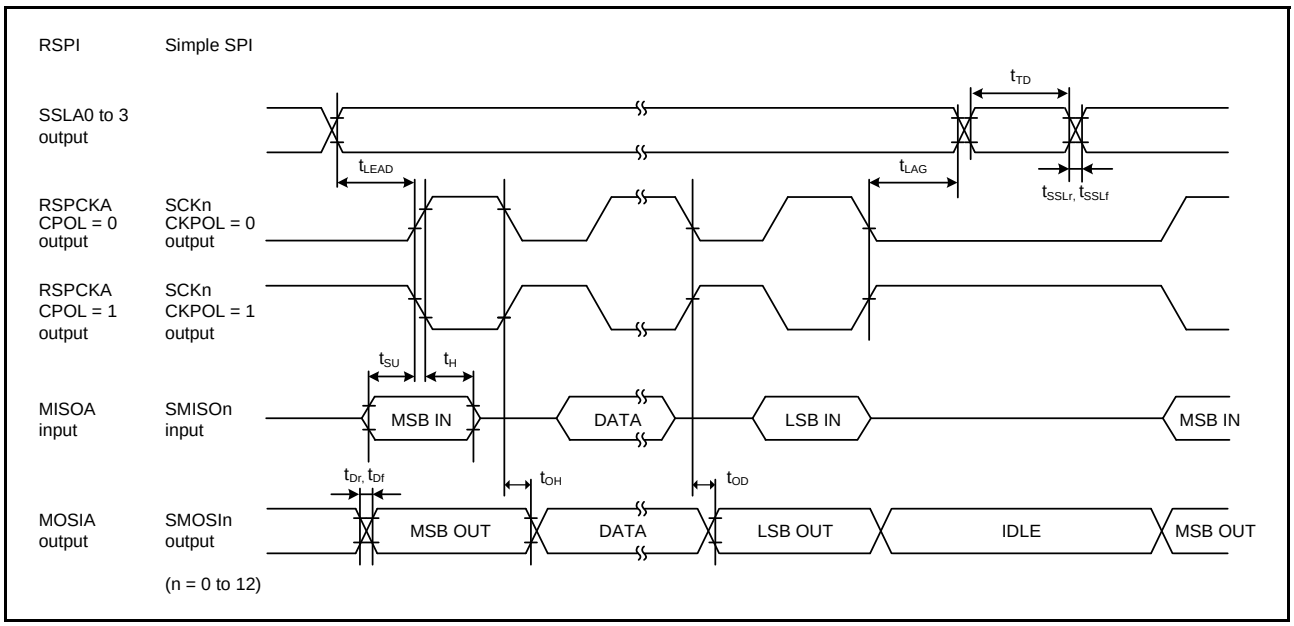


Figure 5.29 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKB Set to Division Ratio Other Than Divided by 2) and Simple SPI Timing (Master, CKPH = 1)

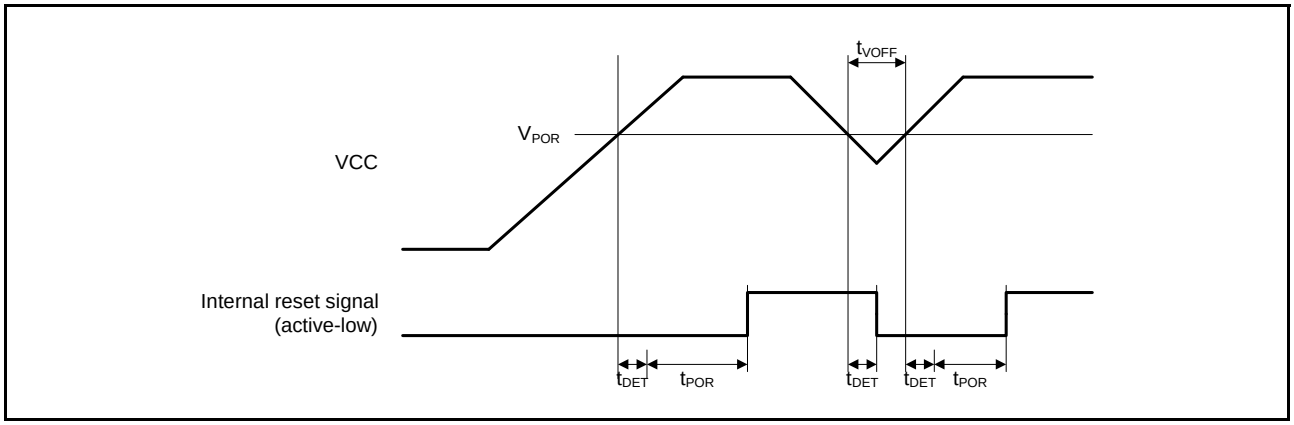


Figure 5.38 Power-on Reset Timing

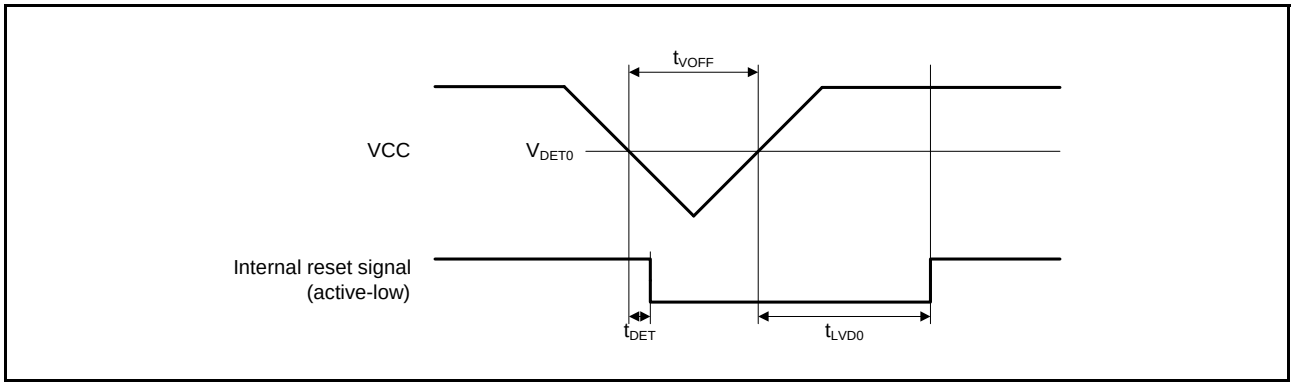
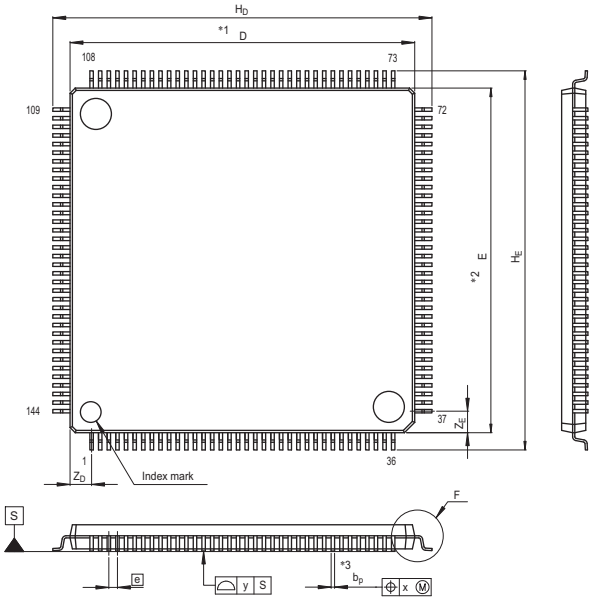


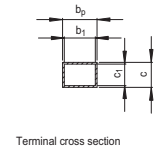
Figure 5.39 Voltage Detection Circuit Timing (V_{DET0})

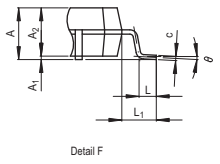
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)