Renesas Electronics America Inc - R5F5634DCDFB#30 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	54MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5634dcdfb-30

1.Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline.

Table 1.1 Outline of Specifications (1 / 4)

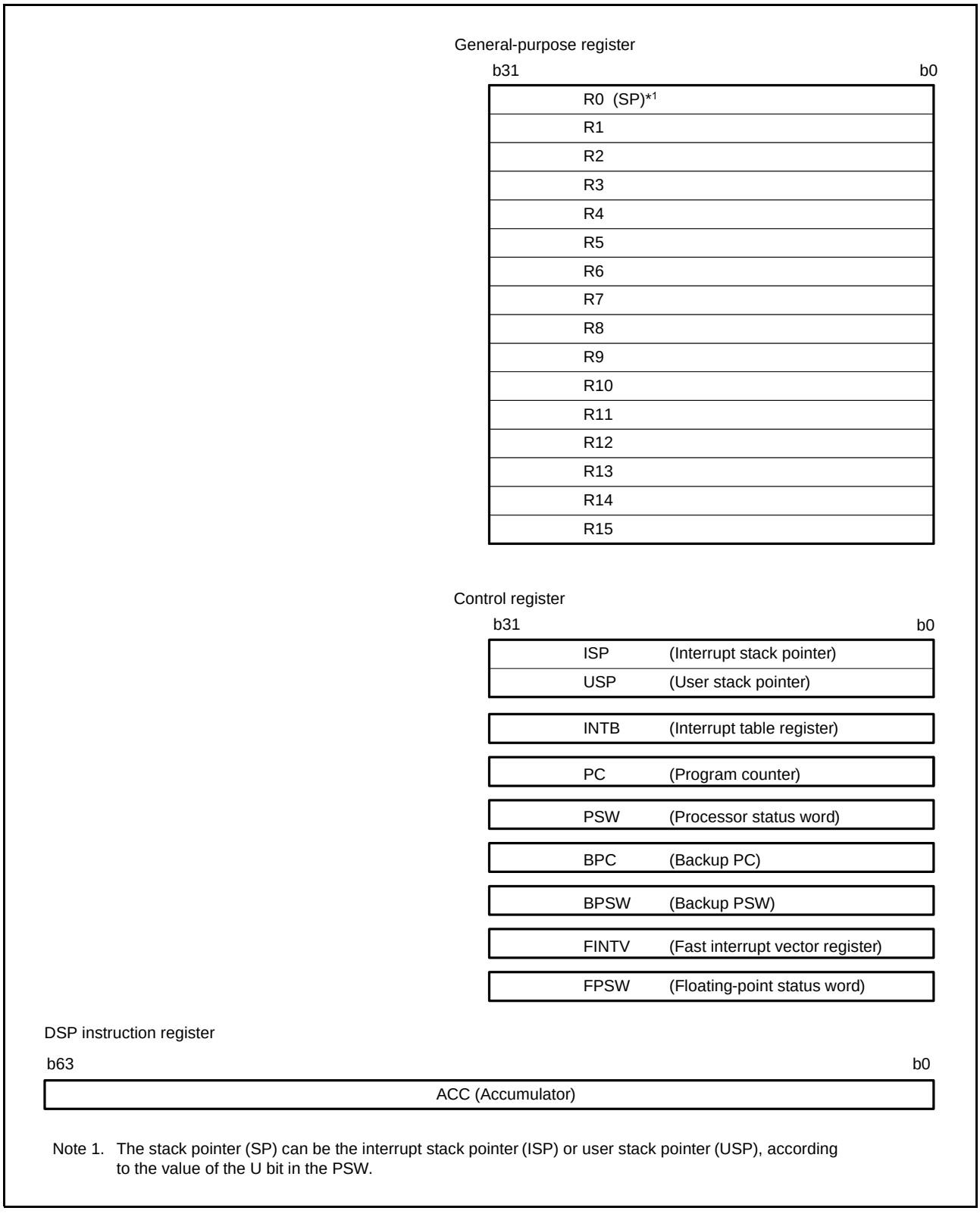
Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 54 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • Memory-protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: 1 M/1.5 M/2 Mbytes • 54 MHz, no-wait memory access • On-board programming: 3 types Off-board programming
	RAM	• Capacity: 128 Kbytes • 54 MHz, no-wait memory access
	E2 DataFlash	• Capacity: 32 Kbytes • Number of times for programming/erasing: 100,000
MCU operating mode		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, low-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection • Measuring circuit for accuracy of clock frequency (clock-accuracy check: CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLKB), external bus clock (BCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 54 MHz (at max.) Peripheral modules run in synchronization with the peripheral module clock (PCLKB): 32 MHz (at max.) Devices connected to the external bus run in synchronization with the external bus clock (BCLK): 27 MHz (at max.) The flash peripheral circuit runs in synchronization with the FlashIF clock (FCLK): 32 MHz (at max.)
Reset		RES# pin reset, power-on reset, voltage monitoring reset, watchdog timer reset, independent watchdog timer reset, deep software standby reset, and software reset
Voltage detection	Voltage detection circuit	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. The detection voltage level of voltage detection circuit 0 is fixed Voltage detection circuit 1 is capable of selecting the detection voltage from 3 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 3 levels
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, low-speed operating mode 1, low-speed operating mode 2
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 178 • External interrupts: 14 (NMI, IRQ0 to IRQ12 pins) • Non-maskable interrupts: 6 (the NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, WDT interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (4 / 4)

Classification	Module/Function	Description
Power supply voltage		• 3-V package VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V • 5-V package VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V
Operating temperature		–40 to +85°C (products with wide-temperature-range spec.)
Packages		144-pin LQFP (PLQP0144KA-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

2. CPU

Figure 2.1 shows the register set of the CPU.



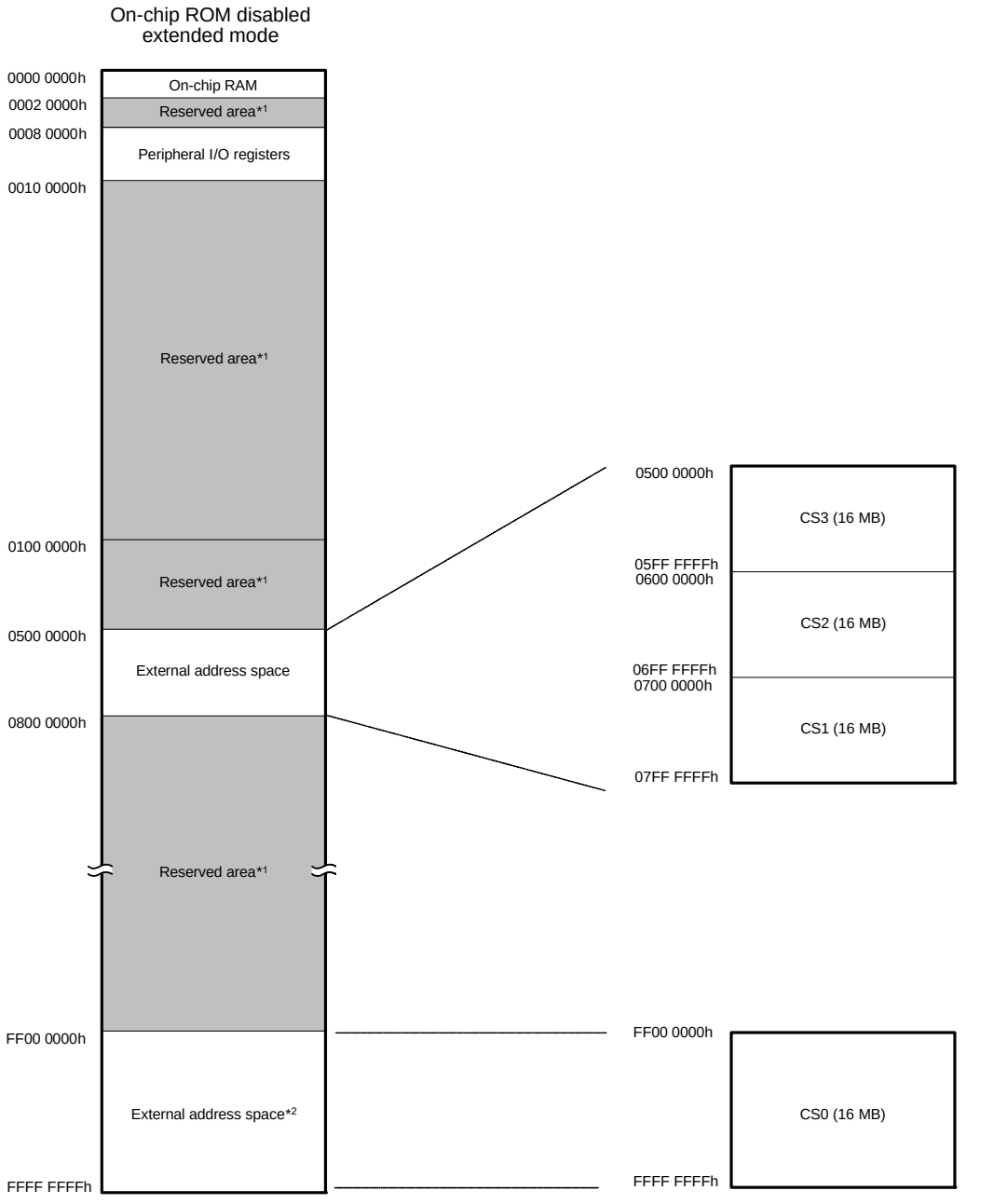
Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW.

Figure 2.1 Register Set of the CPU

3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.



Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

Table 4.1 List of I/O Registers (Address Order) (2 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 201Ch	DMAC0	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK		DMACA	
0008 201Dh	DMAC0	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 201Eh	DMAC0	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 201Fh	DMAC0	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2040h	DMAC1	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2044h	DMAC1	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2048h	DMAC1	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 204Ch	DMAC1	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2050h	DMAC1	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2053h	DMAC1	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2054h	DMAC1	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 205Ch	DMAC1	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 205Dh	DMAC1	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 205Eh	DMAC1	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 205Fh	DMAC1	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2080h	DMAC2	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 2084h	DMAC2	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 2088h	DMAC2	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 208Ch	DMAC2	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 2090h	DMAC2	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 2093h	DMAC2	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 2094h	DMAC2	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 209Ch	DMAC2	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 209Dh	DMAC2	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 209Eh	DMAC2	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 209Fh	DMAC2	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 20C0h	DMAC3	DMA Source Address Register	DMSAR	32	32	2 ICLK			
0008 20C4h	DMAC3	DMA Destination Address Register	DMDAR	32	32	2 ICLK			
0008 20C8h	DMAC3	DMA Transfer Count Register	DMCRA	32	32	2 ICLK			
0008 20CCh	DMAC3	DMA Block Transfer Count Register	DMCRB	16	16	2 ICLK			
0008 20D0h	DMAC3	DMA Transfer Mode Register	DMTMD	16	16	2 ICLK			
0008 20D3h	DMAC3	DMA Interrupt Setting Register	DMINT	8	8	2 ICLK			
0008 20D4h	DMAC3	DMA Address Mode Register	DMAMD	16	16	2 ICLK			
0008 20DCh	DMAC3	DMA Transfer Enable Register	DMCNT	8	8	2 ICLK			
0008 20DDh	DMAC3	DMA Software Start Register	DMREQ	8	8	2 ICLK			
0008 20DEh	DMAC3	DMA Status Register	DMSTS	8	8	2 ICLK			
0008 20DFh	DMAC3	DMA Activation Source Flag Control Register	DMCSL	8	8	2 ICLK			
0008 2200h	DMAC	DMA Module Activation Register	DMAST	8	8	2 ICLK			
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK		DTCa	
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK			
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK			
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK			
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK			
0008 3002h	BSC	CS0 Mode Register	CS0MOD	16	16	1 to 2BCLK		Buses	
0008 3004h	BSC	CS0 Wait Control Register 1	CS0WCR1	32	32	1 to 2BCLK			
0008 3008h	BSC	CS0 Wait Control Register 2	CS0WCR2	32	32	1 to 2BCLK			
0008 3012h	BSC	CS1 Mode Register	CS1MOD	16	16	1 to 2BCLK			
0008 3014h	BSC	CS1 Wait Control Register 1	CS1WCR1	32	32	1 to 2BCLK			
0008 3018h	BSC	CS1 Wait Control Register 2	CS1WCR2	32	32	1 to 2BCLK			

Table 4.1 List of I/O Registers (Address Order) (5 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 7074h	ICU	Interrupt Request Register 116	IR116	8	8	2 ICLK		ICUb	
0008 7075h	ICU	Interrupt Request Register 117	IR117	8	8	2 ICLK			
0008 7076h	ICU	Interrupt Request Register 118	IR118	8	8	2 ICLK			
0008 7077h	ICU	Interrupt Request Register 119	IR119	8	8	2 ICLK			
0008 7078h	ICU	Interrupt Request Register 120	IR120	8	8	2 ICLK			
0008 7079h	ICU	Interrupt Request Register 121	IR121	8	8	2 ICLK			
0008 707Ah	ICU	Interrupt Request Register 122	IR122	8	8	2 ICLK			
0008 707Bh	ICU	Interrupt Request Register 123	IR123	8	8	2 ICLK			
0008 707Ch	ICU	Interrupt Request Register 124	IR124	8	8	2 ICLK			
0008 707Dh	ICU	Interrupt Request Register 125	IR125	8	8	2 ICLK			
0008 707Eh	ICU	Interrupt Request Register 126	IR126	8	8	2 ICLK			
0008 707Fh	ICU	Interrupt Request Register 127	IR127	8	8	2 ICLK			
0008 7080h	ICU	Interrupt Request Register 128	IR128	8	8	2 ICLK			
0008 7081h	ICU	Interrupt Request Register 129	IR129	8	8	2 ICLK			
0008 7082h	ICU	Interrupt Request Register 130	IR130	8	8	2 ICLK			
0008 7083h	ICU	Interrupt Request Register 131	IR131	8	8	2 ICLK			
0008 7084h	ICU	Interrupt Request Register 132	IR132	8	8	2 ICLK			
0008 7085h	ICU	Interrupt Request Register 133	IR133	8	8	2 ICLK			
0008 7086h	ICU	Interrupt Request Register 134	IR134	8	8	2 ICLK			
0008 7087h	ICU	Interrupt Request Register 135	IR135	8	8	2 ICLK			
0008 7088h	ICU	Interrupt Request Register 136	IR136	8	8	2 ICLK			
0008 7089h	ICU	Interrupt Request Register 137	IR137	8	8	2 ICLK			
0008 708Ah	ICU	Interrupt Request Register 138	IR138	8	8	2 ICLK			
0008 708Bh	ICU	Interrupt Request Register 139	IR139	8	8	2 ICLK			
0008 708Ch	ICU	Interrupt Request Register 140	IR140	8	8	2 ICLK			
0008 708Dh	ICU	Interrupt Request Register 141	IR141	8	8	2 ICLK			
0008 708Eh	ICU	Interrupt Request Register 142	IR142	8	8	2 ICLK			
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK			
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK			
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK			
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK			
0008 7093h	ICU	Interrupt Request Register 147	IR147	8	8	2 ICLK			
0008 7094h	ICU	Interrupt Request Register 148	IR148	8	8	2 ICLK			
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK			
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK			
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK			
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK			
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK			
0008 709Ah	ICU	Interrupt Request Register 154	IR154	8	8	2 ICLK			
0008 709Bh	ICU	Interrupt Request Register 155	IR155	8	8	2 ICLK			
0008 709Ch	ICU	Interrupt Request Register 156	IR156	8	8	2 ICLK			
0008 709Dh	ICU	Interrupt Request Register 157	IR157	8	8	2 ICLK			
0008 709Eh	ICU	Interrupt Request Register 158	IR158	8	8	2 ICLK			
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK			
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK			
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK			
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK			
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK			
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK			
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK			
0008 70A6h	ICU	Interrupt Request Register 166	IR166	8	8	2 ICLK			

Table 4.1 List of I/O Registers (Address Order) (16 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 830Ah	RIIC0	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK	RIIC	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 830Ch	RIIC0	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Dh	RIIC0	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 830Eh	RIIC0	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 830Fh	RIIC0	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8310h	RIIC0	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8311h	RIIC0	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8312h	RIIC0	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8313h	RIIC0	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8320h	RIIC1	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8321h	RIIC1	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8322h	RIIC1	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8323h	RIIC1	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8324h	RIIC1	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8325h	RIIC1	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8326h	RIIC1	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8327h	RIIC1	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8328h	RIIC1	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8329h	RIIC1	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Ah	RIIC1	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 832Bh	RIIC1	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 832Ch	RIIC1	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Dh	RIIC1	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 832Eh	RIIC1	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		
0008 832Fh	RIIC1	Slave Address Register U2	SARU2	8	8	2 to 3PCLKB	2 ICLK		
0008 8330h	RIIC1	I2C Bus Bit Rate Low-Level Register	ICBRL	8	8	2 to 3PCLKB	2 ICLK		
0008 8331h	RIIC1	I2C Bus Bit Rate High-Level Register	ICBRH	8	8	2 to 3PCLKB	2 ICLK		
0008 8332h	RIIC1	I2C Bus Transmit Data Register	ICDRT	8	8	2 to 3PCLKB	2 ICLK		
0008 8333h	RIIC1	I2C Bus Receive Data Register	ICDRR	8	8	2 to 3PCLKB	2 ICLK		
0008 8360h	RIIC3	I2C Bus Control Register 1	ICCR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8361h	RIIC3	I2C Bus Control Register 2	ICCR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8362h	RIIC3	I2C Bus Mode Register 1	ICMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8363h	RIIC3	I2C Bus Mode Register 2	ICMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 8364h	RIIC3	I2C Bus Mode Register 3	ICMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 8365h	RIIC3	I2C Bus Function Enable Register	ICFER	8	8	2 to 3PCLKB	2 ICLK		
0008 8366h	RIIC3	I2C Bus Status Enable Register	ICSER	8	8	2 to 3PCLKB	2 ICLK		
0008 8367h	RIIC3	I2C Bus Interrupt Enable Register	ICIER	8	8	2 to 3PCLKB	2 ICLK		
0008 8368h	RIIC3	I2C Bus Status Register 1	ICSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 8369h	RIIC3	I2C Bus Status Register 2	ICSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Slave Address Register L0	SARL0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Ah	RIIC3	Timeout Internal Counter L	TMOCNTL	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Slave Address Register U0	SARU0	8	8	2 to 3PCLKB	2 ICLK		
0008 836Bh	RIIC3	Timeout Internal Counter U	TMOCNTU	8	8*2	2 to 3PCLKB	2 ICLK		
0008 836Ch	RIIC3	Slave Address Register L1	SARL1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Dh	RIIC3	Slave Address Register U1	SARU1	8	8	2 to 3PCLKB	2 ICLK		
0008 836Eh	RIIC3	Slave Address Register L2	SARL2	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (24 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 A163h	SCI11	Transmit Data Register	TDR	8	8	2 to 3PCLKB	2 ICLK	SCIe, SCIf	
0008 A164h	SCI11	Serial Status Register	SSR	8	8	2 to 3PCLKB	2 ICLK		
0008 A165h	SCI11	Receive Data Register	RDR	8	8	2 to 3PCLKB	2 ICLK		
0008 A166h	SCI11	Smart Card Mode Register	SCMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A167h	SCI11	Serial Extended Mode Register	SEMR	8	8	2 to 3PCLKB	2 ICLK		
0008 A168h	SCI11	Noise Filter Setting Register	SNFR	8	8	2 to 3PCLKB	2 ICLK		
0008 A169h	SCI11	I^2C Mode Register 1	SIMR1	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Ah	SCI11	I^2C Mode Register 2	SIMR2	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Bh	SCI11	I^2C Mode Register 3	SIMR3	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Ch	SCI11	I^2C Status Register	SISR	8	8	2 to 3PCLKB	2 ICLK		
0008 A16Dh	SCI11	SPI Mode Register	SPMR	8	8	2 to 3PCLKB	2 ICLK		
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 to 3PCLKB	2 ICLK	CAC	
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 to 3PCLKB	2 ICLK		
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 to 3PCLKB	2 ICLK		
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 to 3PCLKB	2 ICLK		
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 to 3PCLKB	2 ICLK		
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 to 3PCLKB	2 ICLK		
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 to 3PCLKB	2 ICLK	DOC	
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 to 3PCLKB	2 ICLK		
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 to 3PCLKB	2 ICLK		
0008 B100h	ELC	Event Link Control Register	ELCR	8	8	2 to 3PCLKB	2 ICLK	ELC	
0008 B102h	ELC	Event Link Setting Register 1	ELSR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B103h	ELC	Event Link Setting Register 2	ELSR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B104h	ELC	Event Link Setting Register 3	ELSR3	8	8	2 to 3PCLKB	2 ICLK		
0008 B105h	ELC	Event Link Setting Register 4	ELSR4	8	8	2 to 3PCLKB	2 ICLK		
0008 B108h	ELC	Event Link Setting Register 7	ELSR7	8	8	2 to 3PCLKB	2 ICLK		
0008 B10Bh	ELC	Event Link Setting Register 10	ELSR10	8	8	2 to 3PCLKB	2 ICLK		
0008 B10Dh	ELC	Event Link Setting Register 12	ELSR12	8	8	2 to 3PCLKB	2 ICLK		
0008 B110h	ELC	Event Link Setting Register 15	ELSR15	8	8	2 to 3PCLKB	2 ICLK		
0008 B111h	ELC	Event Link Setting Register 16	ELSR16	8	8	2 to 3PCLKB	2 ICLK		
0008 B113h	ELC	Event Link Setting Register 18	ELSR18	8	8	2 to 3PCLKB	2 ICLK		
0008 B114h	ELC	Event Link Setting Register 19	ELSR19	8	8	2 to 3PCLKB	2 ICLK		
0008 B115h	ELC	Event Link Setting Register 20	ELSR20	8	8	2 to 3PCLKB	2 ICLK		
0008 B116h	ELC	Event Link Setting Register 21	ELSR21	8	8	2 to 3PCLKB	2 ICLK		
0008 B117h	ELC	Event Link Setting Register 22	ELSR22	8	8	2 to 3PCLKB	2 ICLK		
0008 B118h	ELC	Event Link Setting Register 23	ELSR23	8	8	2 to 3PCLKB	2 ICLK		
0008 B119h	ELC	Event Link Setting Register 24	ELSR24	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Ah	ELC	Event Link Setting Register 25	ELSR25	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Bh	ELC	Event Link Setting Register 26	ELSR26	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Ch	ELC	Event Link Setting Register 27	ELSR27	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Dh	ELC	Event Link Setting Register 28	ELSR28	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Eh	ELC	Event Link Setting Register 29	ELSR29	8	8	2 to 3PCLKB	2 ICLK		
0008 B11Fh	ELC	Event Link Option Setting Register A	ELOPA	8	8	2 to 3PCLKB	2 ICLK		
0008 B120h	ELC	Event Link Option Setting Register B	ELOPB	8	8	2 to 3PCLKB	2 ICLK		
0008 B121h	ELC	Event Link Option Setting Register C	ELOPC	8	8	2 to 3PCLKB	2 ICLK		
0008 B122h	ELC	Event Link Option Setting Register D	ELOPD	8	8	2 to 3PCLKB	2 ICLK		
0008 B123h	ELC	Port Group Setting Register 1	PGR1	8	8	2 to 3PCLKB	2 ICLK		
0008 B124h	ELC	Port Group Setting Register 2	PGR2	8	8	2 to 3PCLKB	2 ICLK		
0008 B125h	ELC	Port Group Control Register 1	PGC1	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (27 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C062h	PORT2	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK	I/O Ports	
0008 C063h	PORT3	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C065h	PORT5	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C066h	PORT6	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C067h	PORT7	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C068h	PORT8	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C069h	PORT9	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ah	PORTA	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Bh	PORTB	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Ch	PORTC	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Dh	PORTD	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Eh	PORTE	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C06Fh	PORTF	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C071h	PORTH	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C072h	PORTJ	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C073h	PORTK	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C074h	PORTL	Port Mode Register	PMR	8	8	2 to 3PCLKB	2 ICLK		
0008 C080h	PORT0	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C082h	PORT1	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C083h	PORT1	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C084h	PORT2	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C085h	PORT2	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C086h	PORT3	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C087h	PORT3	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ah	PORT5	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Bh	PORT5	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Ch	PORT6	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Eh	PORT7	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C08Fh	PORT7	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C090h	PORT8	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C092h	PORT9	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C094h	PORTA	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C095h	PORTA	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C096h	PORTB	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C097h	PORTB	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C098h	PORTC	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C099h	PORTC	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A6h	PORTK	Open Drain Control Register 0	ODR0	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0A7h	PORTK	Open Drain Control Register 1	ODR1	8	8, 16	2 to 3PCLKB	2 ICLK		
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (29 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C157h	MPC	P27 Pin Function Control Register	P27PFS	8	8	2 to 3PCLKB	2 ICLK	MPC	
0008 C158h	MPC	P30 Pin Function Control Registers	P30PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C159h	MPC	P31 Pin Function Control Registers	P31PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ah	MPC	P32 Pin Function Control Registers	P32PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Bh	MPC	P33 Pin Function Control Registers	P33PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C15Ch	MPC	P34 Pin Function Control Registers	P34PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C160h	MPC	P40 Pin Function Control Registers	P40PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C161h	MPC	P41 Pin Function Control Registers	P41PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C162h	MPC	P42 Pin Function Control Registers	P42PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C163h	MPC	P43 Pin Function Control Registers	P43PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C164h	MPC	P44 Pin Function Control Registers	P44PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C165h	MPC	P45 Pin Function Control Registers	P45PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C166h	MPC	P46 Pin Function Control Registers	P46PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C167h	MPC	P47 Pin Function Control Registers	P47PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C168h	MPC	P50 Pin Function Control Registers	P50PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C169h	MPC	P51 Pin Function Control Registers	P51PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ah	MPC	P52 Pin Function Control Registers	P52PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Ch	MPC	P54 Pin Function Control Registers	P54PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Dh	MPC	P55 Pin Function Control Registers	P55PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C16Eh	MPC	P56 Pin Function Control Registers	P56PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C170h	MPC	P60 Pin Function Control Registers	P60PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C171h	MPC	P61 Pin Function Control Registers	P61PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C178h	MPC	P70 Pin Function Control Registers	P70PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Bh	MPC	P73 Pin Function Control Registers	P73PFS	8	8	2 to 3PCLKB	2 ICLK		Not available in 3-V packages.
0008 C17Ch	MPC	P74 Pin Function Control Registers	P74PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Dh	MPC	P75 Pin Function Control Registers	P75PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Eh	MPC	P76 Pin Function Control Registers	P76PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C17Fh	MPC	P77 Pin Function Control Registers	P77PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C180h	MPC	P80 Pin Function Control Registers	P80PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C181h	MPC	P81 Pin Function Control Registers	P81PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C182h	MPC	P82 Pin Function Control Registers	P82PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C183h	MPC	P83 Pin Function Control Registers	P83PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C186h	MPC	P86 Pin Function Control Registers	P86PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C187h	MPC	P87 Pin Function Control Registers	P87PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C188h	MPC	P90 Pin Function Control Registers	P90PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C189h	MPC	P91 Pin Function Control Registers	P91PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Ah	MPC	P92 Pin Function Control Registers	P92PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C18Bh	MPC	P93 Pin Function Control Registers	P93PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C190h	MPC	PA0 Pin Function Control Registers	PA0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C191h	MPC	PA1 Pin Function Control Registers	PA1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C192h	MPC	PA2 Pin Function Control Registers	PA2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C193h	MPC	PA3 Pin Function Control Registers	PA3PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C194h	MPC	PA4 Pin Function Control Registers	PA4PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C195h	MPC	PA5 Pin Function Control Registers	PA5PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C196h	MPC	PA6 Pin Function Control Registers	PA6PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C197h	MPC	PA7 Pin Function Control Registers	PA7PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C198h	MPC	PB0 Pin Function Control Registers	PB0PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C199h	MPC	PB1 Pin Function Control Registers	PB1PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Ah	MPC	PB2 Pin Function Control Registers	PB2PFS	8	8	2 to 3PCLKB	2 ICLK		
0008 C19Bh	MPC	PB3 Pin Function Control Registers	PB3PFS	8	8	2 to 3PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (31 / 34)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles		Related Function	Remarks
						ICLK ≥ PCLK	ICLK < PCLK		
0008 C293h	SYSTEM	Main Clock Oscillator Forced Oscillation Control Register	MOFCR	8	8	4 to 5PCLKB	2 to 3 ICLK	Clock Generation Circuit	
0008 C296h	FLASH	Flash Write Erase Protection Register	FWEPROR	8	8	4 to 5PCLKB	2 to 3 ICLK	Flash Memory	
0008 C297h	SYSTEM	Voltage Monitoring Circuit Control Register	LVCMPCR	8	8	4 to 5PCLKB	2 to 3 ICLK	LVDA	
0008 C298h	SYSTEM	Voltage Detection Level Select Register	LVDLVLR	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Ah	SYSTEM	Voltage Monitoring 1 Circuit Control Register 0	LVD1CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C29Bh	SYSTEM	Voltage Monitoring 2 Circuit Control Register 0	LVD2CR0	8	8	4 to 5PCLKB	2 to 3 ICLK		
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep Standby Backup Register 0 to 31	DPSBKR0 to 31	8	8	4 to 5PCLKB	2 to 3 ICLK	Low Power Consumption	
000A 0A00h	CEC	CEC Local Address Setting Register	CADR	16	16	1 to 2PCLK	1 ICLK	CEC	Not available in 5-V packages.
000A 0A02h	CEC	CEC Control Register 1	CECCTL1	8	8	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A04h	CEC	CEC Transmission Start Bit Width Setting Register	STATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A06h	CEC	CEC Transmission Start Bit Low Width Setting Register	STATL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A08h	CEC	CEC Transmission Logical 0 Low Width Setting Register	LGC0L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ah	CEC	CEC Transmission Logical 1 Low Width Setting Register	LGC1L	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Ch	CEC	CEC Transmission Data Bit Width Setting Register	DATB	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A0Eh	CEC	CEC Reception Data Sampling Time Setting Register	NOMT	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A10h	CEC	CEC Reception Start Bit Minimum Low Width Setting Register	STATLL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A12h	CEC	CEC Reception Start Bit Maximum Low Width Setting Register	STATLH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A14h	CEC	CEC Reception Start Bit Minimum Bit Width Setting Register	STATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A16h	CEC	CEC Reception Start Bit Maximum Bit Width Setting Register	STATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A18h	CEC	CEC Reception Logical 0 Minimum Low Width Setting Register	LGC0LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ah	CEC	CEC Reception Logical 0 Maximum Low Width Setting Register	LGC0LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Ch	CEC	CEC Reception Logical 1 Minimum Low Width Setting Register	LGC1LL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A1Eh	CEC	CEC Reception Logical 1 Maximum Low Width Setting Register	LGC1LH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A20h	CEC	CEC Reception Data Bit Minimum Bit Width Setting Register	DATBL	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A22h	CEC	CEC Reception Data Bit Maximum Bit Width Setting Register	DATBH	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.
000A 0A24h	CEC	CEC Data Bit Reference Width Setting Register	NOMP	16	16	1 to 2PCLK	1 ICLK		Not available in 5-V packages.

Table 5.6 DC Characteristics (5)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	Low-speed operating mode 1	Normal operating mode	No peripheral operation*2	ICLK = 1 MHz	I_{CC}	4	—	mA	
			All peripheral operation: Normal*3	ICLK = 1 MHz		4.2	—		
			All peripheral operation: Max.*3	ICLK = 1 MHz		—	15		
		Sleep mode	No peripheral operation	ICLK = 1 MHz		3.8	—		
			All peripheral operation: Normal	ICLK = 1 MHz		4.0	—		
		All-module clock stop mode				3.7	—		
	Low-speed operating mode 2	Normal operating mode	No peripheral operation*4	ICLK = 125 kHz		0.4	—		
			All peripheral operation: Normal*5	ICLK = 125 kHz		0.5	—		
			All peripheral operation: Max.*5	ICLK = 125 kHz		—	8*6		
		Sleep mode	No peripheral operation	ICLK = 125 kHz		0.3	—		
			All peripheral operation: Normal	ICLK = 125 kHz		0.4	—		
		All-module clock stop mode				0.28	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main clock.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main clock.
Note 4. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is LOCO.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is LOCO.
Note 6. Value when the main clock continues oscillating at 13.5 MHz.

Table 5.7 DC Characteristics (6)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, T_a = –40 to +85°C

Item				Symbol	Typ.	Max.	Unit	Test Conditions
Supply power*1	Software standby mode			I_{CC}	40	1000	µA	
	Deep software standby mode	RAM power supplied			22	200		
		RAM power not supplied	Power-on reset circuit low power consumption function disabled		21	60		
			Power-on reset circuit low power consumption function enabled		6.2	28		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 1. The values in parentheses indicate when the MONFCR register is set to a value other than A5h (noise filter enabled) while CECMCLK is selected as the CEC operating clock and RCRMCLK is selected as the RCR operating clock.
Note 2. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 3. When using a main clock, request the oscillator manufacturer to evaluate the oscillator. For the oscillation stabilization time, refer to the evaluation results obtained from the oscillator manufacturer.
Note 4. The number of cycles n selected by the value of the MOSCWTCR.MSTS[4:0] bits determines the main-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{MAINOSCWT} = t_{MAINOSC} + \frac{n + 16384}{f_{MAIN}}$$

Note 5. The number of cycles n selected by the value of the PLLWTCR.PSTS[4:0] bits determines the PLL-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{PLLWT1} = t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

$$t_{PLLWT2} = t_{PLL2} + \frac{n + 131072}{f_{PLL}} = t_{MAINOSC} + t_{PLL1} + \frac{n + 131072}{f_{PLL}}$$

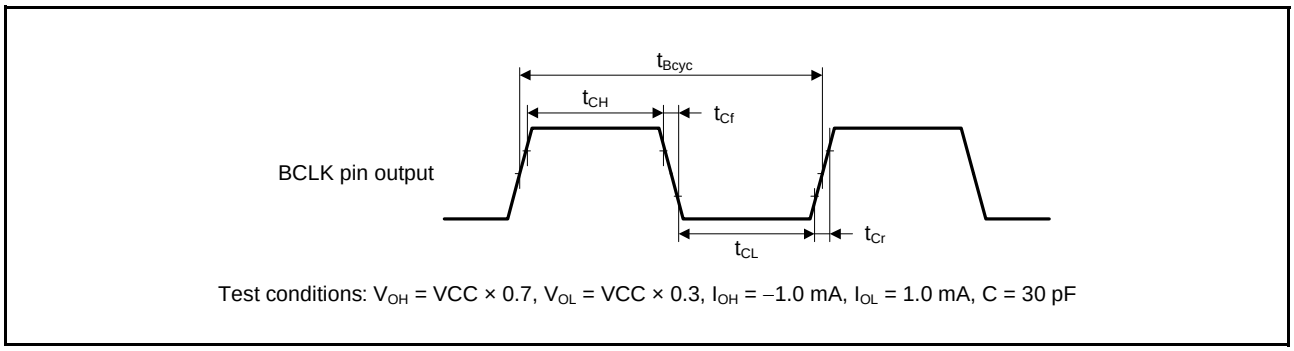


Figure 5.1 BCLK Pin Output Timing

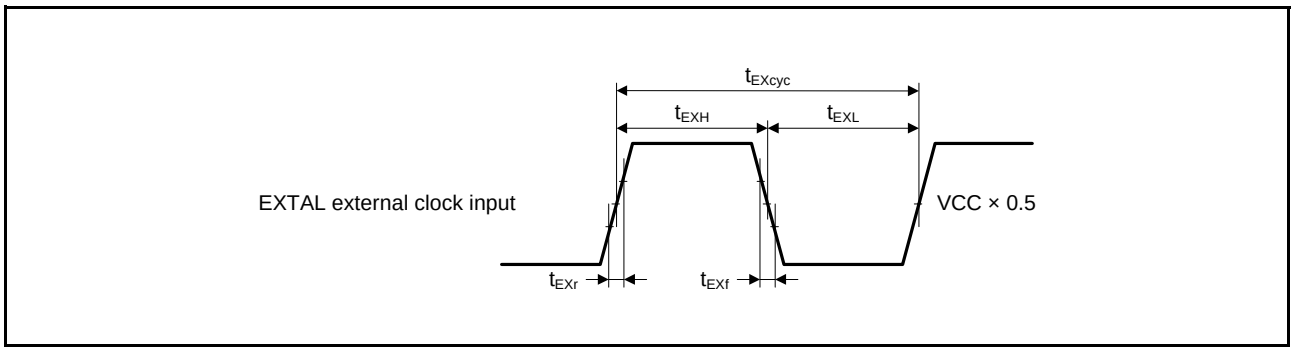


Figure 5.2 EXTAL External Clock Input Timing

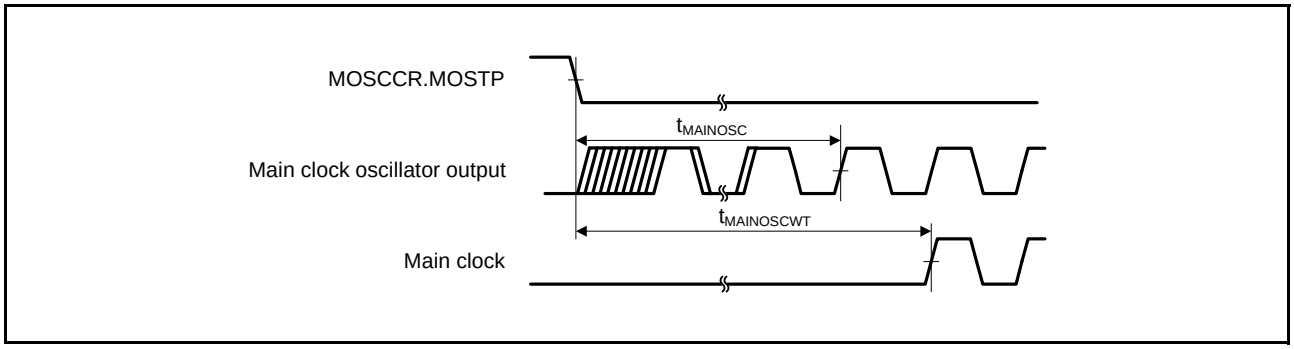


Figure 5.3 Main Clock Oscillation Start Timing

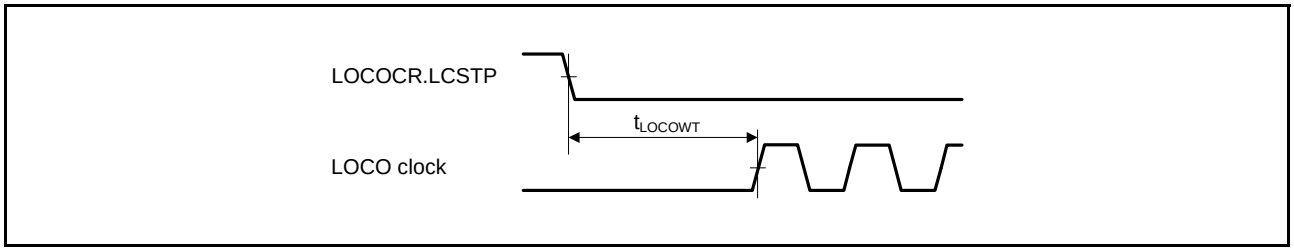


Figure 5.4 LOCO Clock Oscillation Start Timing

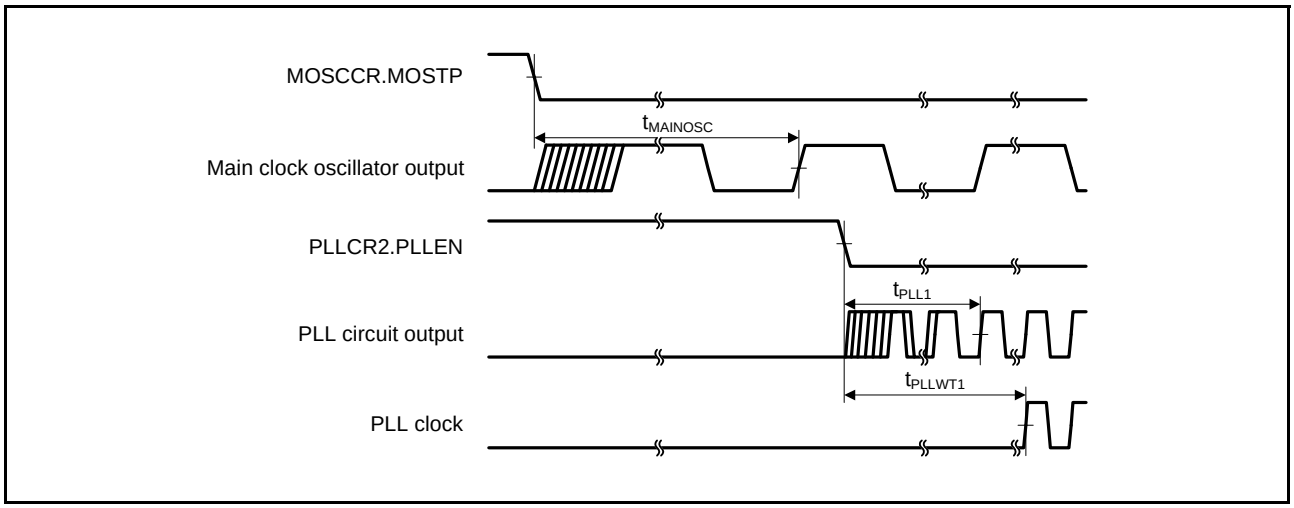


Figure 5.5 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

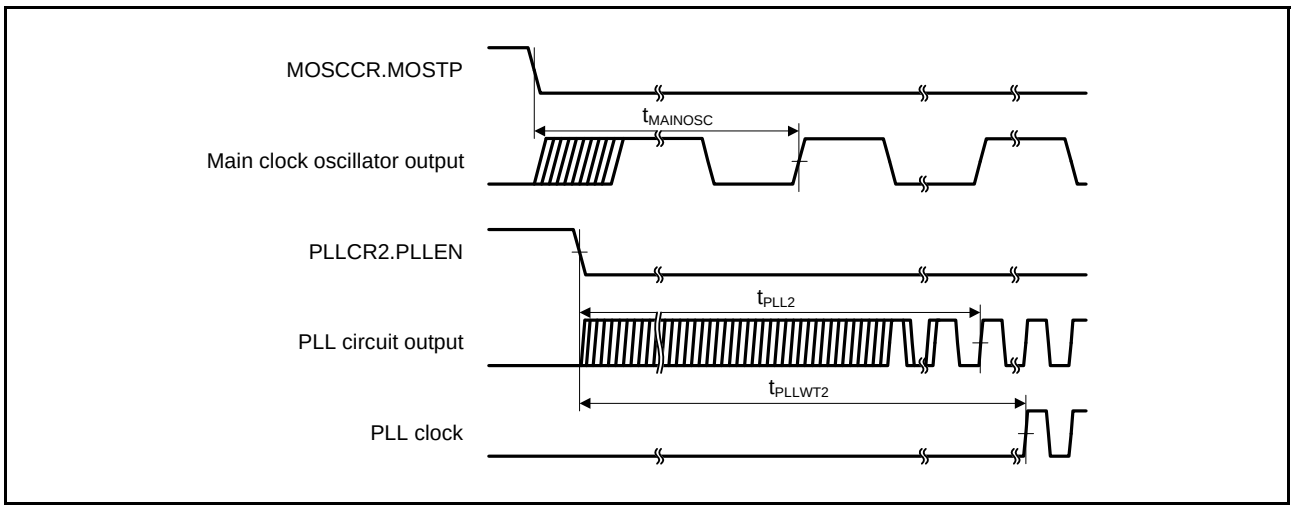
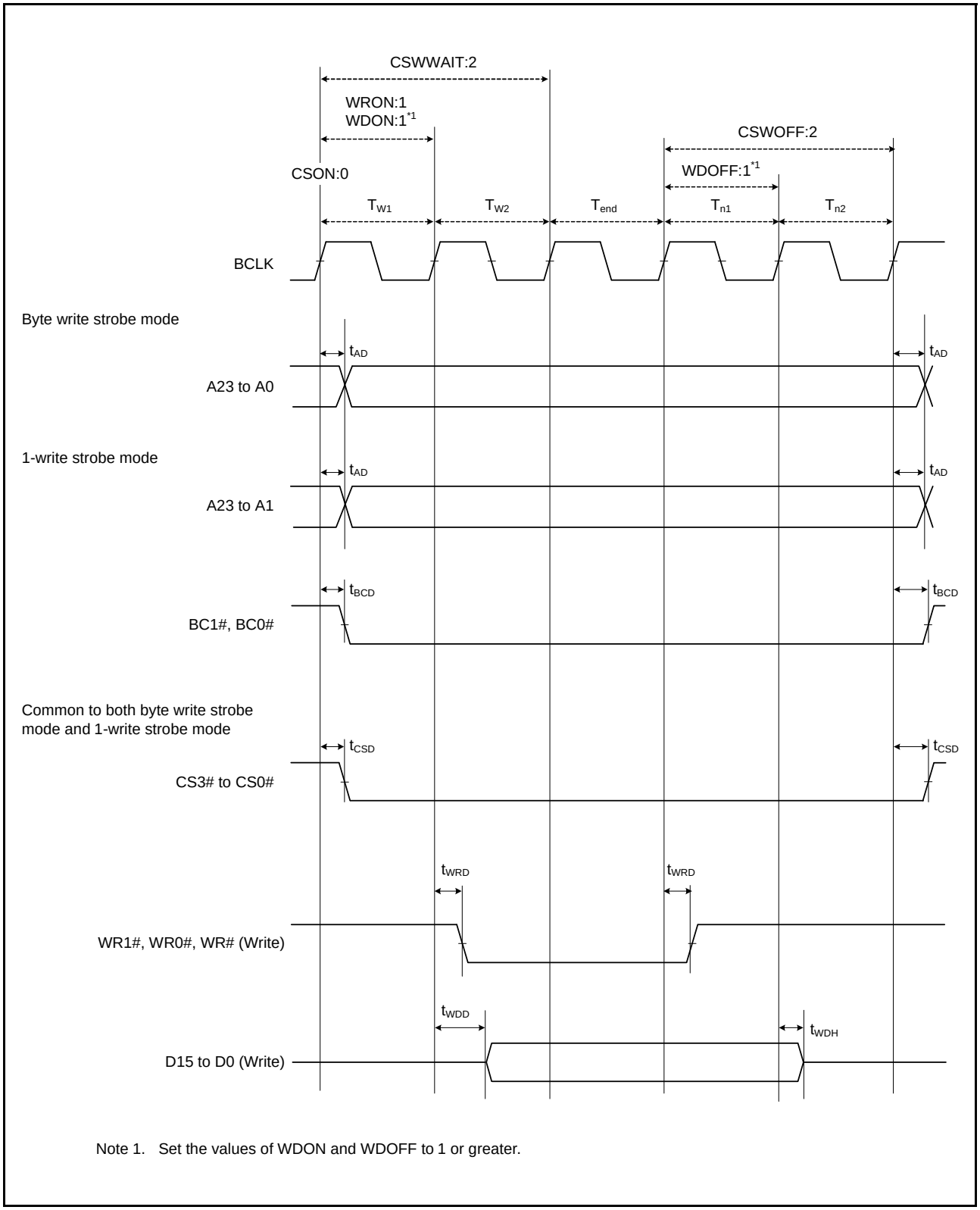


Figure 5.6 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.14 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

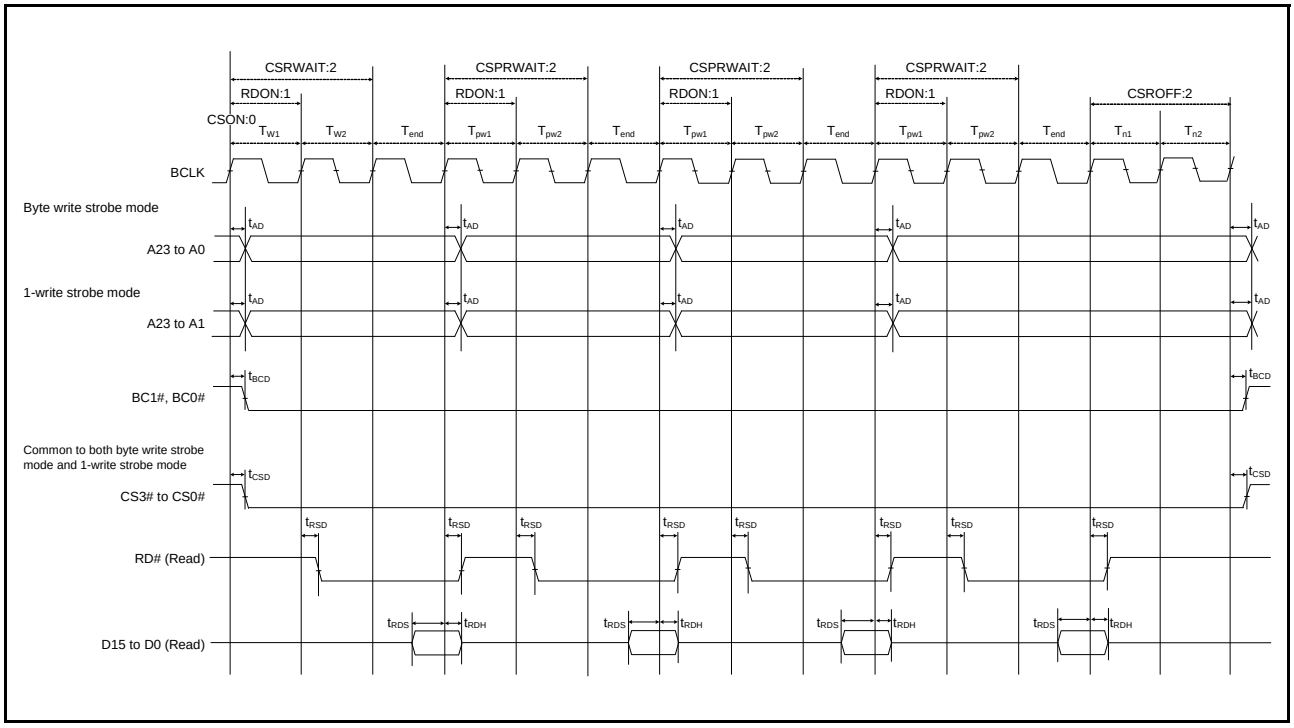
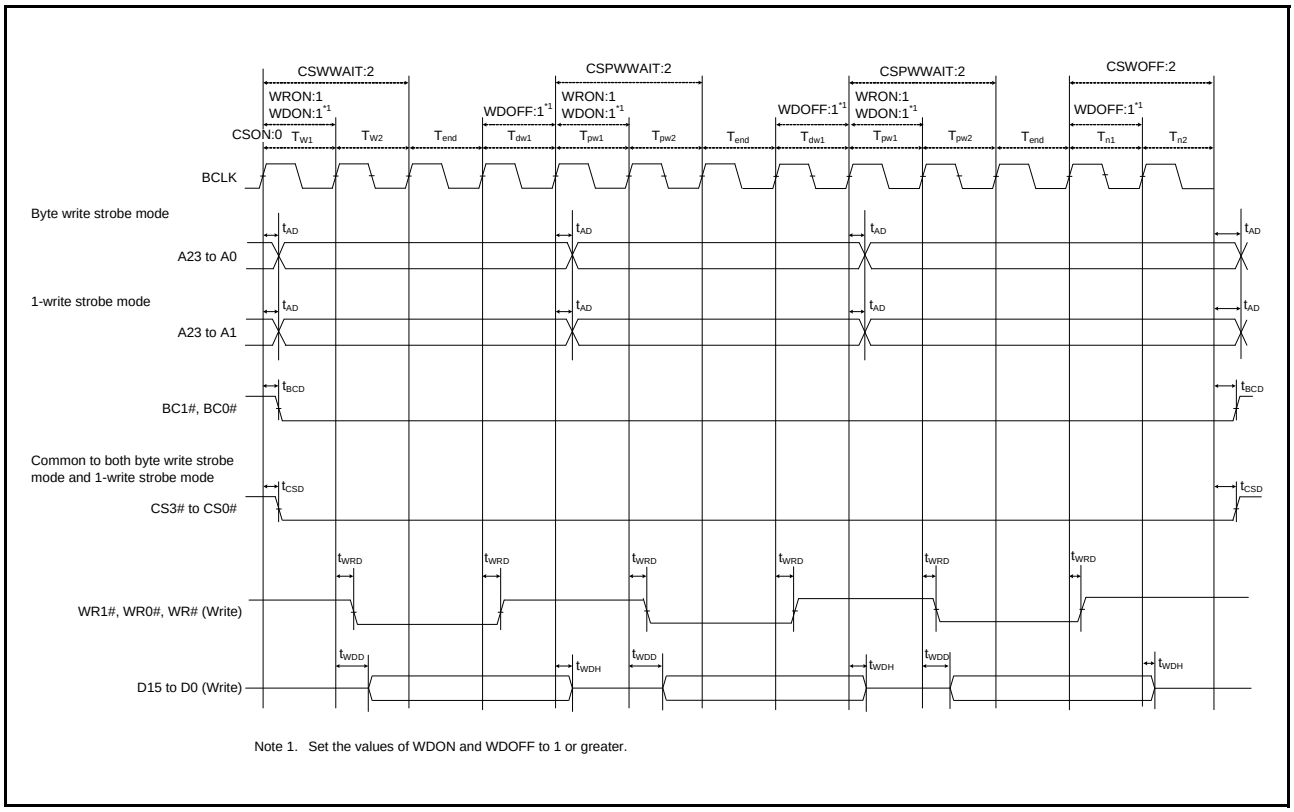


Figure 5.15 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)



Note 1. Set the values of WDON and WDOFF to 1 or greater.

Figure 5.16 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

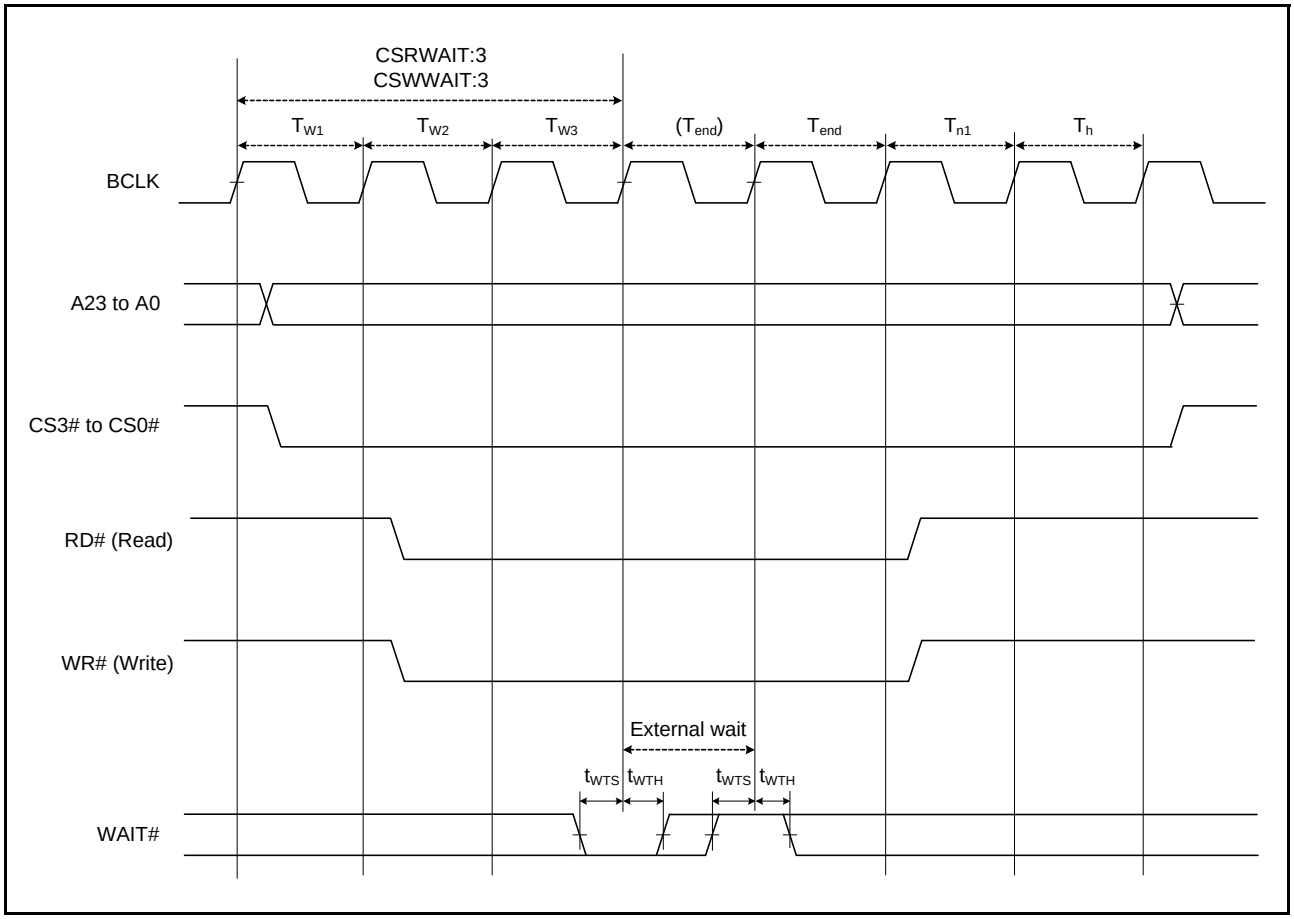


Figure 5.17 External Bus Timing/External Wait Control

Table 5.23 Bus Timing (Multiplexed Bus)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
fBCLK ≤ 54 MHz (BCLK pin output frequency ≤ 27 MHz), VOH = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = –1.0 mA,
I_{OL} = 1.0 mA, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	30	ns	Figure 5.18, Figure 5.19
Byte control delay time	t_{BCD}	—	30	ns	
CS# delay time	t_{CSD}	—	30	ns	
RD# delay time	t_{RSD}	—	30	ns	
ALE delay time	t_{ALED}	—	30	ns	
Read data setup time	t_{RDS}	20	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	30	ns	
Write data delay time	t_{WDD}	—	30	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	20	—	ns	Figure 5.17
WAIT# hold time	t_{WTH}	0	—	ns	

5.3.6 Timing of On-Chip Peripheral Modules

Table 5.24 Timing of On-Chip Peripheral Modules (1)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
T_a = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.20
MTU/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.21
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.22
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.23
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.24
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.25
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.26
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.27
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$*2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$*2		5 t_{cac} + 6.5 t_{Pcyc}	—	ns	

Note 1. t_{Pcyc}: PCLKB cycle
Note 2. t_{cac}: CAC count clock source cycle

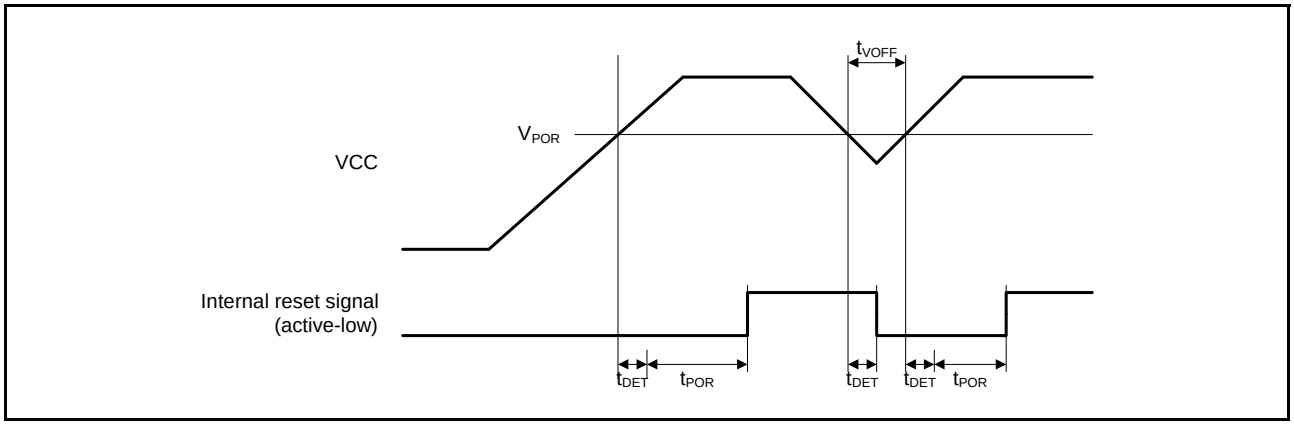


Figure 5.38 Power-on Reset Timing

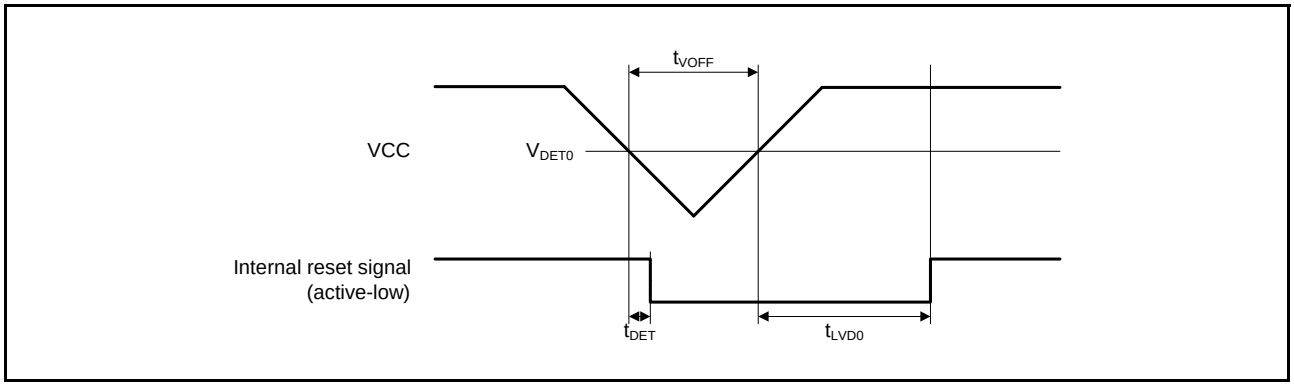
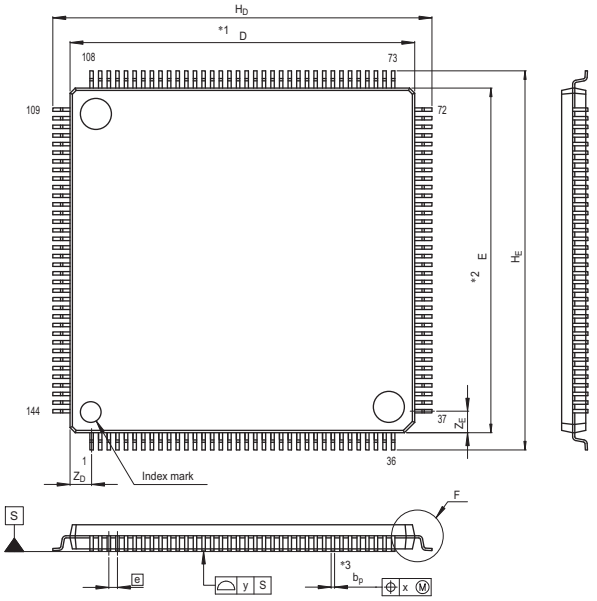


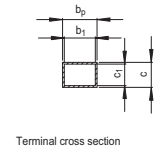
Figure 5.39 Voltage Detection Circuit Timing (V_{DET0})

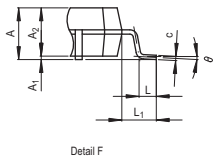
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g







NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure A 144-Pin LQFP (PLQP0144KA-A)