# Renesas Electronics America Inc - R5F5634DYDFB#30 Datasheet

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 54MHz |
| Connectivity | I²C, SCI, SPI |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 1.5MB (1.5M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 128K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LFQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5634dydfb-30 |

**Table 1.1 Outline of Specifications (2 / 4)**

| Classification | Module/Function | Description |
|---|---|---|
| External bus extension | | • The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings.<br>Capacity of each area: 16 Mbytes (CS0 to CS3)<br>A chip-select signal (CS0# to CS3#) can be output for each area.<br>Each area is specifiable as an 8-bit or 16-bit bus space<br>The data arrangement in each area is selectable as little or big endian (only for data).<br>Bus format: Separate bus, multiplex bus<br>• Wait control<br>• Write buffer facility |
| DMA | DMA controller (DMACA) | • 4 channels<br>• Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | Data transfer controller (DTCa) | • Three transfer modes: Normal transfer, repeat transfer, and block transfer<br>• Activation sources: Interrupts<br>• Chain transfer function |
| I/O ports | General I/O ports | 144-pin<br>• I/O: 114<br>• Input: 9 (P40 to P47, P35)<br>• Pull-up resistors: 111<br>• Open-drain outputs: 114<br>• 5-V tolerance: Not supported |
| Event link controller (ELC) | | • Event signals of 56 types can be directly connected to the module<br>• Operations of timer modules are selectable at event input<br>• Capable of event link operation for ports B and E |
| Multi-function pin controller (MPC) | | • Capable of selecting input/output function from multiple pins |
| Timers | 16-bit timer pulse unit (TPUa) | • (16 bits × 6 channels) × 1 unit<br>• Maximum of 16 pulse-input/output possible<br>• Select from among seven or eight counter-input clock signals for each channel<br>• Supports the input capture/output compare function<br>• Output of PWM waveforms in up to 15 phases in PWM mode<br>• Support for buffered operation, phase-counting mode (two-phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel.<br>• Capable of generating conversion start triggers for the A/D converters<br>• Signals from the input capture pins are input via a digital filter |
| | Multi-function timer pulse unit 2 (MTU2a) | • (16 bits × 6 channels) × 1 unit<br>• Up to 16 pulse-input/output lines and three pulse-input lines are available with six 16-bit timer channels<br>• Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available.<br>• Input capture function<br>• 21 output compare/input capture registers<br>• Pulse output mode<br>• Complementary PWM output mode<br>• Reset synchronous PWM mode<br>• Phase-counting mode<br>• Generation of triggers for A/D converter conversion |
| | Port output enable 2 (POE2a) | Controls the high-impedance state of the MTU's waveform output pins |
| | Programmable pulse generator (PPG) | • (4 bits × 4 groups) × 1 unit<br>• Pulse output with the MTU output as a trigger<br>• Maximum of 16 pulse-output possible |
| | 8-bit timer (TMR) | • (8 bits × 2 channels) × 2 units<br>• Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal<br>• Capable of output of pulse trains with desired duty cycles or of PWM signals<br>• The 2 channels of each unit can be cascaded to create a 16-bit timer<br>• Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12<br>• Capable of generating a receive clock for the RCR |
| | Compare match timer (CMT) | • (16 bits × 2 channels) × 2 units<br>• Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512) |
| | Watchdog timer (WDTA) | • 14 bits × 1 channel<br>• Select from among six counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192) |

**Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (1 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TPU, TMR, POE, PPG, CAC) | Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR) | Interrupt | AD, DA |
|---|---|---|---|---|---|---|---|
| 1 | AVSS0 | | | | | | |
| 2 | | P05 | | | | | DA1 |
| 3 | VREFH | | | | | | |
| 4 | | P03 | | | | IRQ11 | DA0 |
| 5 | VREFL | | | | | | |
| 6 | | P02 | | TMCI1 | SCK6 | IRQ10 | |
| 7 | | P01 | | TMCI0 | RXD6/SMISO6/SSCL6/PMC1 | IRQ9 | |
| 8 | | P00 | | TMRI0 | TXD6/SMOSI6/SSDA6/PMC0 | IRQ8 | |
| 9 | | PF5 | | | | IRQ4 | |
| 10 | EMLE | | | | | | |
| 11 | | PJ5 | | | | | |
| 12 | VSS | | | | | | |
| 13 | | PJ3 | | MTIOC3C | CTS0#/RTS0#/SS0#/CTS6#/ RTS6#/SS6# | | |
| 14 | VCL | | | | | | |
| 15 | | PJ1 | | MTIOC3A | | | |
| 16 | MD/FINED | | | | | | |
| 17 | | PJ2 | | | | | |
| 18 | | PJ4 | | | | | |
| 19 | RES# | | | | | | |
| 20 | XTAL | | | | | | |
| 21 | VSS | | | | | | |
| 22 | EXTAL | | | | | | |
| 23 | VCC | | | | | | |
| 24 | | P35 | | | | NMI | |
| 25 | TRST# | P34 | | MTIOC0A/TMCI3/POE2#/ PO12 | SCK0/SCK6 | IRQ4 | |
| 26 | | P33 | | MTIOC0D/TIOCD0/TMRI3/ POE3#/PO11 | RXD0/SMISO0/SSCL0/RXD6/ SMISO6/SSCL6 | IRQ3_DS | |
| 27 | | P32 | | MTIOC0C/TIOCC0/TMO3/ PO10 | TXD0/SMOSI0/SSDA0/TXD6/ SMOSI6/SSDA6 | IRQ2_DS | |
| 28 | TMS | P31 | | MTIOC4D/TMCI2/PO9 | CTS1#/RTS1#/SS1#/SSLB0 | IRQ1_DS | |
| 29 | TDI | P30 | | MTIOC4B/TMRI3/POE8#/ PO8 | RXD1/SMISO1/SSCL1/MISOB | IRQ0_DS | |
| 30 | FINEC/TCK | P27 | CS3# | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB | | |
| 31 | TDO | P26 | CS2# | MTIOC2A/TMO1/PO6 | TXD1/SMOSI1/SSDA1/CTS3#/ RTS3#/SS3#/MOSIB | | |
| 32 | | P25 | CS1# | MTIOC4C/MTCLKB/TIOCA4/ PO5 | RXD3/SMISO3/SSCL3 | | ADTRG0# |
| 33 | | P24 | CS0# | MTIOC4A/MTCLKA/TIOCB4/ TMRI1/PO4 | SCK3 | | |
| 34 | | P23 | | MTIOC3D/MTCLKD/ TIOCD3/PO3 | TXD3/SMOSI3/SSDA3/CTS0#/ RTS0#/SS0# | | |
| 35 | | P22 | | MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2 | SCK0 | | |
| 36 | | P21 | | MTIOC1B/TIOCA3/TMCI0/ PO1 | RXD0/SMISO0/SSCL0/SCL1 | IRQ9 | |
| 37 | | P20 | | MTIOC1A/TIOCB3/TMRI0/ PO0 | TXD0/SMOSI0/SSDA0/SDA1 | IRQ8 | |
| 38 | | P17 | | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#/PO15 | SCK1/TXD3/SMOSI3/SSDA3/ MISOA/SDA0_DS | IRQ7 | |

**Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (2 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TPU, TMR, POE, PPG, CAC) | Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR) | Interrupt | AD, DA |
|---|---|---|---|---|---|---|---|
| 39 | | P87 | | TIOCA2 | | | |
| 40 | | P16 | | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/PO14 | TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA/ SCL0_DS | IRQ6 | ADTRG0# |
| 41 | | P86 | | TIOCA0 | | | |
| 42 | | P15 | | MTIOC0B/MTCLKB/TIOCB2/ TCLKB/TMCI2/PO13 | RXD1/SMISO1/SSCL1/SCK3 | IRQ5 | |
| 43 | | P14 | | MTIOC3A/MTCLKA/TIOCB5/ TCLKA/TMRI2/PO15 | CTS1#/RTS1#/SS1# | IRQ4 | |
| 44 | | P13 | | MTIOC0B/TIOCA5/TMO3/ PO13 | TXD2/SMOSI2/SSDA2/SDA0 | IRQ3 | |
| 45 | | P12 | | TMCI1 | RXD2/SMISO2/SSCL2/SCL0 | IRQ2 | |
| 46 | | PH3 | | TMCI0 | | | |
| 47 | | PH2 | | TMRI0 | | IRQ1 | |
| 48 | | PH1 | | TMO0 | | IRQ0 | |
| 49 | | PH0 | | CACREF | | | |
| 50 | | P56 | | MTIOC3C/TIOCA1 | | | |
| 51 | TRDATA3 | P55 | WAIT# | MTIOC4D/TMO3 | | IRQ10 | |
| 52 | TRDATA2 | P54 | ALE | MTIOC4B/TMCI1 | CTS2#/RTS2#/SS2# | | |
| 53 | | P53 | BCLK | | | | |
| 54 | | P52 | RD# | | RXD2/SMISO2/SSCL2/SSLB3 | | |
| 55 | | P51 | WR1#/BC1#/ WAIT# | | SCK2/SSLB2 | | |
| 56 | | P50 | WR0#/WR# | | TXD2/SMOSI2/SSDA2/SSLB1 | | |
| 57 | VSS | | | | | | |
| 58 | TRCLK | P83 | | MTIOC4C | CTS10#/RTS10#/SS10# | | |
| 59 | VCC | | | | | | |
| 60 | | PC7 | A23/CS0# | MTIOC3A/MTCLKB/TMO2/ CACREF | TXD8/SMOSI8/SSDA8/MISOA | | |
| 61 | | PC6 | A22/CS1# | MTIOC3C/MTCLKA/TMCI2 | RXD8/SMISO8/SSCL8/MOSIA | | |
| 62 | | PC5 | A21/CS2#/ WAIT# | MTIOC3B/MTCLKD/TMRI2 | SCK8/RSPCKA | | |
| 63 | TRSYNC# | P82 | | MTIOC4A | TXD10/SMOSI10/SSDA10 | | |
| 64 | TRDATA1 | P81 | | MTIOC3D | RXD10/SMISO10/SSCL10 | | |
| 65 | TRDATA0 | P80 | | MTIOC3B | SCK10 | | |
| 66 | | PC4 | A20/CS3# | MTIOC3D/MTCLKC/TMCI1/ POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0 | | |
| 67 | | PC3 | A19 | MTIOC4D/TCLKB | TXD5/SMOSI5/SSDA5 | | |
| 68 | | P77 | | | TXD11/SMOSI11/SSDA11 | | |
| 69 | | P76 | | | RXD11/SMISO11/SSCL11 | | |
| 70 | | PC2 | A18 | MTIOC4B/TCLKA | RXD5/SMISO5/SSCL5/SSLA3 | | |
| 71 | | P75 | | | SCK11 | | |
| 72 | | P74 | | | CTS11#/RTS11#/SS11# | | |
| 73 | | PC1 | A17 | MTIOC3A/TCLKD | SCK5/SSLA2/SDA3 | IRQ12 | |
| 74 | | PL1 | | | | | |
| 75 | | PC0 | A16 | MTIOC3C/TCLKC | CTS5#/RTS5#/SS5#/SSLA1/ SCL3 | | |
| 76 | | PL0 | | | | | |
| 77 | | P73*1 | | | | IRQ12 | |
| | | PL5*1 | | | CECIO | IRQ12 | |
| 78 | | PB7 | A15 | MTIOC3B/TIOCB5 | TXD9/SMOSI9/SSDA9 | | |

**Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (3 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TPU, TMR, POE, PPG, CAC) | Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR) | Interrupt | AD, DA |
|---|---|---|---|---|---|---|---|
| 79 | | PB6 | A14 | MTIOC3D/TIOCA5 | RXD9/SMISO9/SSCL9 | | |
| 80 | | PB5 | A13 | MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/POE1# | SCK9 | | |
| 81 | | PB4 | A12 | TIOCA4 | CTS9#/RTS9#/SS9# | | |
| 82 | | PB3 | A11 | MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ POE3# | SCK4/SCK6 | | |
| 83 | | PB2 | A10 | TIOCC3/TCLKC | CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6# | | |
| 84 | | PB1 | A9 | MTIOC0C/MTIOC4C/ TIOCB3/TMCI0 | TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6 | IRQ4_DS | |
| 85 | | P72 | | | | | |
| 86 | | P71 | | | | | |
| 87 | | PB0 | A8 | MTIC5W/TIOCA3 | RXD4/SMISO4/SSCL4/RXD6/ SMISO6/SSCL6/RSPCKA | IRQ12 | |
| 88 | | PA7 | A7 | TIOCB2 | MISOA | | |
| 89 | | PA6 | A6 | MTIC5V/MTCLKB/TIOCA2/ TMCI3/POE2# | CTS5#/RTS5#/SS5#/MOSIA | | |
| 90 | | PA5 | A5 | TIOCB1 | RSPCKA | | |
| 91 | VCC | | | | | | |
| 92 | | PA4 | A4 | MTIC5U/MTCLKA/TIOCA1/ TMRI0 | TXD5/SMOSI5/SSDA5/SSLA0 | IRQ5_DS | |
| 93 | VSS | | | | | | |
| 94 | | PA3 | A3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB | RXD5/SMISO5/SSCL5 | IRQ6_DS | |
| 95 | | PA2 | A2 | | RXD5/SMISO5/SSCL5/SSLA3 | | |
| 96 | | PA1 | A1 | MTIOC0B/MTCLKC/TIOCB0 | SCK5/SSLA2 | IRQ11 | |
| 97 | | PA0 | A0/BC0# | MTIOC4A/TIOCA0/CACREF | SSLA1 | | |
| 98 | | P67 | | | | | |
| 99 | | P66 | | | | | |
| 100 | | P65 | | | | | |
| 101 | | PE7 | D15 [A15/D15] | | MISOB | IRQ7 | AN015 |
| 102 | | PE6 | D14 [A14/D14] | | CTS4#/RTS4#/SS4#/MOSIB | IRQ6 | AN014 |
| 103 | | PK5 | | | TXD4/SMOSI4/SSDA4 | | |
| 104 | | P70 | | | SCK4 | | |
| 105 | | PK4 | | | RXD4/SMISO4/SSCL4 | | |
| 106 | | PE5 | D13 [A13/D13] | MTIOC4C/MTIOC2B | RSPCKB | IRQ5 | AN013 |
| 107 | | PE4 | D12 [A12/D12] | MTIOC4D/MTIOC1A | SSLB0 | | AN012 |
| 108 | | PE3 | D11 [A11/D11] | MTIOC4B/POE8# | CTS12#/RTS12#/SS12#/ MISOB | | AN011 |
| 109 | | PE2 | D10 [A10/D10] | MTIOC4A | RXD12/RXDX12/SMISO12/ SSCL12/SSLB3/MOSIB | IRQ7_DS | AN010 |
| 110 | | PE1 | D9 [A9/D9] | MTIOC4C | TXD12/TXDX12/SMOSI12/ SSDA12/SSLB2/RSPCKB/ SIOX12 | | AN009 |
| 111 | | PE0 | D8 [A8/D8] | | SCK12/SSLB1 | | AN008 |
| 112 | | P64 | | | | | |
| 113 | | P63 | | | | | |
| 114 | | P62 | | | | | |
| 115 | | P61 | | | CTS9#/RTS9#/SS9# | | |
| 116 | | PK3 | | | RXD9/SMISO9/SSCL9 | | |
| 117 | | P60 | | | SCK9 | | |

**Table 1.5 List of Pins and Pin Functions (144-Pin LQFP) (4 / 4)**

| Pin No. | Power Supply, Clock, System Control | I/O Port | External Bus | Timers (MTU, TPU, TMR, POE, PPG, CAC) | Communications (SCIe, SCIf, RSPI, RIIC, CEC, RCR) | Interrupt | AD, DA |
|---|---|---|---|---|---|---|---|
| 118 | | PK2 | | | TXD9/SMOSI9/SSDA9 | | |
| 119 | | PD7 | D7 [A7/D7] | MTIC5U/POE0# | | IRQ7 | |
| 120 | | PD6 | D6 [A6/D6] | MTIC5V/POE1# | | IRQ6 | |
| 121 | | PD5 | D5 [A5/D5] | MTIC5W/POE2# | | IRQ5 | |
| 122 | | PD4 | D4 [A4/D4] | POE3# | | IRQ4 | |
| 123 | | PD3 | D3 [A3/D3] | POE8# | | IRQ3 | |
| 124 | | PD2 | D2 [A2/D2] | MTIOC4D | | IRQ2 | |
| 125 | | PD1 | D1 [A1/D1] | MTIOC4B | | IRQ1 | |
| 126 | | PD0 | D0 [A0/D0] | | | IRQ0 | |
| 127 | | P93 | | | CTS7#/RTS7#/SS7# | | |
| 128 | | P92 | | | RXD7/SMISO7/SSCL7 | | |
| 129 | | P91 | | | SCK7 | | |
| 130 | VSS | | | | | | |
| 131 | | P90 | | | TXD7/SMOSI7/SSDA7 | | |
| 132 | VCC | | | | | | |
| 133 | | P47 | | | | | AN007 |
| 134 | | P46 | | | | | AN006 |
| 135 | | P45 | | | | | AN005 |
| 136 | | P44 | | | | | AN004 |
| 137 | | P43 | | | | | AN003 |
| 138 | | P42 | | | | | AN002 |
| 139 | | P41 | | | | | AN001 |
| 140 | VREFL0 | | | | | | |
| 141 | | P40 | | | | | AN000 |
| 142 | VREFH0 | | | | | | |
| 143 | AVCC0 | | | | | | |
| 144 | | P07 | | | | | ADTRG0# |

Note 1. Pin 77 is available as P73 in 5-V packages, and PL5 in 3-V packages.

# 3. Address Space

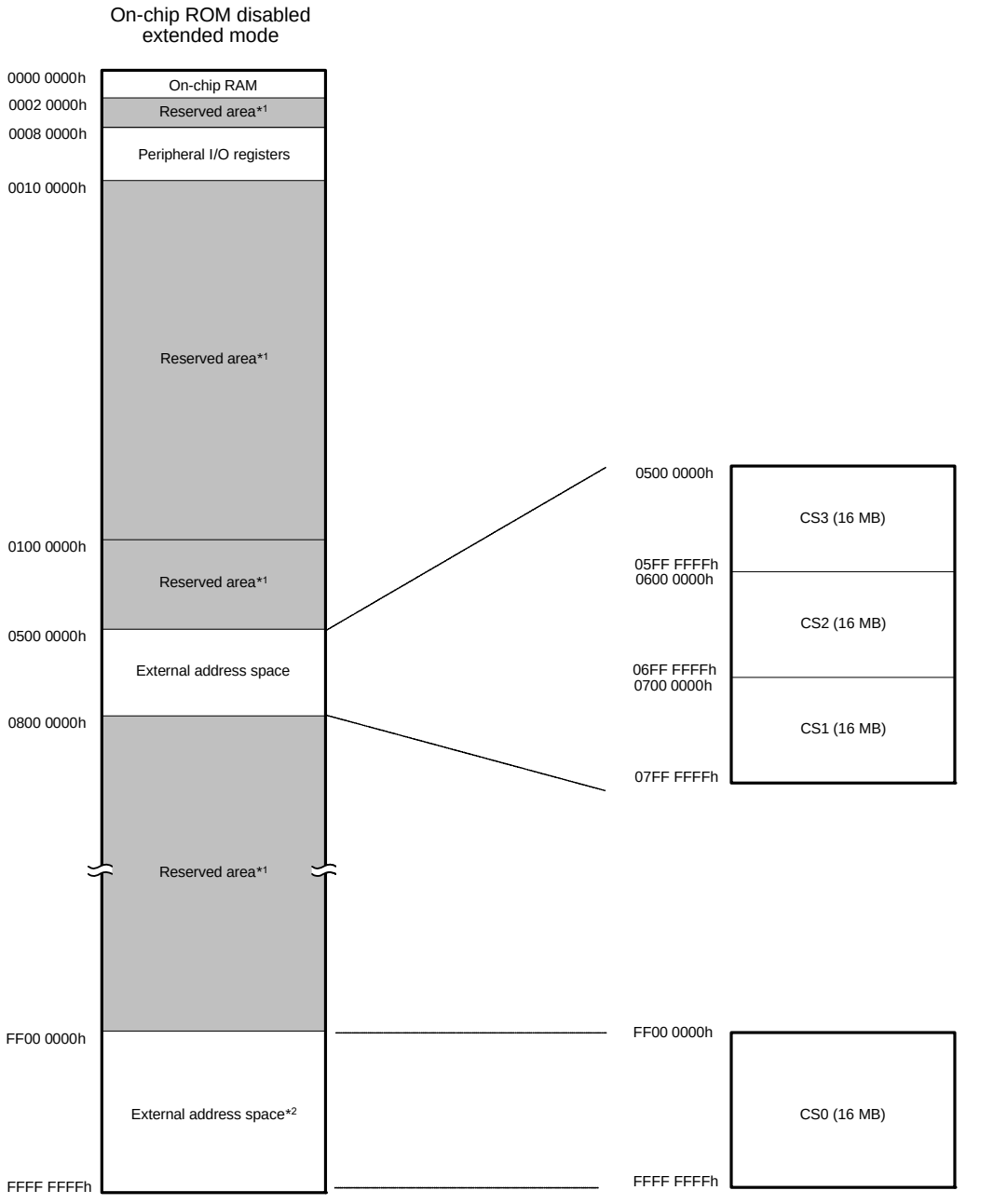
## 3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

## 3.2 External Address Space

The external address space is divided into up to four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.




Note 1. Reserved areas should not be accessed.

Note 2. The CS0 area is disabled in on-chip ROM enabled extended mode. In this mode, the address space for addresses above 0800 0000h is as shown in figure on this section “Memory Map in Each Operating Mode”.

**Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)**

**Table 4.1 List of I/O Registers (Address Order) (12 / 34)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 73BAh | ICU | Interrupt Source Priority Register 186 | IPR186 | 8 | 8 | 2 ICLK | | ICUb | |
| 0008 73BEh | ICU | Interrupt Source Priority Register 190 | IPR190 | 8 | 8 | 2 ICLK | | | |
| 0008 73C2h | ICU | Interrupt Source Priority Register 194 | IPR194 | 8 | 8 | 2 ICLK | | | |
| 0008 73C6h | ICU | Interrupt Source Priority Register 198 | IPR198 | 8 | 8 | 2 ICLK | | | |
| 0008 73C7h | ICU | Interrupt Source Priority Register 199 | IPR199 | 8 | 8 | 2 ICLK | | | |
| 0008 73C8h | ICU | Interrupt Source Priority Register 200 | IPR200 | 8 | 8 | 2 ICLK | | | |
| 0008 73C9h | ICU | Interrupt Source Priority Register 201 | IPR201 | 8 | 8 | 2 ICLK | | | |
| 0008 73CAh | ICU | Interrupt Source Priority Register 202 | IPR202 | 8 | 8 | 2 ICLK | | | |
| 0008 73CBh | ICU | Interrupt Source Priority Register 203 | IPR203 | 8 | 8 | 2 ICLK | | | |
| 0008 73CCh | ICU | Interrupt Source Priority Register 204 | IPR204 | 8 | 8 | 2 ICLK | | | |
| 0008 73CDh | ICU | Interrupt Source Priority Register 205 | IPR205 | 8 | 8 | 2 ICLK | | | |
| 0008 73CEh | ICU | Interrupt Source Priority Register 206 | IPR206 | 8 | 8 | 2 ICLK | | | |
| 0008 73D2h | ICU | Interrupt Source Priority Register 210 | IPR210 | 8 | 8 | 2 ICLK | | | |
| 0008 73D6h | ICU | Interrupt Source Priority Register 214 | IPR214 | 8 | 8 | 2 ICLK | | | |
| 0008 73DAh | ICU | Interrupt Source Priority Register 218 | IPR218 | 8 | 8 | 2 ICLK | | | |
| 0008 73DEh | ICU | Interrupt Source Priority Register 222 | IPR222 | 8 | 8 | 2 ICLK | | | |
| 0008 73E2h | ICU | Interrupt Source Priority Register 226 | IPR226 | 8 | 8 | 2 ICLK | | | |
| 0008 73E6h | ICU | Interrupt Source Priority Register 230 | IPR230 | 8 | 8 | 2 ICLK | | | |
| 0008 73EAh | ICU | Interrupt Source Priority Register 234 | IPR234 | 8 | 8 | 2 ICLK | | | |
| 0008 73EEh | ICU | Interrupt Source Priority Register 238 | IPR238 | 8 | 8 | 2 ICLK | | | |
| 0008 73F2h | ICU | Interrupt Source Priority Register 242 | IPR242 | 8 | 8 | 2 ICLK | | | |
| 0008 73F3h | ICU | Interrupt Source Priority Register 243 | IPR243 | 8 | 8 | 2 ICLK | | | |
| 0008 73F4h | ICU | Interrupt Source Priority Register 244 | IPR244 | 8 | 8 | 2 ICLK | | | |
| 0008 73F5h | ICU | Interrupt Source Priority Register 245 | IPR245 | 8 | 8 | 2 ICLK | | | |
| 0008 73F6h | ICU | Interrupt Source Priority Register 246 | IPR246 | 8 | 8 | 2 ICLK | | | |
| 0008 73F7h | ICU | Interrupt Source Priority Register 247 | IPR247 | 8 | 8 | 2 ICLK | | | |
| 0008 73F8h | ICU | Interrupt Source Priority Register 248 | IPR248 | 8 | 8 | 2 ICLK | | | |
| 0008 73F9h | ICU | Interrupt Source Priority Register 249 | IPR249 | 8 | 8 | 2 ICLK | | | |
| 0008 73FAh | ICU | Interrupt Source Priority Register 250 | IPR250 | 8 | 8 | 2 ICLK | | | |
| 0008 7400h | ICU | DMAC Activation Request Select Register 0 | DMRSR0 | 8 | 8 | 2 ICLK | | | |
| 0008 7404h | ICU | DMAC Activation Request Select Register 1 | DMRSR1 | 8 | 8 | 2 ICLK | | | |
| 0008 7408h | ICU | DMAC Activation Request Select Register 2 | DMRSR2 | 8 | 8 | 2 ICLK | | | |
| 0008 740Ch | ICU | DMAC Activation Request Select Register 3 | DMRSR3 | 8 | 8 | 2 ICLK | | | |
| 0008 7500h | ICU | IRQ Control Register 0 | IRQCR0 | 8 | 8 | 2 ICLK | | | |
| 0008 7501h | ICU | IRQ Control Register 1 | IRQCR1 | 8 | 8 | 2 ICLK | | | |
| 0008 7502h | ICU | IRQ Control Register 2 | IRQCR2 | 8 | 8 | 2 ICLK | | | |
| 0008 7503h | ICU | IRQ Control Register 3 | IRQCR3 | 8 | 8 | 2 ICLK | | | |
| 0008 7504h | ICU | IRQ Control Register 4 | IRQCR4 | 8 | 8 | 2 ICLK | | | |
| 0008 7505h | ICU | IRQ Control Register 5 | IRQCR5 | 8 | 8 | 2 ICLK | | | |
| 0008 7506h | ICU | IRQ Control Register 6 | IRQCR6 | 8 | 8 | 2 ICLK | | | |
| 0008 7507h | ICU | IRQ Control Register 7 | IRQCR7 | 8 | 8 | 2 ICLK | | | |
| 0008 7508h | ICU | IRQ Control Register 8 | IRQCR8 | 8 | 8 | 2 ICLK | | | |
| 0008 7509h | ICU | IRQ Control Register 9 | IRQCR9 | 8 | 8 | 2 ICLK | | | |
| 0008 750Ah | ICU | IRQ Control Register 10 | IRQCR10 | 8 | 8 | 2 ICLK | | | |
| 0008 750Bh | ICU | IRQ Control Register 11 | IRQCR11 | 8 | 8 | 2 ICLK | | | |
| 0008 750Ch | ICU | IRQ Control Register 12 | IRQCR12 | 8 | 8 | 2 ICLK | | | |
| 0008 750Dh | CEC | CEC Interrupt Control Register 1 | CECINTCR1 | 8 | 8 | 2 ICLK | | CEC | Not available in 5-V packages. |

**Table 4.1 List of I/O Registers (Address Order) (17 / 34)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 836Fh | RIIC3 | Slave Address Register U2 | SARU2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | RIIC | |
| 0008 8370h | RIIC3 | I²C Bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8371h | RIIC3 | I²C Bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8372h | RIIC3 | I²C Bus Transmit Data Register | ICDRT | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8373h | RIIC3 | I²C Bus Receive Data Register | ICDRR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8380h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | RSPI | |
| 0008 8381h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8382h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8383h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8384h | RSPI0 | RSPI Data Register | SPDR | 32 | 16, 32 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8388h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8389h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Dh | RSPI0 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Eh | RSPI0 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 838Fh | RSPI0 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8390h | RSPI0 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8392h | RSPI0 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8394h | RSPI0 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8396h | RSPI0 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8398h | RSPI0 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 839Ah | RSPI0 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 839Ch | RSPI0 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 839Eh | RSPI0 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A0h | RSPI1 | RSPI Control Register | SPCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A1h | RSPI1 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A2h | RSPI1 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A3h | RSPI1 | RSPI Status Register | SPSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A4h | RSPI1 | RSPI Data Register | SPDR | 32 | 16, 32 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A8h | RSPI1 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83A9h | RSPI1 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83AAh | RSPI1 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83ABh | RSPI1 | RSPI Data Control Register | SPDCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83ACh | RSPI1 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83ADh | RSPI1 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83AEh | RSPI1 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83AFh | RSPI1 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83B0h | RSPI1 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83B2h | RSPI1 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83B4h | RSPI1 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83B6h | RSPI1 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83B8h | RSPI1 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83BAh | RSPI1 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83BCh | RSPI1 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 83BEh | RSPI1 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8600h | MTU3 | Timer Control Register | TCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | MTU2a | |
| 0008 8601h | MTU4 | Timer Control Register | TCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 8602h | MTU3 | Timer Mode Register | TMDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (21 / 34)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 A004h | SCI0 | Serial Status Register | SSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | SCIe, SCIf | |
| 0008 A005h | SCI0 | Receive Data Register | RDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A006h | SCI0 | Smart Card Mode Register | SCMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A007h | SCI0 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A008h | SCI0 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A009h | SCI0 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A00Ah | SCI0 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A00Bh | SCI0 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A00Ch | SCI0 | $I^2C$ Status Register | SISR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A00Dh | SCI0 | SPI Mode Register | SPMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A020h | SCI1 | Serial Mode Register | SMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A021h | SCI1 | Bit Rate Register | BRR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A022h | SCI1 | Serial Control Register | SCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A023h | SCI1 | Transmit Data Register | TDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A024h | SCI1 | Serial Status Register | SSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A025h | SCI1 | Receive Data Register | RDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A026h | SCI1 | Smart Card Mode Register | SCMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A027h | SCI1 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A028h | SCI1 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A029h | SCI1 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A02Ah | SCI1 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A02Bh | SCI1 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A02Ch | SCI1 | $I^2C$ Status Register | SISR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A02Dh | SCI1 | SPI Mode Register | SPMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A040h | SCI2 | Serial Mode Register | SMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A041h | SCI2 | Bit Rate Register | BRR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A042h | SCI2 | Serial Control Register | SCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A043h | SCI2 | Transmit Data Register | TDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A044h | SCI2 | Serial Status Register | SSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A045h | SCI2 | Receive Data Register | RDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A046h | SCI2 | Smart Card Mode Register | SCMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A047h | SCI2 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A048h | SCI2 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A049h | SCI2 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A04Ah | SCI2 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A04Bh | SCI2 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A04Ch | SCI2 | $I^2C$ Status Register | SISR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A04Dh | SCI2 | SPI Mode Register | SPMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A060h | SCI3 | Serial Mode Register | SMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A061h | SCI3 | Bit Rate Register | BRR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A062h | SCI3 | Serial Control Register | SCR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A063h | SCI3 | Transmit Data Register | TDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A064h | SCI3 | Serial Status Register | SSR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A065h | SCI3 | Receive Data Register | RDR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A066h | SCI3 | Smart Card Mode Register | SCMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A067h | SCI3 | Serial Extended Mode Register | SEMR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A068h | SCI3 | Noise Filter Setting Register | SNFR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A069h | SCI3 | $I^2C$ Mode Register 1 | SIMR1 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A06Ah | SCI3 | $I^2C$ Mode Register 2 | SIMR2 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A06Bh | SCI3 | $I^2C$ Mode Register 3 | SIMR3 | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 A06Ch | SCI3 | $I^2C$ Status Register | SISR | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (30 / 34)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 0008 C19Ch | MPC | PB4 Pin Function Control Registers | PB4PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | MPC | |
| 0008 C19Dh | MPC | PB5 Pin Function Control Registers | PB5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C19Eh | MPC | PB6 Pin Function Control Registers | PB6PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C19Fh | MPC | PB7 Pin Function Control Registers | PB7PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A0h | MPC | PC0 Pin Function Control Registers | PC0PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A1h | MPC | PC1 Pin Function Control Registers | PC1PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A2h | MPC | PC2 Pin Function Control Registers | PC2PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A3h | MPC | PC3 Pin Function Control Registers | PC3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A4h | MPC | PC4 Pin Function Control Registers | PC4PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A5h | MPC | PC5 Pin Function Control Registers | PC5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A6h | MPC | PC6 Pin Function Control Registers | PC6PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A7h | MPC | PC7 Pin Function Control Registers | PC7PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A8h | MPC | PD0 Pin Function Control Registers | PD0PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1A9h | MPC | PD1 Pin Function Control Registers | PD1PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1AAh | MPC | PD2 Pin Function Control Registers | PD2PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1ABh | MPC | PD3 Pin Function Control Registers | PD3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1ACh | MPC | PD4 Pin Function Control Registers | PD4PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1ADh | MPC | PD5 Pin Function Control Registers | PD5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1AEh | MPC | PD6 Pin Function Control Registers | PD6PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1AFh | MPC | PD7 Pin Function Control Registers | PD7PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B0h | MPC | PE0 Pin Function Control Registers | PE0PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B1h | MPC | PE1 Pin Function Control Registers | PE1PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B2h | MPC | PE2 Pin Function Control Registers | PE2PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B3h | MPC | PE3 Pin Function Control Registers | PE3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B4h | MPC | PE4 Pin Function Control Registers | PE4PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B5h | MPC | PE5 Pin Function Control Registers | PE5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B6h | MPC | PE6 Pin Function Control Registers | PE6PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1B7h | MPC | PE7 Pin Function Control Registers | PE7PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1BDh | MPC | PF5 Pin Function Control Registers | PF5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1C8h | MPC | PH0 Pin Function Control Registers | PH0PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1C9h | MPC | PH1 Pin Function Control Registers | PH1PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1CAh | MPC | PH2 Pin Function Control Registers | PH2PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1CBh | MPC | PH3 Pin Function Control Registers | PH3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1D1h | MPC | PJ1 Pin Function Control Registers | PJ1PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1D3h | MPC | PJ3 Pin Function Control Registers | PJ3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1DAh | MPC | PK2 Pin Function Control Registers | PK2PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1DBh | MPC | PK3 Pin Function Control Registers | PK3PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1DCh | MPC | PK4 Pin Function Control Registers | PK4PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1DDh | MPC | PK5 Pin Function Control Registers | PK5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | |
| 0008 C1E5h | MPC | PL5 Pin Function Control Register | PL5PFS | 8 | 8 | 2 to 3PCLKB | 2 ICLK | | Not available in 5-V packages. |
| 0008 C280h | SYSTEM | Deep Standby Control Register | DPSBYCR | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | Low Power Consumption | |
| 0008 C282h | SYSTEM | Deep Standby Interrupt Enable Register 0 | DPSIER0 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C284h | SYSTEM | Deep Standby Interrupt Enable Register 2 | DPSIER2 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C286h | SYSTEM | Deep Standby Interrupt Flag Register 0 | DPSIFR0 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C288h | SYSTEM | Deep Standby Interrupt Flag Register 2 | DPSIFR2 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C28Ah | SYSTEM | Deep Standby Interrupt Edge Register 0 | DPSIEGR0 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C28Ch | SYSTEM | Deep Standby Interrupt Edge Register 2 | DPSIEGR2 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | Resets | |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4 to 5PCLKB | 2 to 3 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (33 / 34)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function | Remarks |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | | |
| 000A 0B16h | RCR0 | Receive Data 0 Register | DAT0 | 8 | 8 | 1 to 2PCLK | 1 ICLK | RCR | Not available in 5-V packages. |
| 000A 0B17h | RCR0 | Receive Data 1 Register | DAT1 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B18h | RCR0 | Receive Data 2 Register | DAT2 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B19h | RCR0 | Receive Data 3 Register | DAT3 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B1Ah | RCR0 | Receive Data 4 Register | DAT4 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B1Bh | RCR0 | Receive Data 5 Register | DAT5 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B1Ch | RCR0 | Receive Data 6 Register | DAT6 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B1Dh | RCR0 | Receive Data 7 Register | DAT7 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B1Eh | RCR0 | Measurement Result Register | TIM | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B80h | RCR1 | Function Select Register 0 | CON0 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B81h | RCR1 | Function Select Register 1 | CON1 | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B82h | RCR1 | Status Register | STS | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B83h | RCR1 | Interrupt Control Register | INT | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B84h | RCR1 | Compare Control Register | CPC | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B85h | RCR1 | Compare Value Setting Register | CPD | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B86h | RCR1 | Header Pattern Setting Register (Min) | HDPMIN | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B88h | RCR1 | Header Pattern Setting Register (Max) | HDPMAX | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B8Ah | RCR1 | Data 0 Pattern Setting Register (Min) | D0PMIN | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B8Bh | RCR1 | Data 0 Pattern Setting Register (Max) | D0PMAX | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B8Ch | RCR1 | Data 1 Pattern Setting Register (Min) | D1PMIN | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B8Dh | RCR1 | Data 1 Pattern Setting Register (Max) | D1PMAX | 8 | 8 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B8Eh | RCR1 | Special Data Pattern Setting Register (Min) | SDPMIN | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B90h | RCR1 | Special Data Pattern Setting Register (Max) | SDPMAX | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |
| 000A 0B92h | RCR1 | Pattern End Setting Register | PE | 16 | 16 | 1 to 2PCLK | 1 ICLK | | Not available in 5-V packages. |

### Table 5.6 DC Characteristics (5)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

| Item | | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Supply current*1 | Low-speed operating mode 1 | Normal operating mode | No peripheral operation*2 | ICLK = 1 MHz | $I_{CC}$ | 4 | — | mA | |
| | | | All peripheral operation: Normal*3 | ICLK = 1 MHz | | 4.2 | — | | |
| | | | All peripheral operation: Max.*3 | ICLK = 1 MHz | | — | 15 | | |
| | | Sleep mode | No peripheral operation | ICLK = 1 MHz | | 3.8 | — | | |
| | | | All peripheral operation: Normal | ICLK = 1 MHz | | 4.0 | — | | |
| | | All-module clock stop mode | | | | 3.7 | — | | |
| | Low-speed operating mode 2 | Normal operating mode | No peripheral operation*4 | ICLK = 125 kHz | | 0.4 | — | | |
| | | | All peripheral operation: Normal*5 | ICLK = 125 kHz | | 0.5 | — | | |
| | | | All peripheral operation: Max.*5 | ICLK = 125 kHz | | — | 8*6 | | |
| | | Sleep mode | No peripheral operation | ICLK = 125 kHz | | 0.3 | — | | |
| | | | All peripheral operation: Normal | ICLK = 125 kHz | | 0.4 | — | | |
| | | All-module clock stop mode | | | | 0.28 | — | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is the main clock.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is the main clock.
Note 4. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is LOCO.
Note 5. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is LOCO.
Note 6. Value when the main clock continues oscillating at 13.5 MHz.

### Table 5.7 DC Characteristics (6)

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

| Item | | | | Symbol | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Supply power*1 | Software standby mode | | | $I_{CC}$ | 40 | 1000 | µA | |
| | Deep software standby mode | RAM power supplied | | | 22 | 200 | | |
| | | RAM power not supplied | Power-on reset circuit low power consumption function disabled | | 21 | 60 | | |
| | | | Power-on reset circuit low power consumption function enabled | | 6.2 | 28 | | |

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

**Table 5.12 Output Values of Voltage (1)**

Conditions: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output | $V_{OL}$ | — | 0.5 | V | $I_{OL}$ = 1.0 mA |
| | | High-drive output | | — | 0.5 | | $I_{OL}$ = 2.0 mA |
| | RIIC pins | | | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| | CEC pins | | | — | 0.6 | | $I_{OL}$ = 2.1 mA |
| Output high | All output pins | Normal output | $V_{OH}$ | VCC – 0.5 | — | V | $I_{OH}$ = –1.0 mA |
| | | High-drive output | | VCC – 0.5 | — | | $I_{OH}$ = –2.0 mA |

**Table 5.13 Output Values of Voltage (2)**

Conditions: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V, $T_a$ = –40 to +85°C

| Item | | | Symbol | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Output low | All output pins (other than RIIC) | Normal output | $V_{OL}$ | — | 0.8 | V | $I_{OL}$ = 2.0 mA |
| | | High-drive output | | — | 0.8 | | $I_{OL}$ = 4.0 mA |
| | RIIC pins | | | — | 0.4 | | $I_{OL}$ = 3.0 mA |
| | | | | — | 0.6 | | $I_{OL}$ = 6.0 mA |
| Output high | All output pins | Normal output | $V_{OH}$ | VCC – 0.8 | — | V | $I_{OH}$ = –2.0 mA |
| | | High-drive output | | VCC – 0.8 | — | | $I_{OH}$ = –4.0 mA |

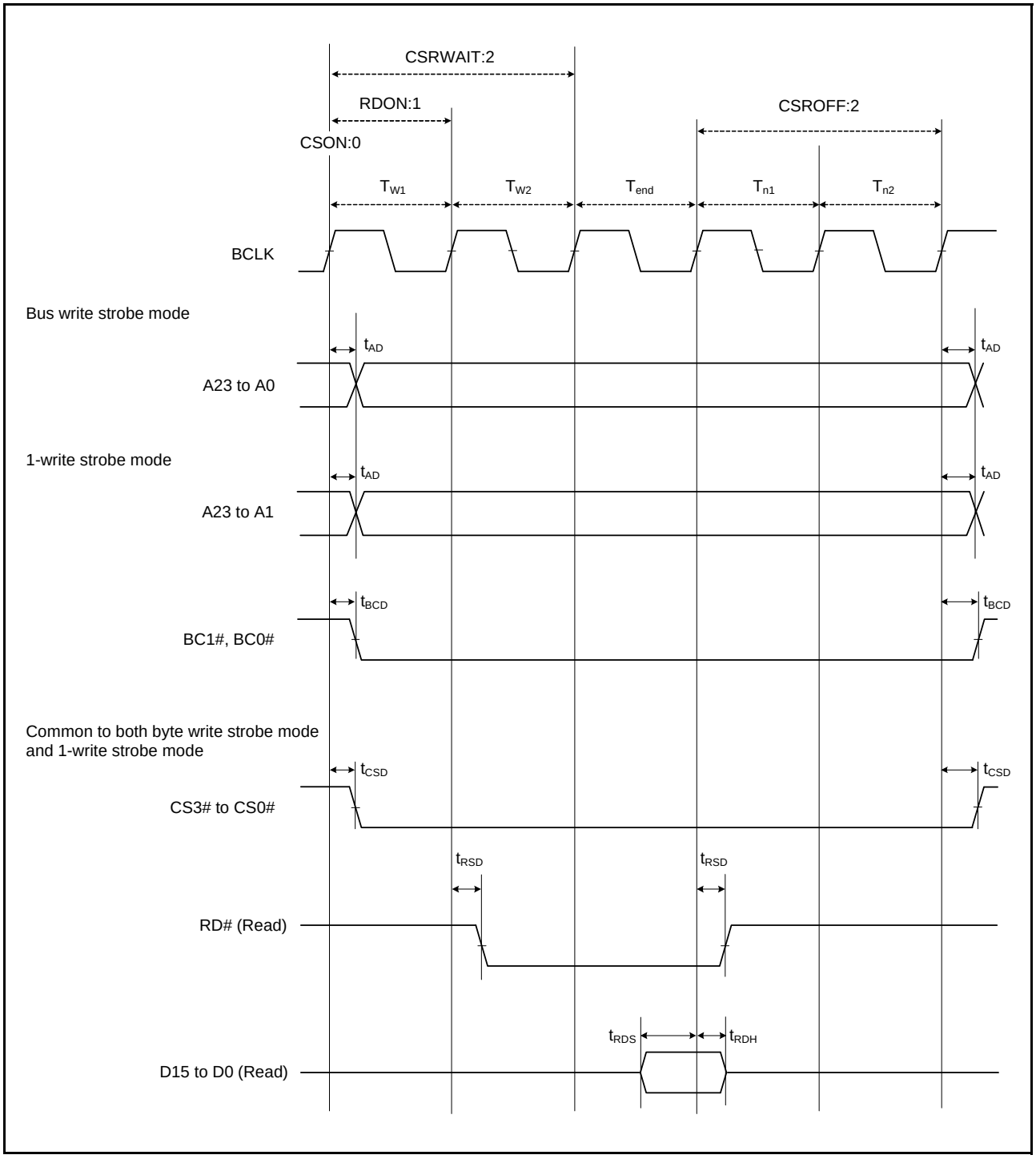



**Figure 5.13 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)**

## 5.3.6 Timing of On-Chip Peripheral Modules

**Table 5.24 Timing of On-Chip Peripheral Modules (1)**

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
$T_a$ = –40 to +85°C
When high-drive output is selected by the drive capacity control register

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
$T_a$ = –40 to +85°C
When high-drive output is selected by the drive capacity control register

| Item | | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---|---|---|---|---|---|---|---|
| I/O ports | Input data pulse width | | $t_{PRW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.20 |
| MTU/TPU | Input capture input pulse width | Single-edge setting | $t_{TICW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.21 |
| | | Both-edge setting | | 2.5 | — | | |
| | Timer clock pulse width | Single-edge setting | $t_{TCKWH}$, $t_{TCKWL}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.22 |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |
| POE | POE# input pulse width | | $t_{POEW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.23 |
| TMR | Timer clock pulse width | Single-edge setting | $t_{TMCWH}$, $t_{TMCWL}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.24 |
| | | Both-edge setting | | 2.5 | — | | |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | $t_{Pcyc}$ | Figure 5.25 |
| | | Clock synchronous | | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 16 | — | $t_{Pcyc}$ | Figure 5.26 |
| | | Clock synchronous | | 4 | — | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | — | 20 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | — | 20 | ns | |
| | Transmit data delay time | Clock synchronous | $t_{TXD}$ | — | 40 | ns | |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 40 | — | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 40 | — | ns | |
| A/D converter | Trigger input pulse width | | $t_{TRGW}$ | 1.5 | — | $t_{Pcyc}$ | Figure 5.27 |
| CAC | CACREF input pulse width | $t_{Pcyc} \le t_{cac}$*2 | $t_{CACREF}$ | 4.5 $t_{cac}$ + 3 $t_{Pcyc}$ | — | ns | |
| | | $t_{Pcyc} > t_{cac}$*2 | | 5 $t_{cac}$ + 6.5 $t_{Pcyc}$ | — | ns | |

Note 1. $t_{Pcyc}$: PCLKB cycle
Note 2. $t_{cac}$: CAC count clock source cycle

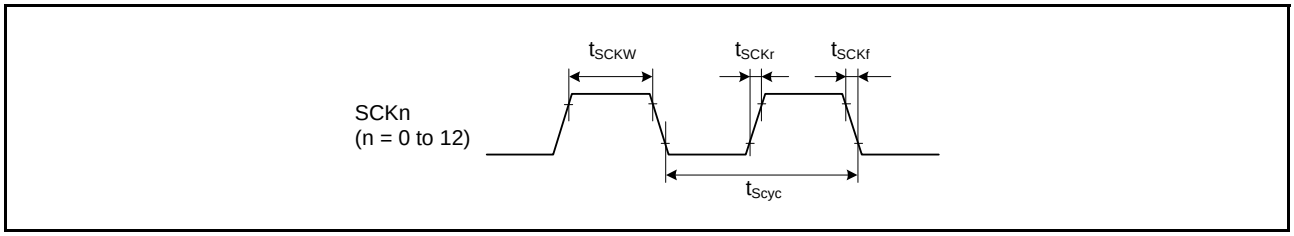



**Figure 5.25 SCK Clock Input Timing**

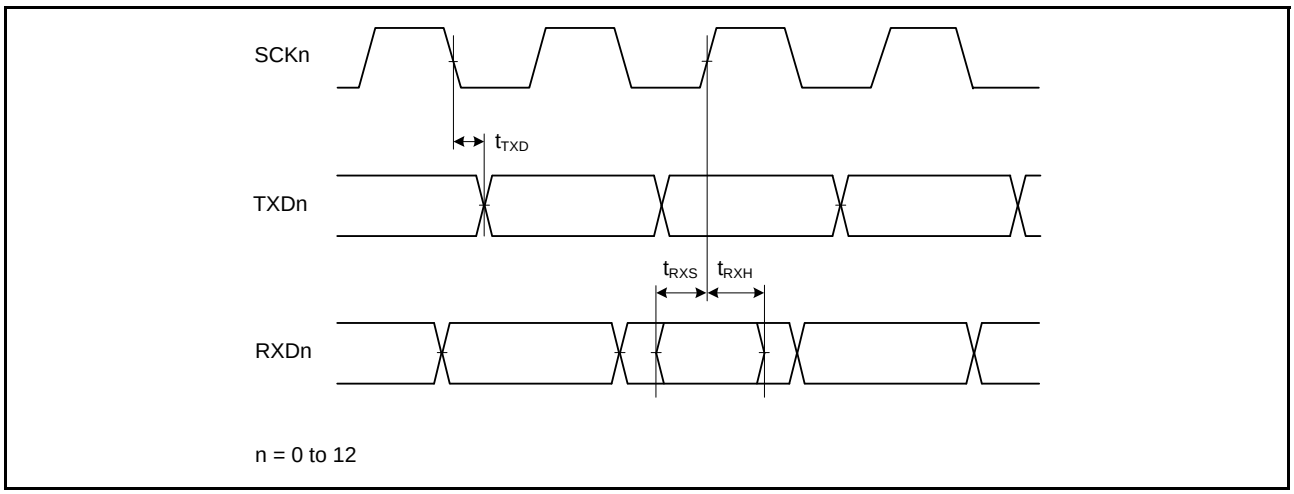



**Figure 5.26 SCI Input/Output Timing: Clock Synchronous Mode**

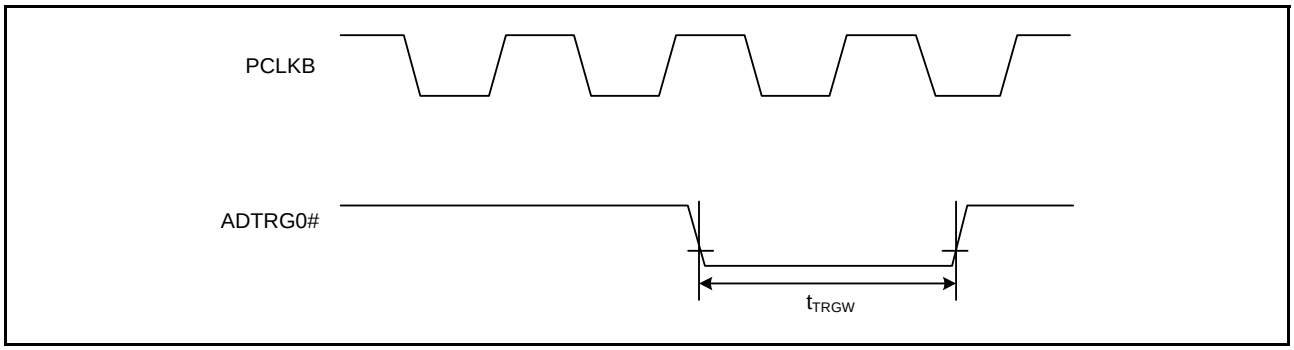



**Figure 5.27 A/D Converter External Trigger Input Timing**

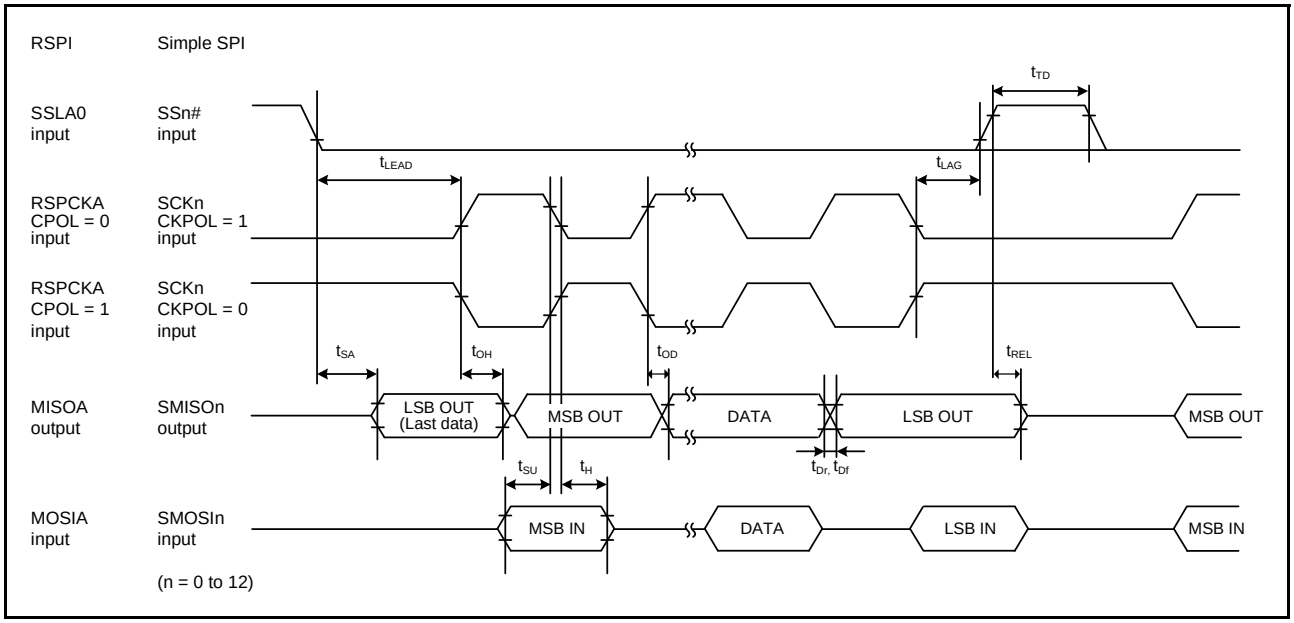
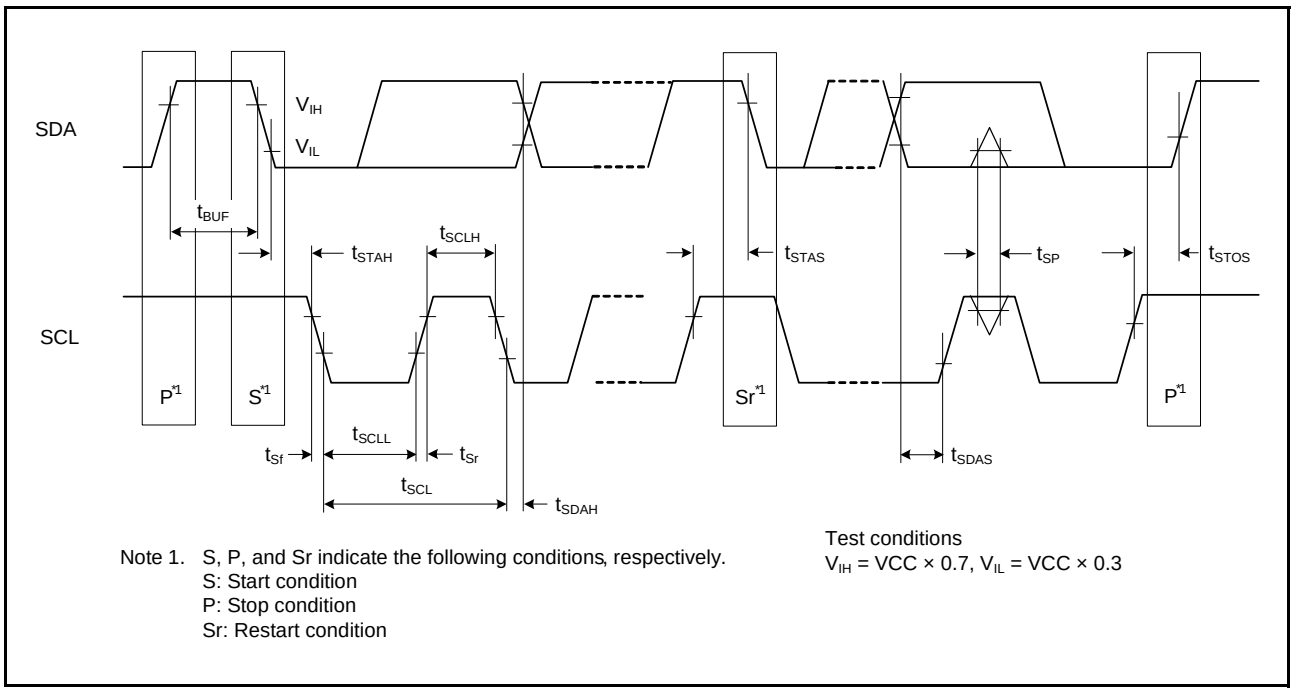



**Figure 5.34 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)**




Note 1. S, P, and Sr indicate the following conditions, respectively.
S: Start condition
P: Stop condition
Sr: Restart condition

Test conditions
$V_{IH}$ = VCC × 0.7, $V_{IL}$ = VCC × 0.3

**Figure 5.35 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing**

### Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

### Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

### Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

## 5.5 D/A Conversion Characteristics

**Table 5.33 D/A Conversion Characteristics (1)**

Conditions 1: VCC = AVCC0 = VREFH0 = 2.7 to 3.6 V, VREFH = 2.7 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
$T_a$ = –40 to +85°C

Conditions 2: VCC = AVCC0 = VREFH0 = 4.0 to 5.5 V, VREFH = 4.0 V to AVCC0, VSS = AVSS0 = VREFL = VREFL0 = 0 V,
$T_a$ = –40 to +85°C

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| Resolution | — | — | 10 | Bit | |
| Conversion time | — | — | ±3.0 | µs | 20-pF capacitive load |
| Absolute accuracy | — | ±3.0 | ±5.0 | LSB | 4-MΩ resistive load |
| | — | — | ±4.0 | LSB | 8-MΩ resistive load |
| RO output resistance | — | 3.6 | — | kΩ | |